

First Results of *0.15 μ m CMOS SOI Pixel Detector*

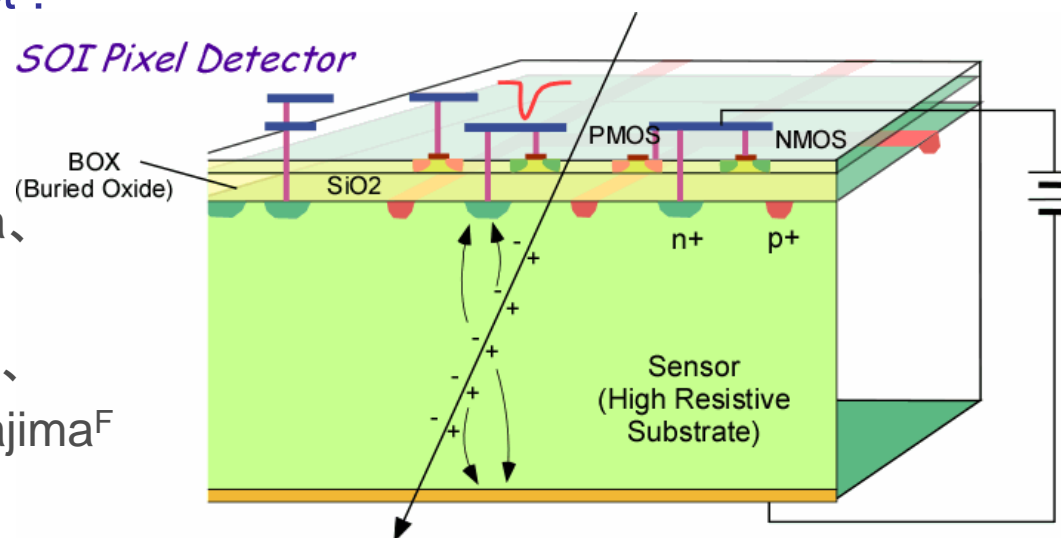
SLAC Exp. Seminar, Apr. 4, 2006

Yasuo Arai (KEK)

KEK Detector Technology Project :
[SOIPIX Group]

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OUTLINE

1. Introduction

What is Silicon-On-Insulator?

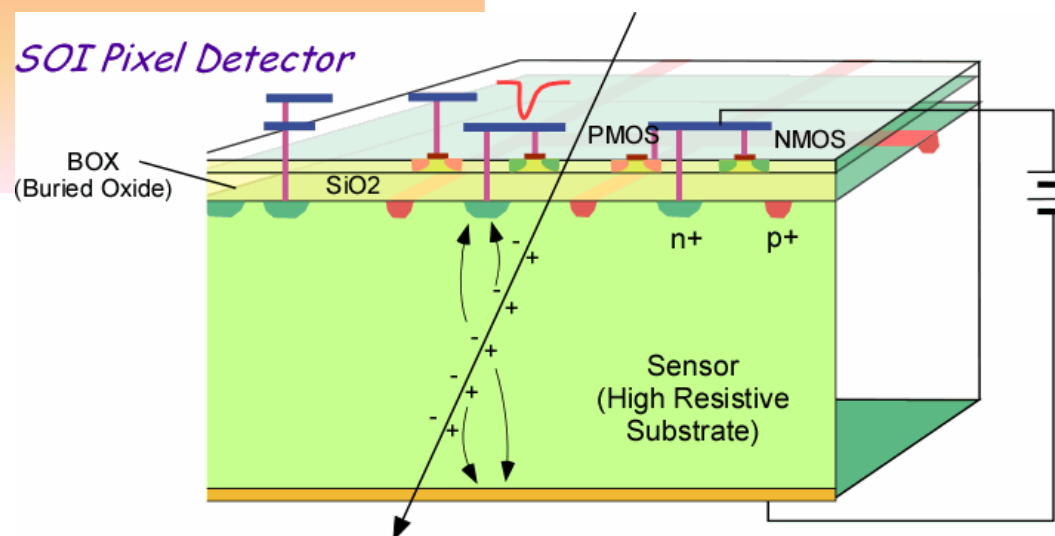
2. SOI Pixel Development at KEK

3. Specific Issues on SOI Pixel

TCAD Simulation

4. Test Results

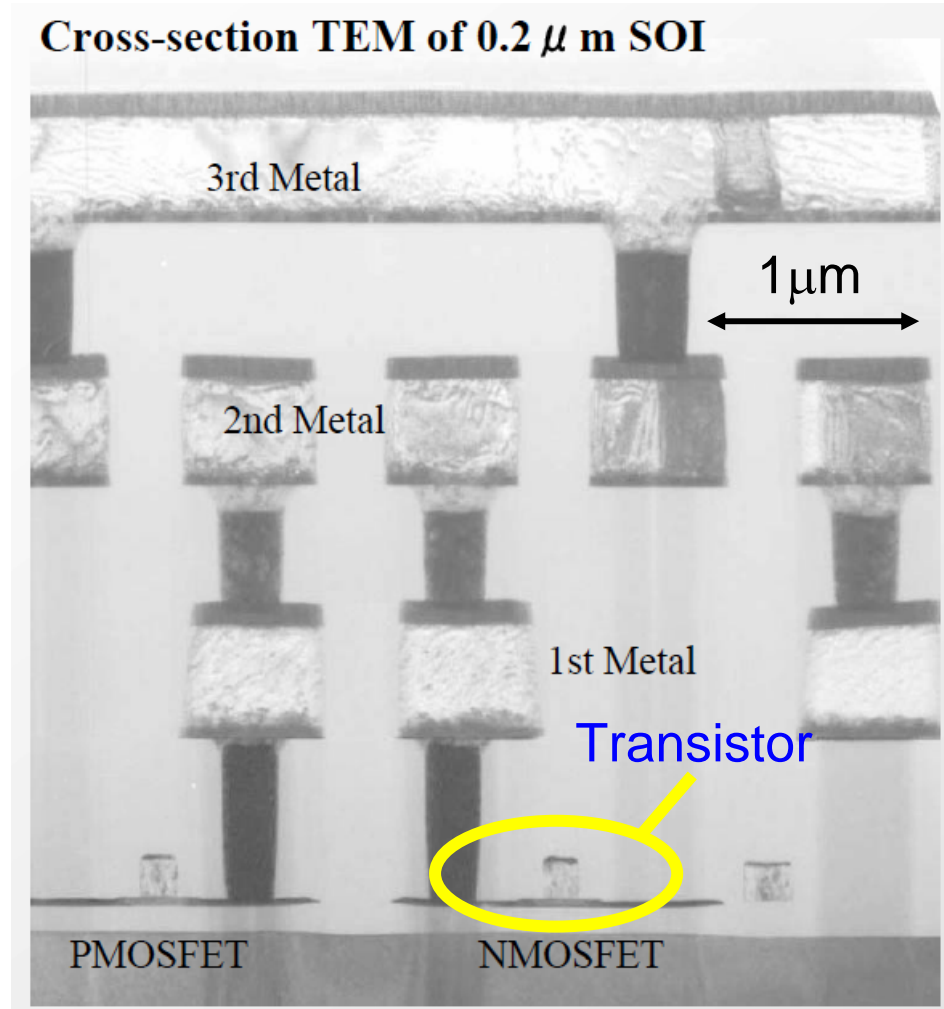
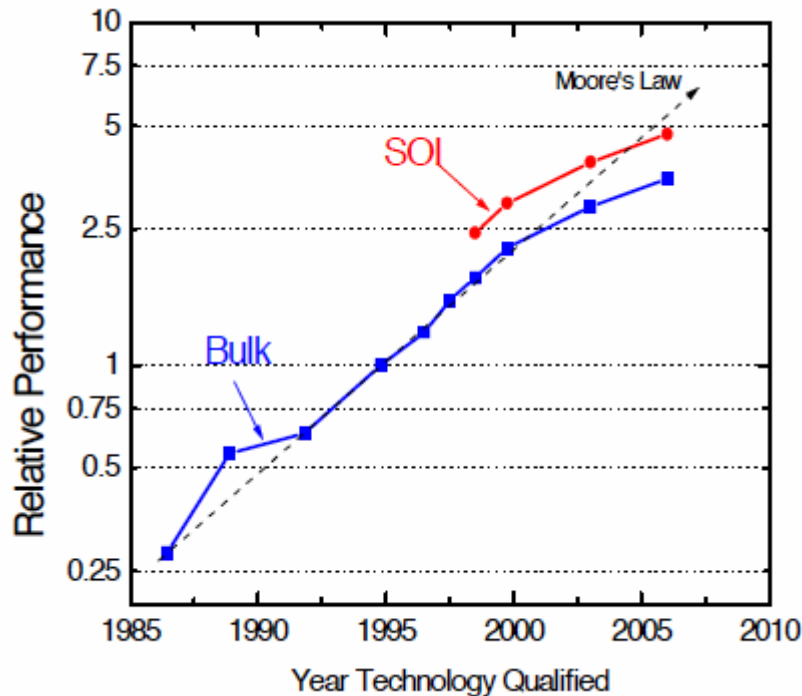
5. Summary



1. Introduction

What is Silicon-On-Insulator?

- A thin layer (50nm ~ 100 μ m) of Si layered on SiO₂
- Higher speed (up to 15%) and Lower power (up to 20%) over Bulk CMOS.

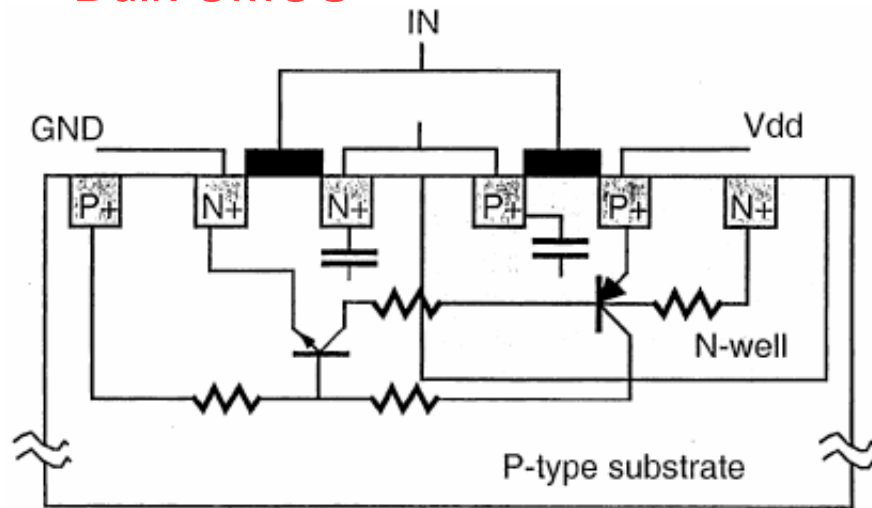


OKI Electric Industry Co., Ltd.

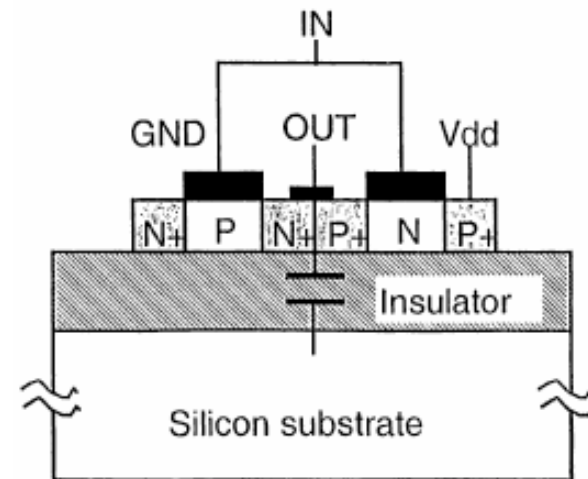
Feature of SOI-CMOS Devices

- Full Dielectric Isolation : *Latchup Free, Small Area*
- Low Junction Capacitance : *High Speed, Low Power*
- Low Leakage, Low V_{th} Shift : *High Temp. (~ 300 °C) Application*
- High Soft Error Immunity : *Rad-Hard application*

Bulk CMOS



SOI CMOS



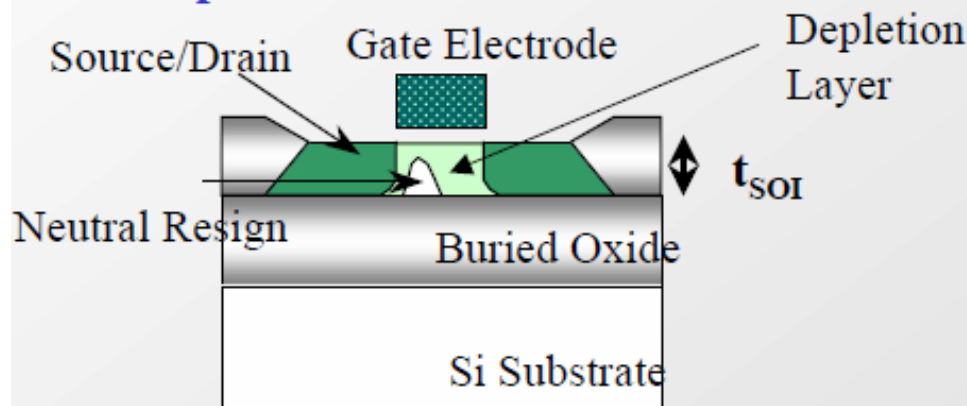
(Ref. 'SOI Technology' by Jean-Pierre Colinge, Springer)

PD vs. FD

PD-SOI (Partially Depleted)

- ◆ Thick SOI Thickness (T_{SOI})
 $\sim 0.1 - 0.2 \mu\text{m}$
- ◆ Depletion Layer $< T_{\text{SOI}}$

- ◇ Large Floating body effect
- ◇ High Drive Current by Kink effect
→ High speed application
- ◇ Compatible Process with Bulk-Si

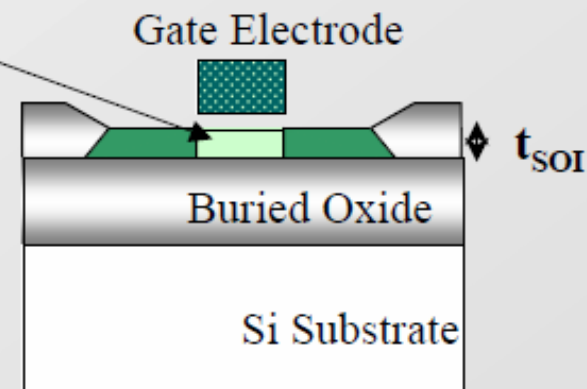


**IBM PowerPC, AMD Athlon,
Sony Cell ...**

FD-SOI (Fully Depleted)

- ◆ Thin SOI Thickness (T_{SOI})
 $< 0.05 \mu\text{m}$
- ◆ Depletion Layer $> T_{\text{SOI}}$

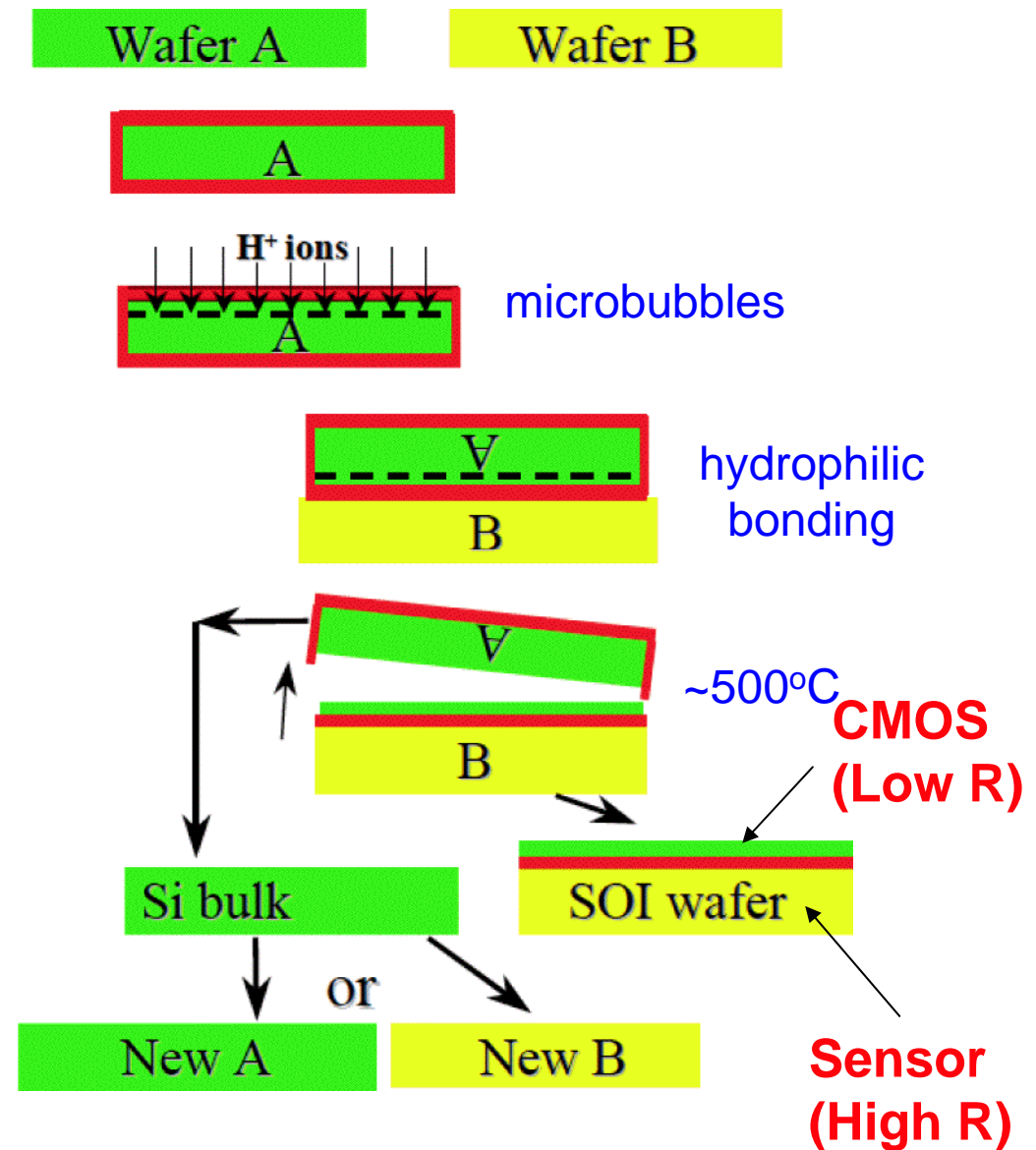
- ◇ Less Floating body effect
- ◇ Better Subthreshold Slopes
→ Low- V_{th} is available
- ◇ Process Issues in thin-film SOI



**OKI Radio Controlled
Wrist Watch (CASIO)**

SOI Wafer Fabrication (UNIBOND™, SOITEC)

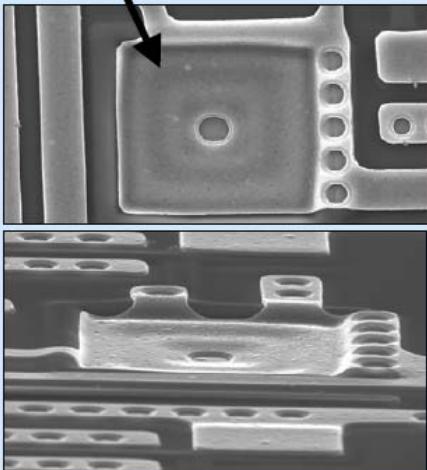
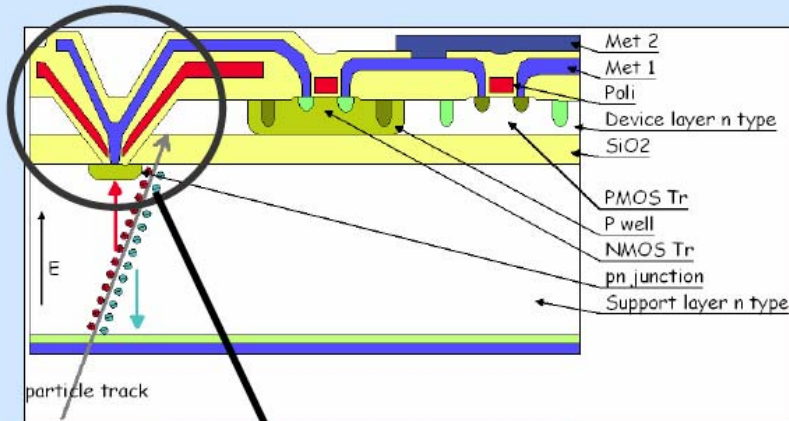
- 1 Initial silicon wafers A & B
- 2 Oxidation of wafer A to create insulating layer
- 3 Smart Cut ion implantation induces formation of an in-depth weakened layer
- 4 Cleaning & bonding wafer A to the handle substrate, wafer B
- 5 Smart Cut - cleavage at the mean ion penetration depth splits off wafer A
- 6 Wafer B undergoes annealing, CMP and touch polish => SOI wafer complete
- 8 Split-off wafer A is recycled, becoming the new wafer A or B



Previous Activity



Principle of SOI monolithic detector



W.Kucewicz

Vertex 2004 - Villa Vigoni, Menaggio - Como, 13 - 18 September 2004

The idea:

Integration of the pixel detector and readout electronics in the wafer-bonded SOI substrate

Electronics → Device layer

- Low resistive ($9-13 \Omega\text{cm}$, CZ)
- $1.5 \mu\text{m}$ thick
- Standard CMOS technology

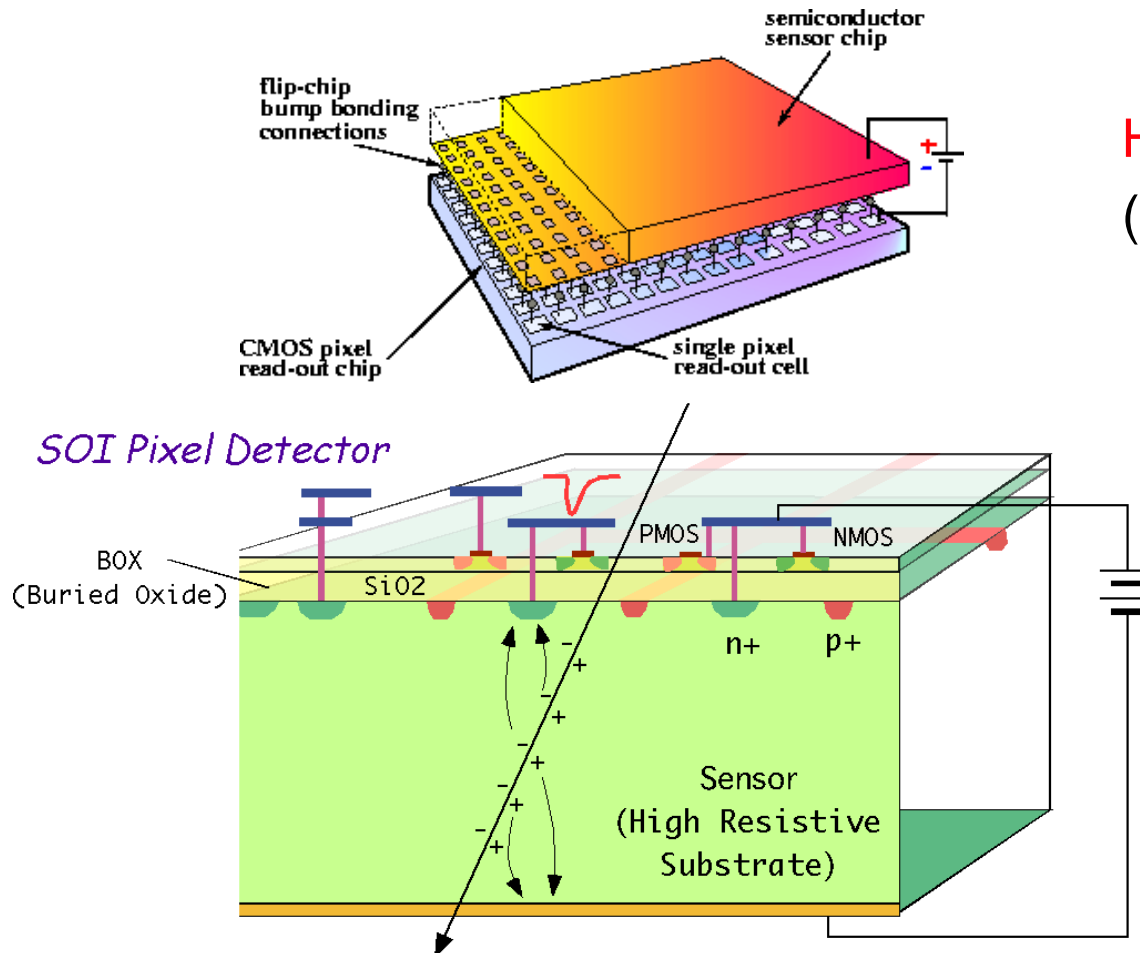
Detector → Support layer

- High resistive ($> 4 \text{ k}\Omega\text{cm}$, FZ)
- $300 \mu\text{m}$ thick
- Conventional p⁺-n
- DC-coupled

*Processed in Lab. with $\sim 3\mu\text{m}$ technology.
Ended at 2004?*

2. SOI Pixel Development at KEK

Last spring, New Detector R&D projects were called at KEK, and we proposed Development of SOI (Silicon-On-Insulator) Pixel Detector. Main members consist of Belle and ATLAS silicon detector group.



Hybrid Pixel Detector
(need many bump bondings)



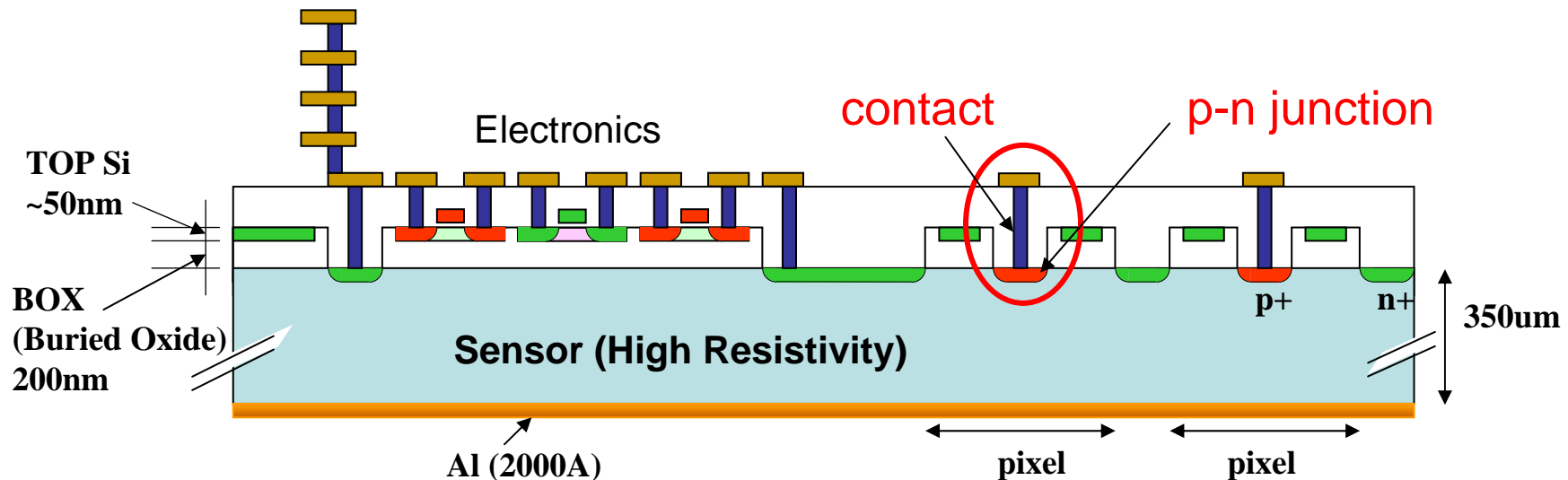
SOI Pixel Detector
Monolithic Detector with
Sensor(Hi-R) and
Electronics(Low-R)

Feature of Our SOI Pixel Detector

- Using Commercial 0.15 μm FD-SOI process (OKI Elec. Ind.).
- SOI Wafer (SOITEC Hi-R, 150 mm ϕ)
Top Si : Cz, $\sim 18 \Omega\text{-cm}$, p-type, 50 nm thick
Buried Oxide: 200 nm thick
Handle wafer: Cz, Hi-R $> 1\text{k} \Omega\text{-cm}$ (*No type assignment by supplier*), 650 μm thick (thinned after process $< 350\mu\text{m}$)
- Multi Project Wafer (Masks are shared with other design)
+ additional process step.
- Add only 3 mask layers to create sensor (p+, n+, and contact to substrate).
- Back side is plated with Al (200 nm).

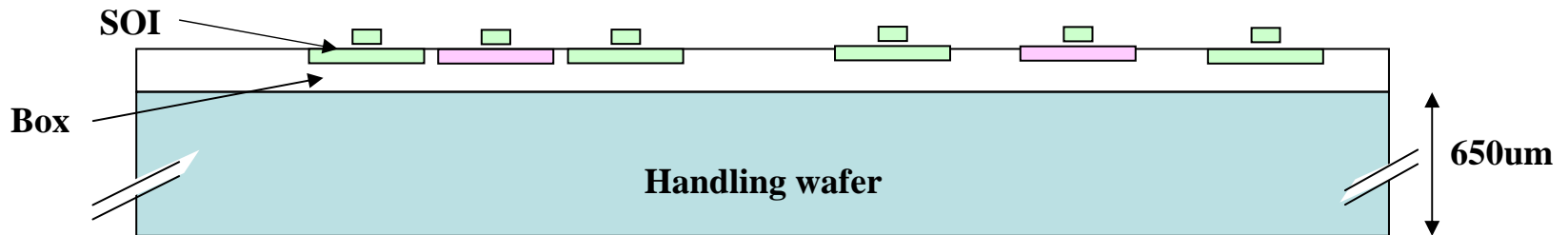
History

- '05. 6: OKI agreed on SOIPIX development with us.
- '05.10: 3 x 2 (for p/n substrate) + 3 chips (total 9 chips) submitted.
(32x32 small pixel, 4x4 large pixel, Short strip, Tr TEG ...)
- '05.12: Test of contact fabrication.
- '06. 2: Test of p-n junction fabrication.
- '06.3 middle : Process ends.
- '06.3.30 Bare Chip Delivered.
(-> so the present results are very preliminary and limited)

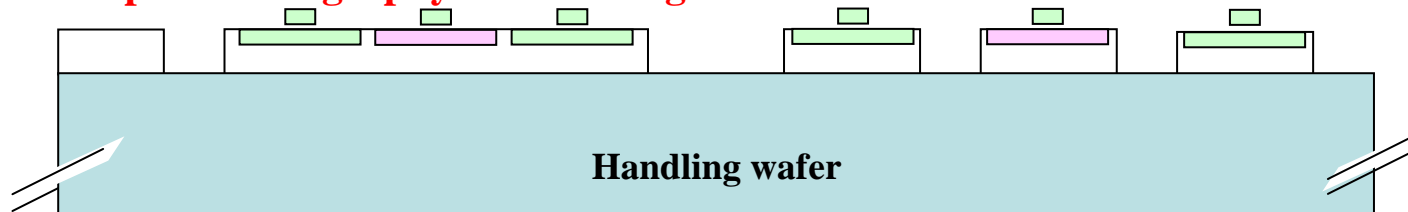


SOI Pixel Process step flow

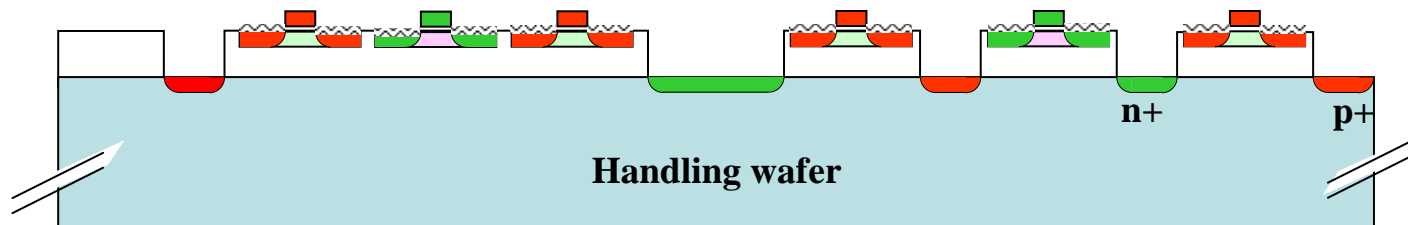
① After Gate stack formation



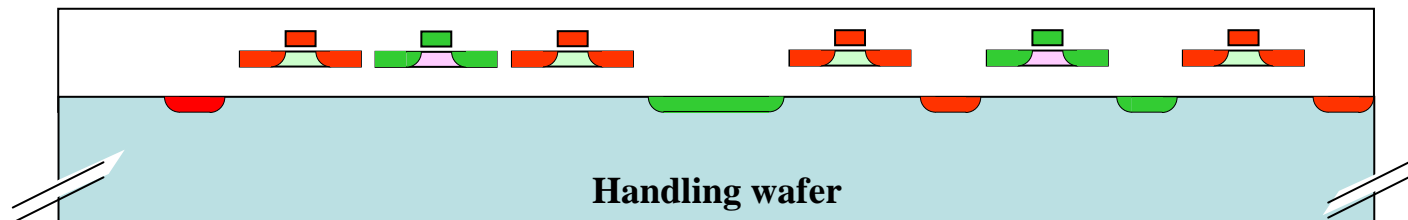
② Box Window photo lithography and etching



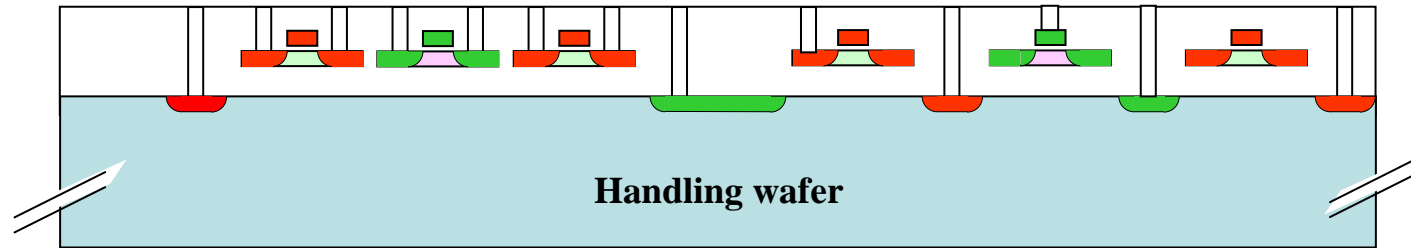
③ Source/Drain Implantation followed by S/D annealing and Salicidation



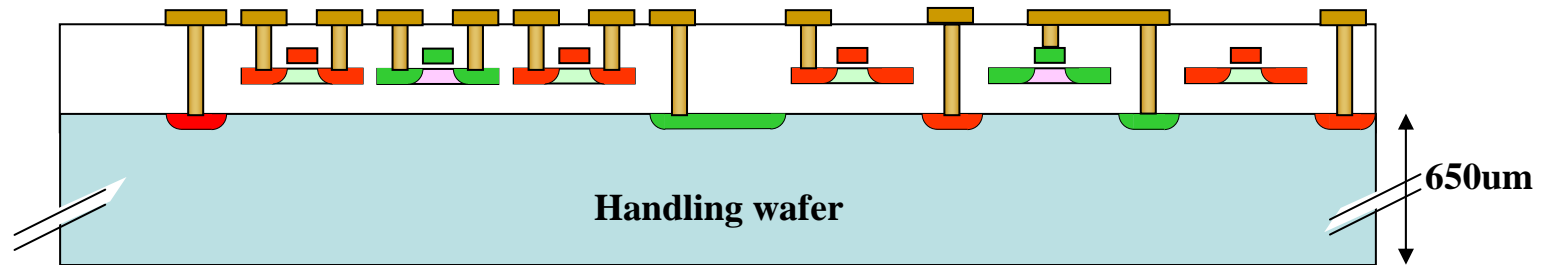
④ 1st ILD (interlayer dielectrics) filling and CMP planarization



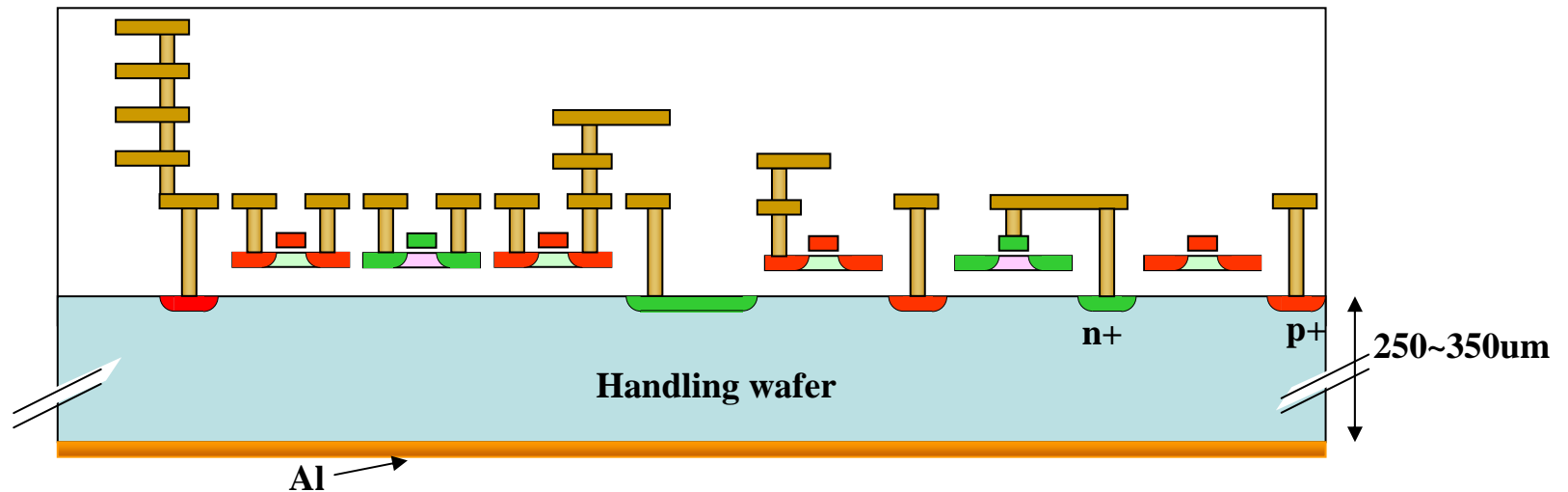
⑤ Contact etching



⑥ Contact plug filling and 1st Metal formation

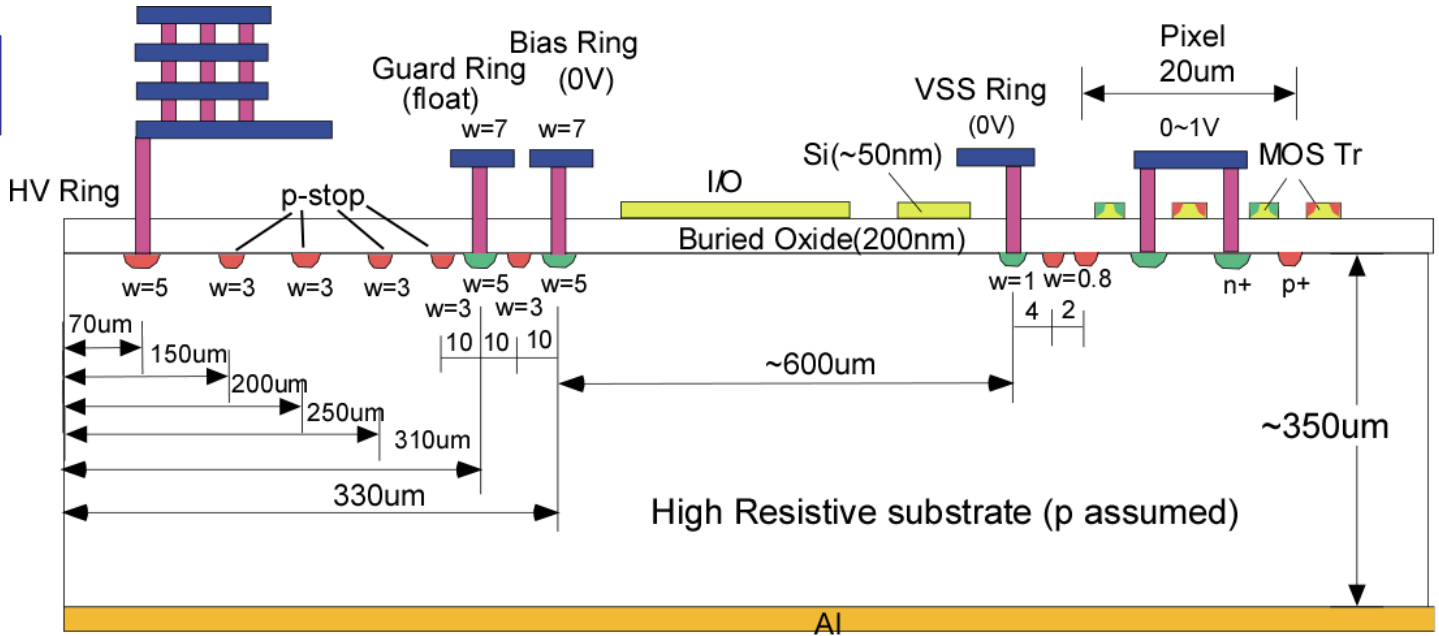


⑦ 3 ~ 5 Metal formation followed by Backside polishing and Al coating



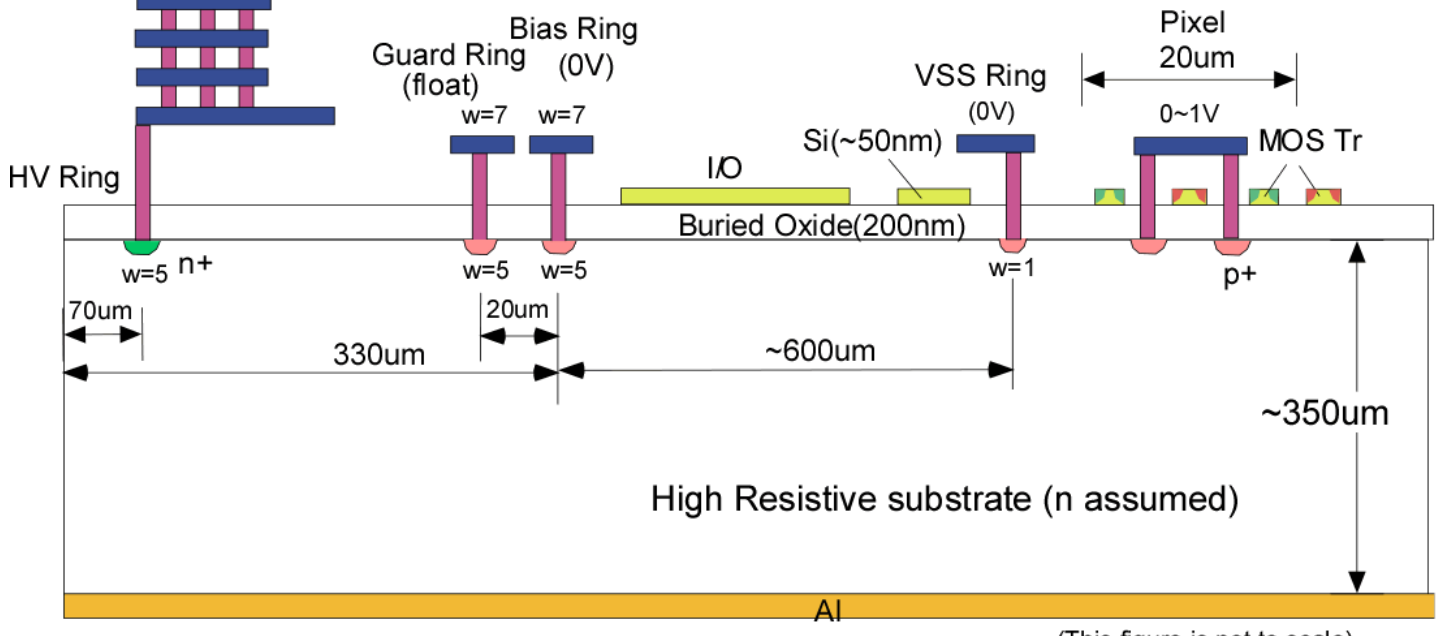
Side View

n+ on p--



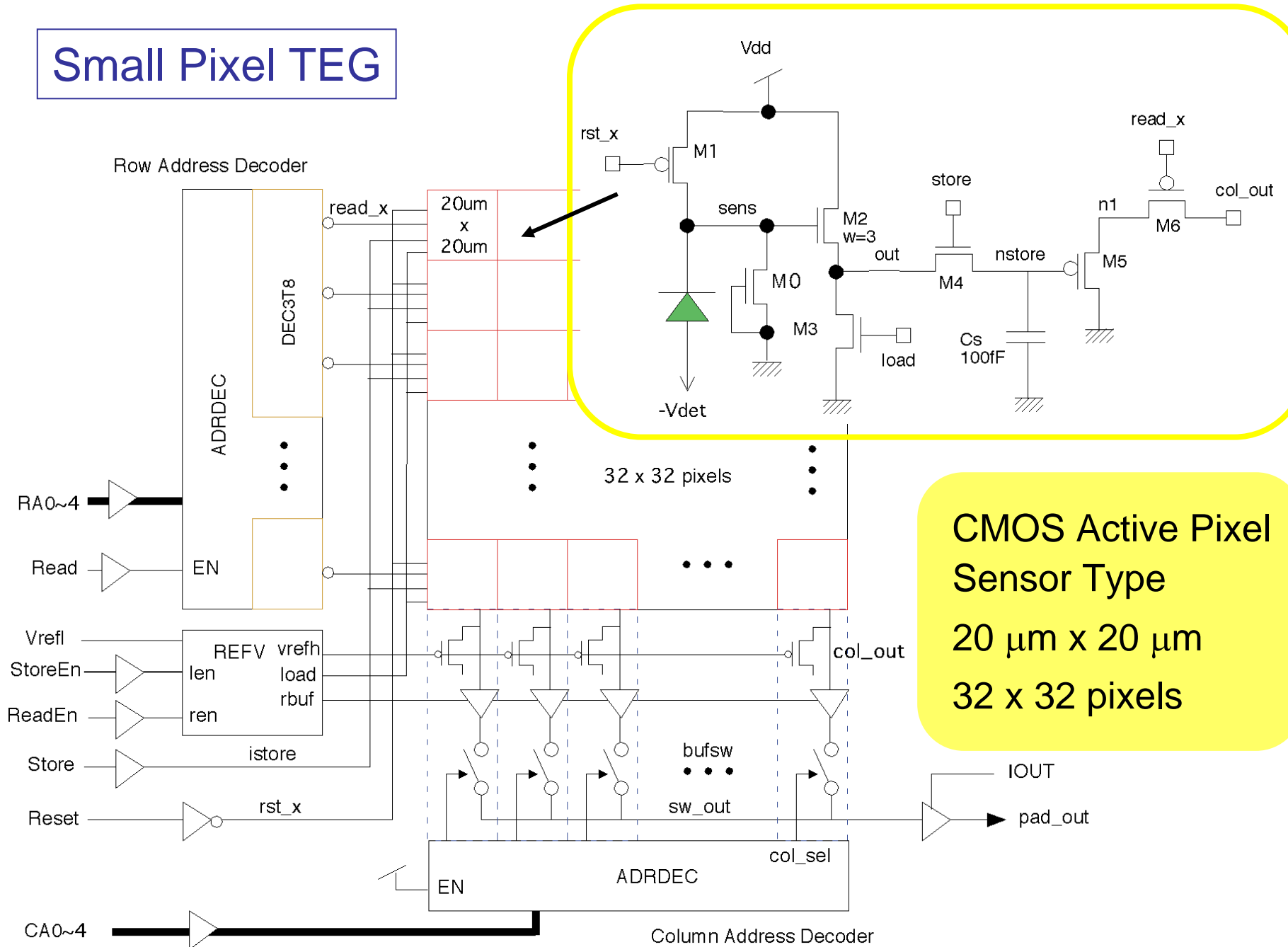
(This figure is not to scale)

p+ on n--



(This figure is not to scale)

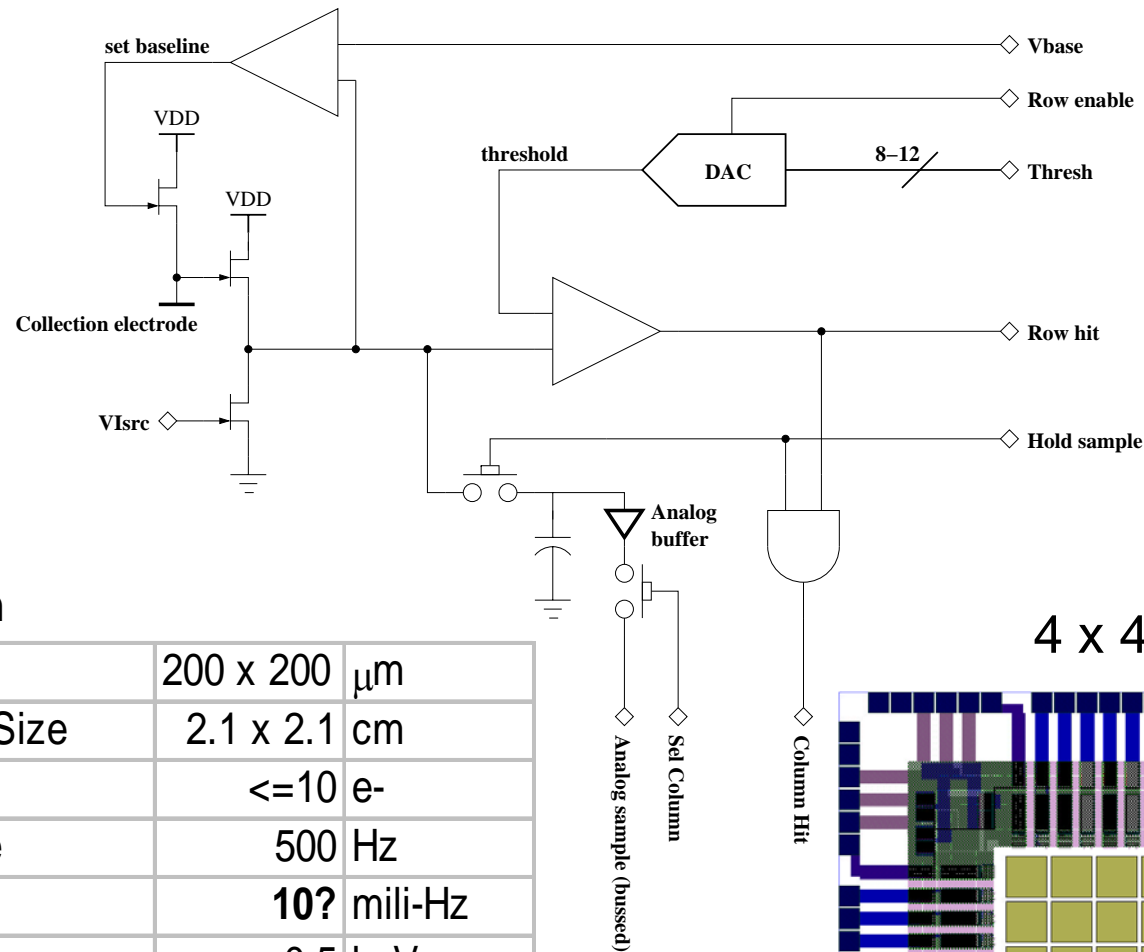
Small Pixel TEG



**CMOS Active Pixel
Sensor Type**
20 μm x 20 μm
32 x 32 pixels

IHXCP (Imaging Hard X-Ray Compton Polarimeter) TEG

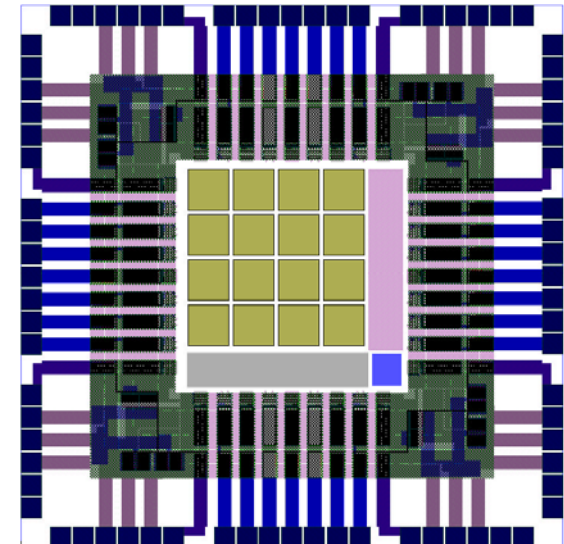
U of Hawaii &
SLAC



Target Specification

Pixel Size	200 x 200 μm
Pixel Array (Detector) Size	2.1 x 2.1 cm
Noise	≤ 10 e-
Global Trigger Rate	500 Hz
Single Pixel Rate	10? mili-Hz
Trigger Threshold	0.5 keV
Trigger Latency	1-2 μs
Power	200 $\mu\text{W}/\text{pixel}$
ADC precision	12 bits

4 x 4 pixels



3. Specific Issues on SOI Pixel

- **n+, p+ implant**

 - Formed with Tr Source/Drain not to increase number of masks.

- **Thinning**

 - Wafer is thinned from 650um to 350um. Further thinning is possible.

- **Back Side process**

 - No implant on back side. Just add Al (2000 Å) Plating.

- **Thermal Donor generation**

 - Type of the high-R wafer may change by TD generation during process.

 - We prepared both p & n substrate designs.

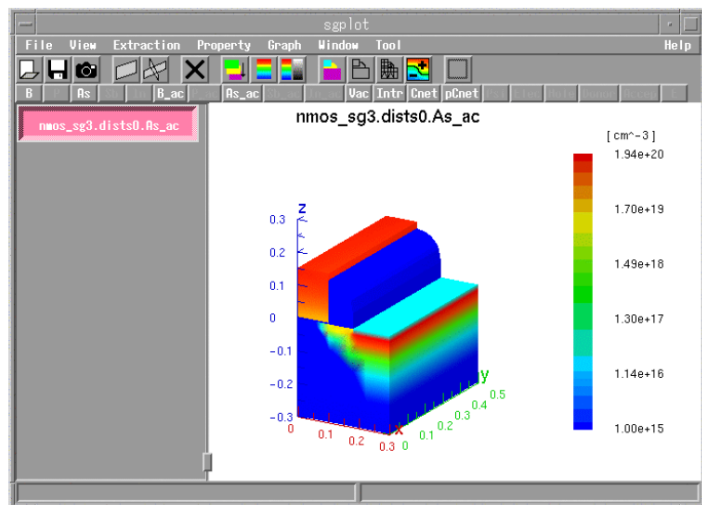
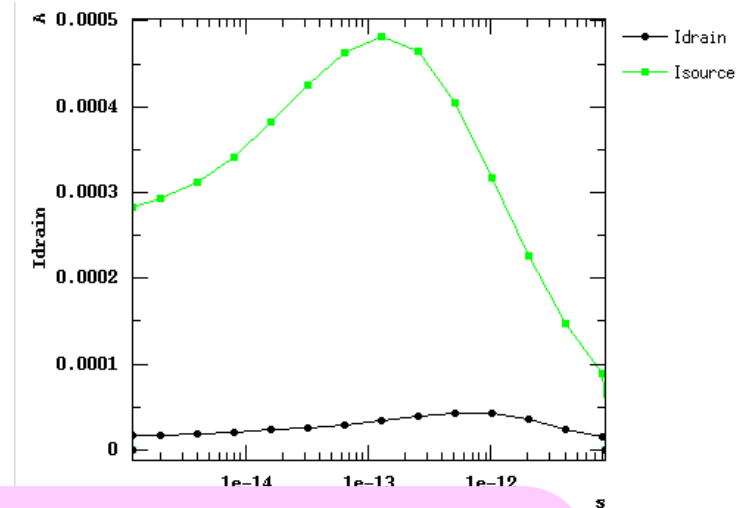
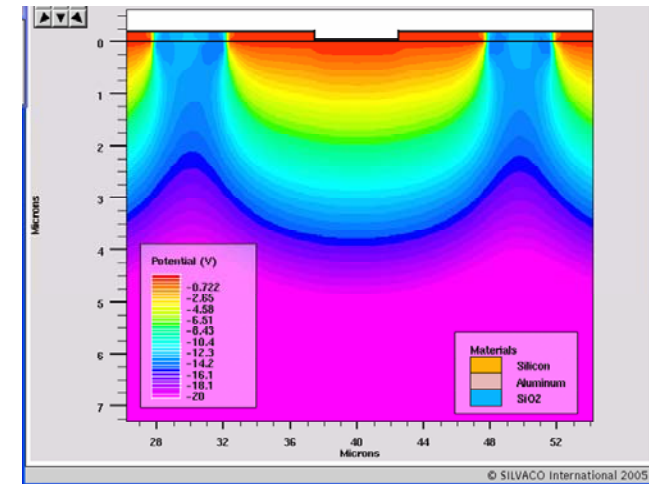
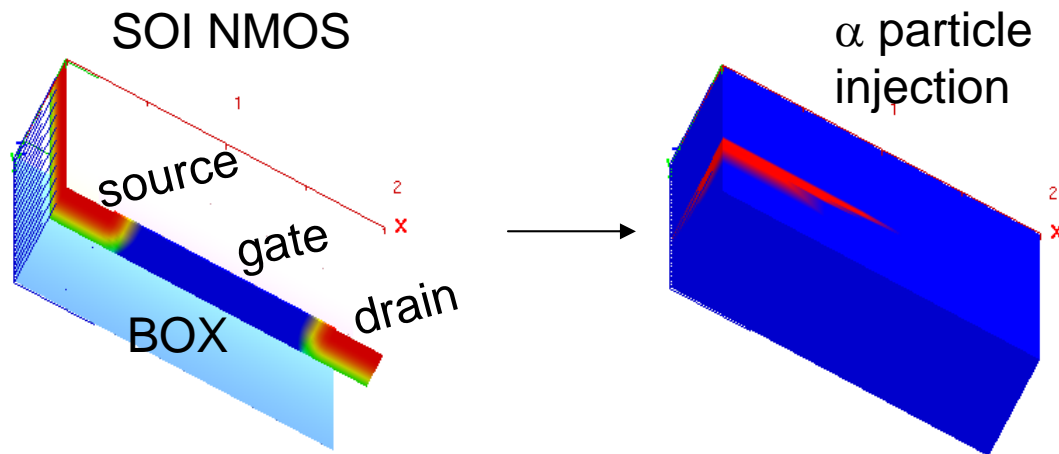
- **Back Gate Effect to SOI Tr**

 - Substrate works as back gate, so the voltage must be low under Tr.**

 - All Tr are placed within Guard Ring, and body is tied to VDD/VSS.

3D Process/Device Simulator ENEXSS

- Developed by SELETE (Japan Consortium) (<http://www.selete.co.jp/>)
- Full 3D simulation

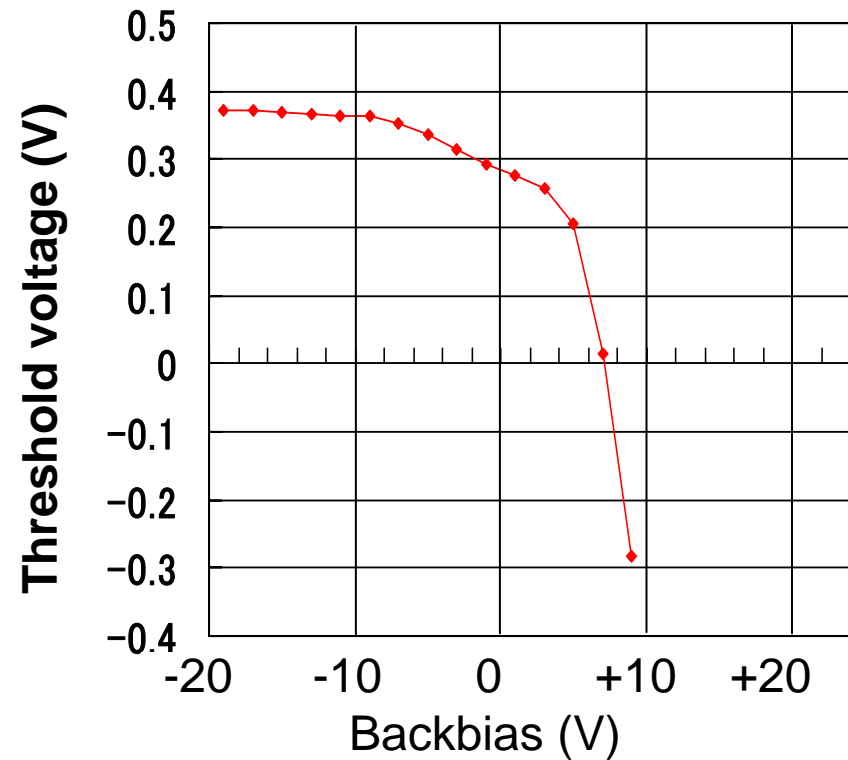
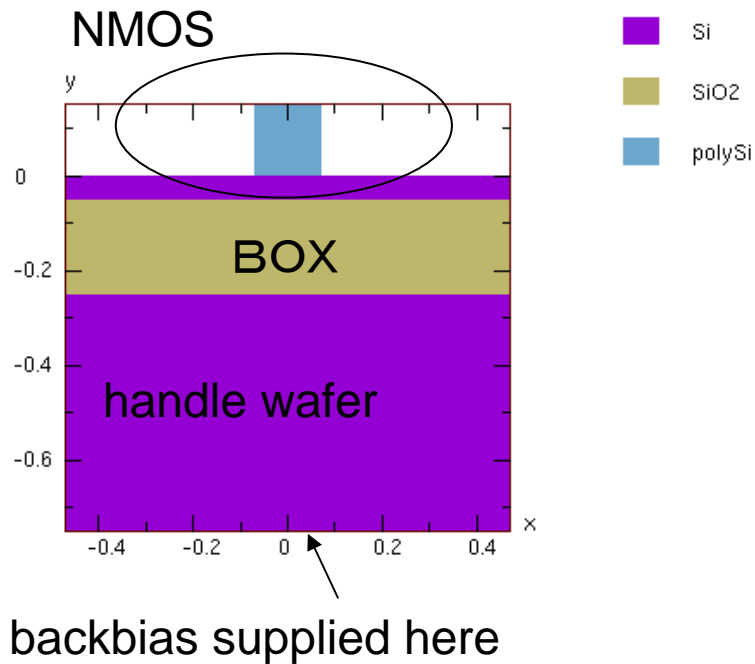


Useful to get

- Field Map
- Device Characteristics
- Signal generated by particle, etc.

Back Bias Simulation

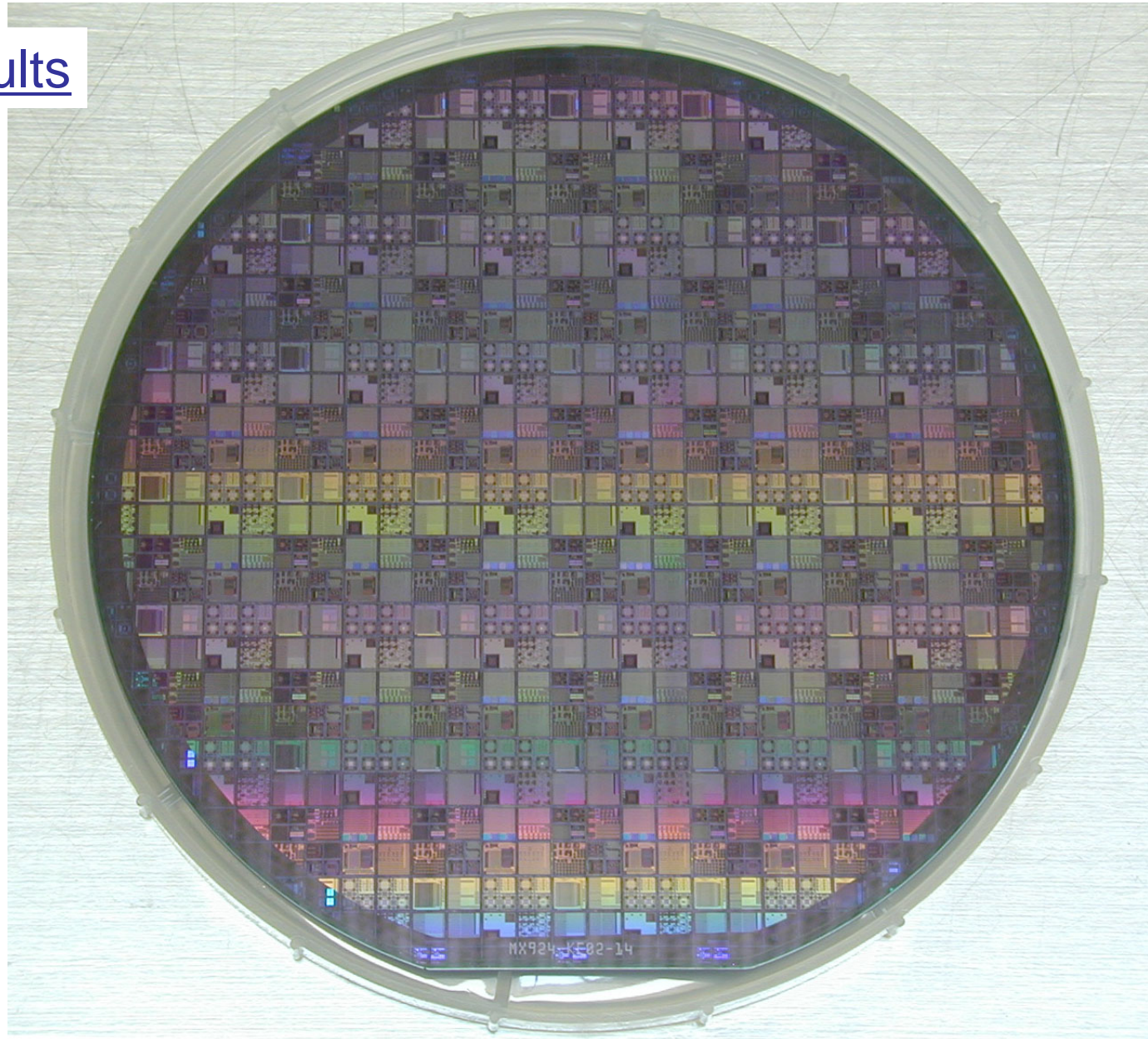
TCAD: ENEXSS



With $|\text{back bias}| > 8\text{V}$, NMOS or PMOS become always ON.
Voltage of substrate under Tr must be kept low.

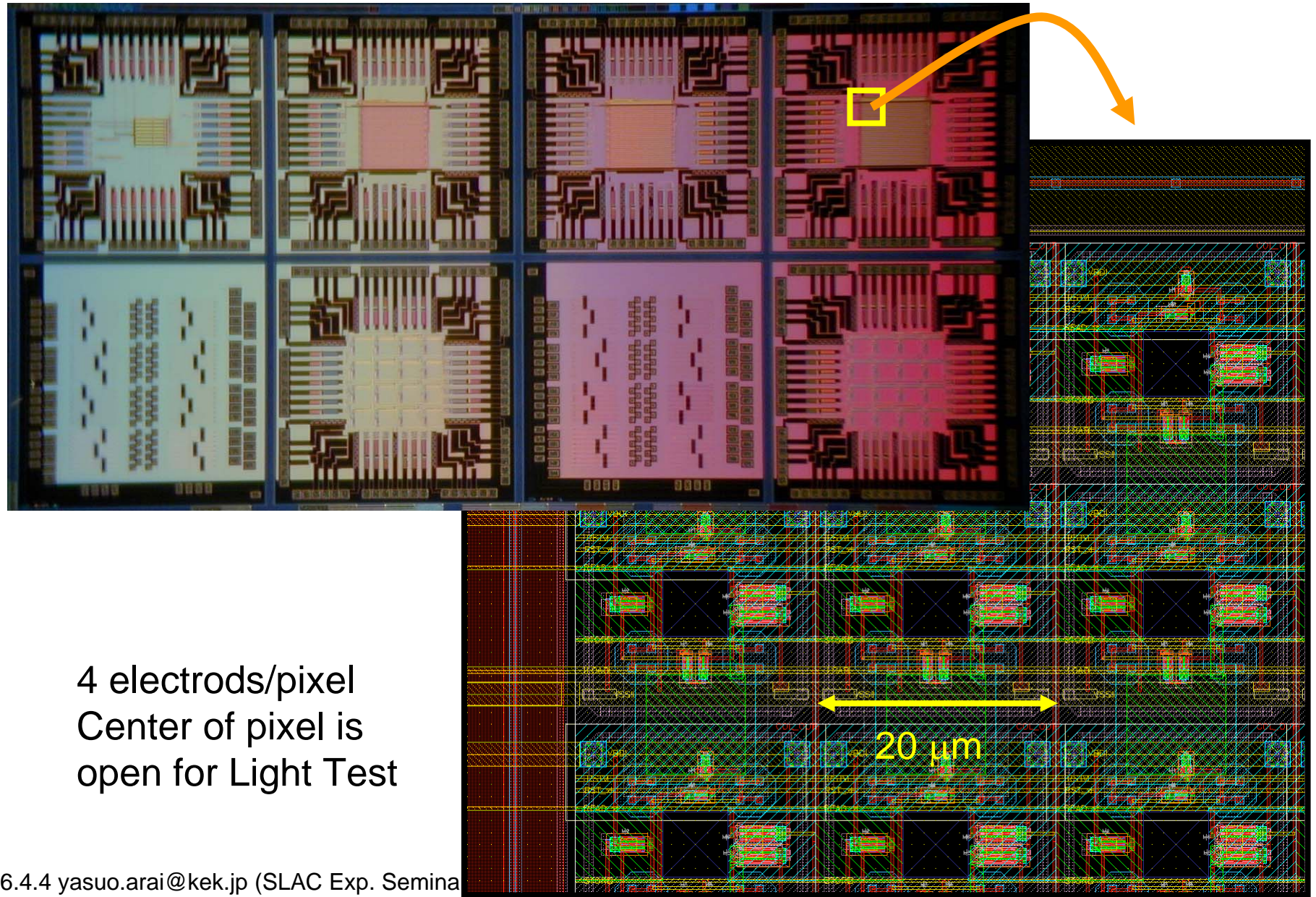
4. Test Results

MPW Wafer
6 inch ϕ



← 2.5 mm →

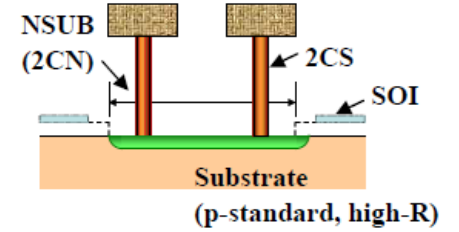
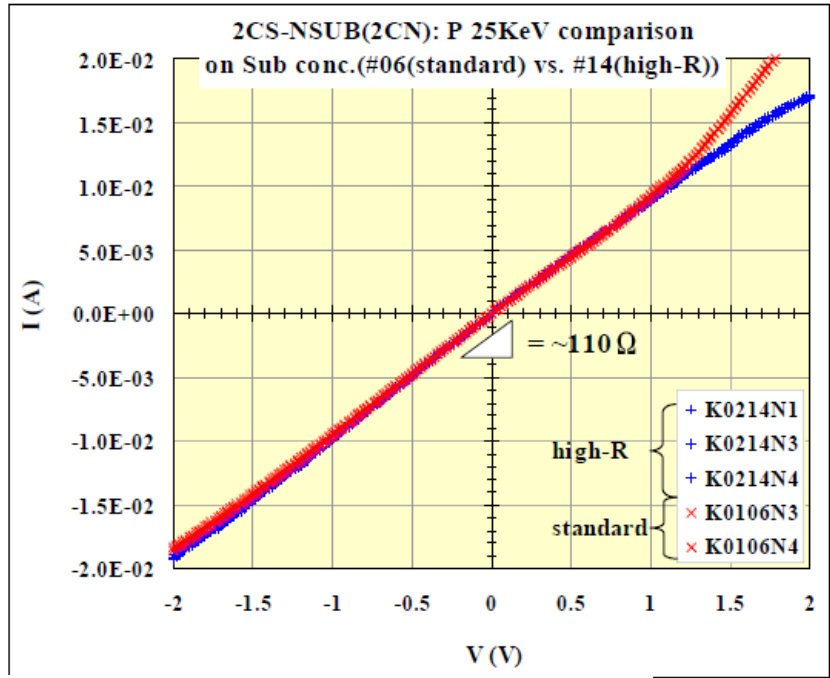
TEG Chip Layout



4 electrodes/pixel
Center of pixel is
open for Light Test

n+ contact

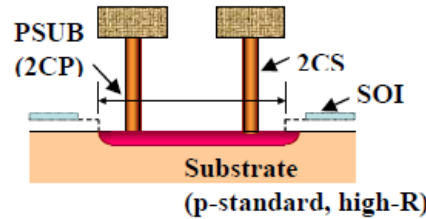
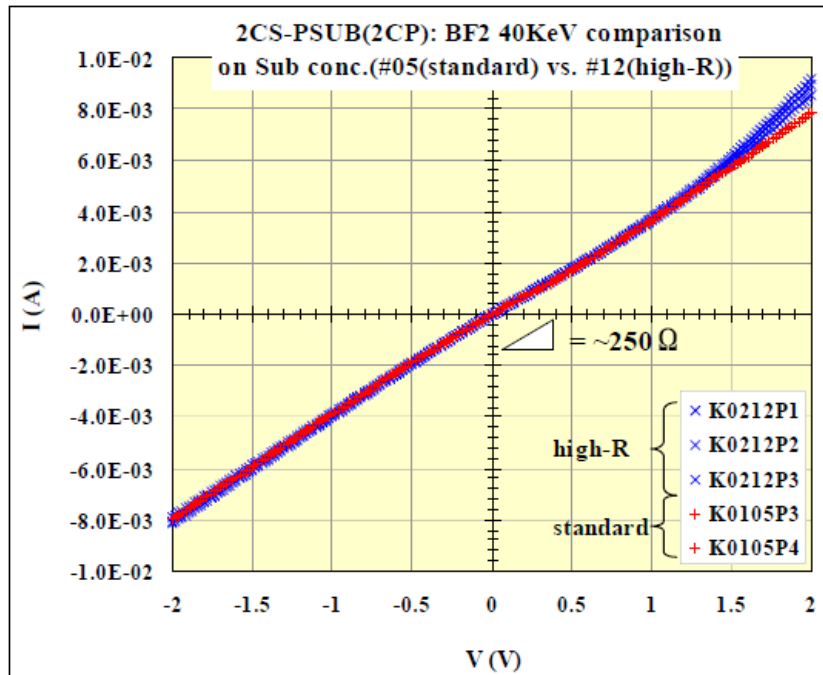
Contact & Sheet Resistance



Hi-R ($> 1k \Omega\text{cm}$)

Std. wafer (p+, $\sim 13 \Omega\text{cm}$)

p+ contact



Hi-R ($> 1k \Omega\text{cm}$)

Std. wafer (p+, $\sim 13 \Omega\text{cm}$)

[Sheet R]

n+ : $33 \Omega/\text{square}$

p+ : $136 \Omega/\text{square}$

[Contact]

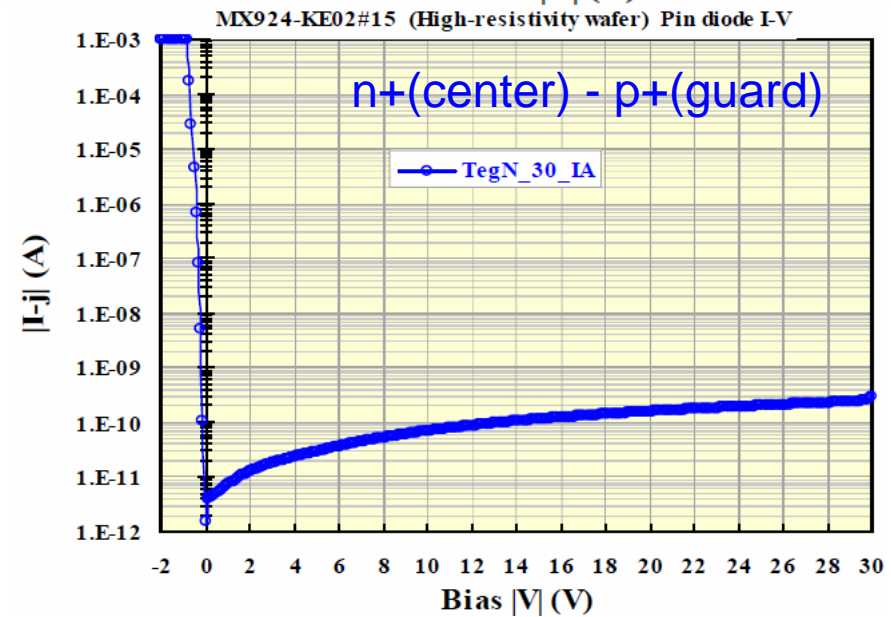
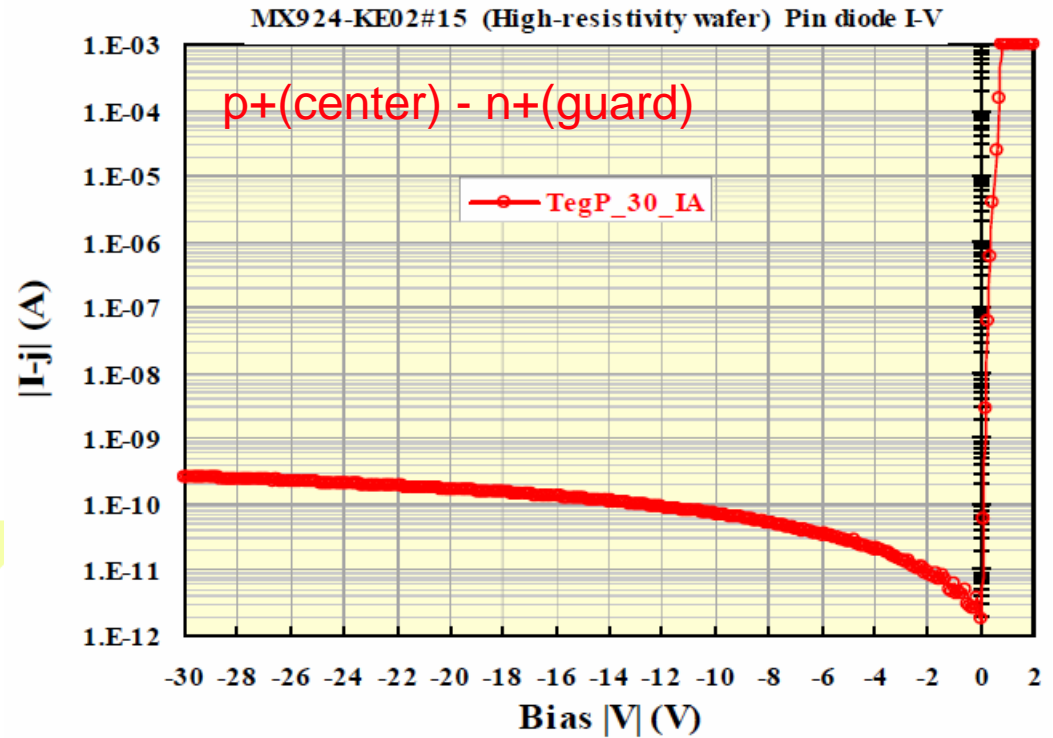
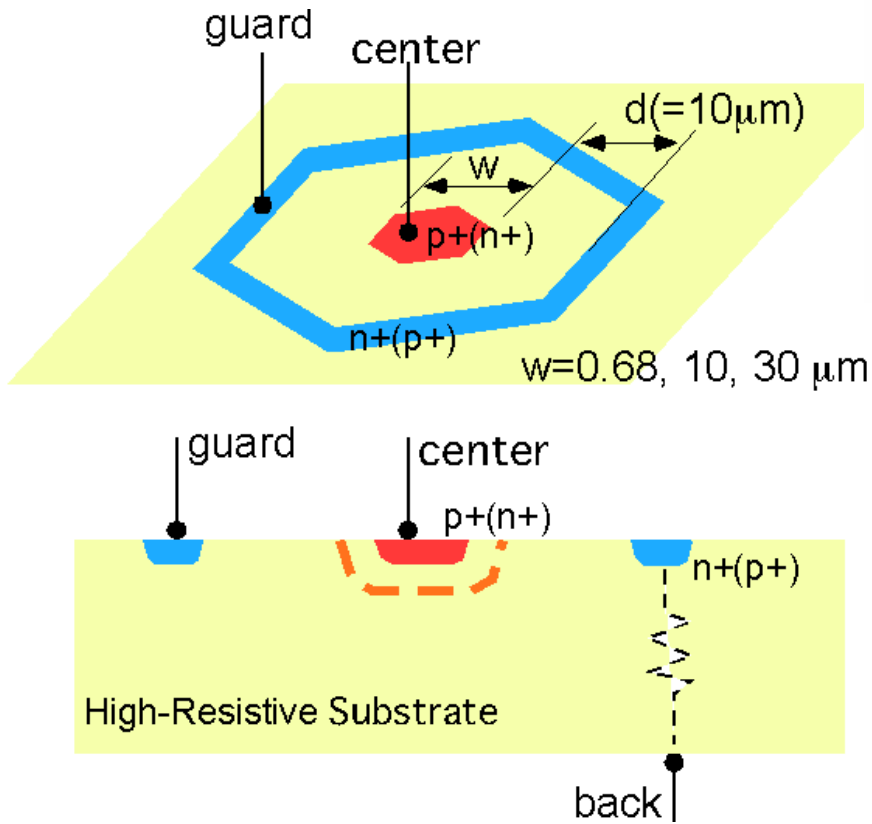
($0.16 \times 0.16 \mu\text{m}^2$)

n+ : 87Ω

p+ : 218Ω

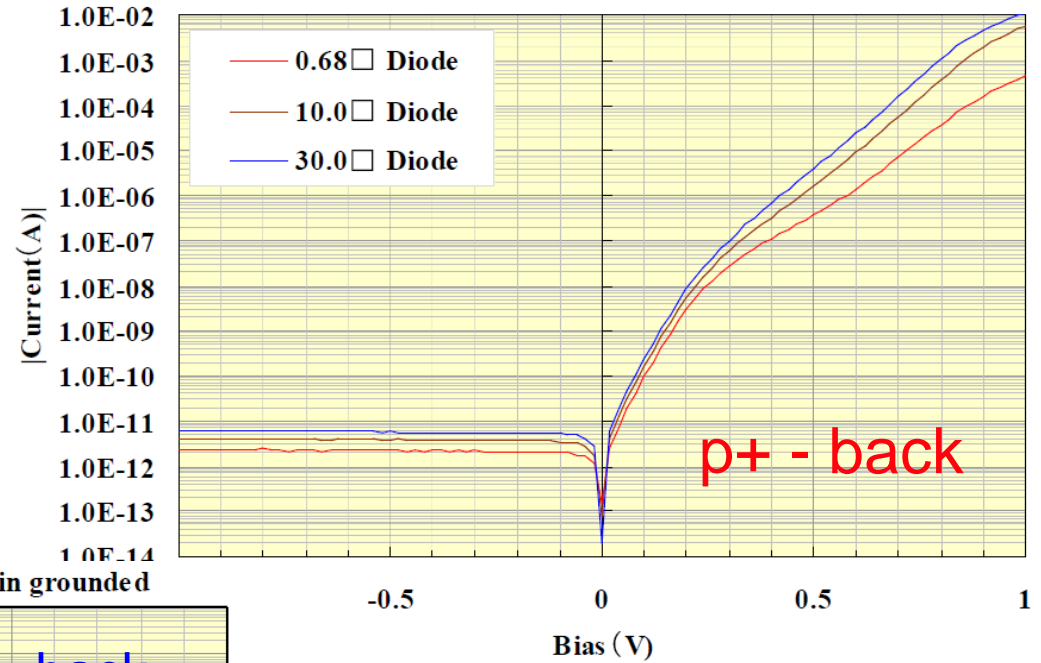
p-n junction I-V characteristics

p+(center) - n+ (guard) &
n+(center) - p+(guard)

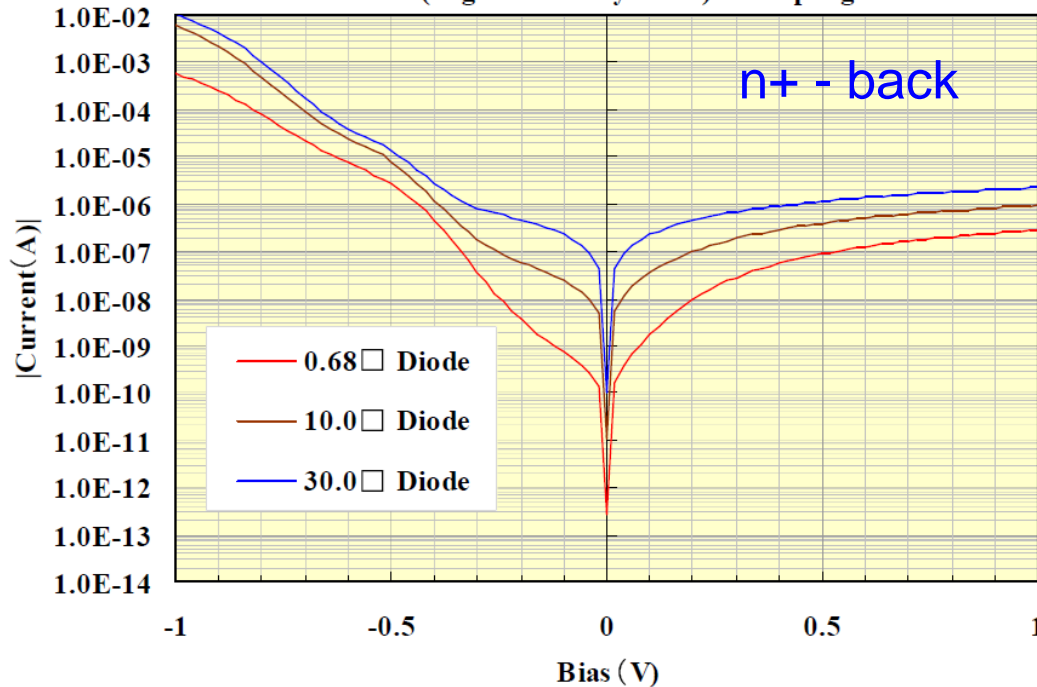


n+ / p+ --- back
I-V characteristics

MX925 KE-02#14 (High resistivity wafer) Back pin grounded



MX925 KE-02#14 (High resistivity wafer) Back pin grounded



n+(center) – back is Ohmic
→ Substrate is n-type

Substrate Resistivity

[before process]

No type assign, $> 1 \text{ k}\Omega\text{cm}$



[after process] (4-points measurement)

n-type, $\rho \sim 700 \text{ }\Omega\text{cm}$ ($\rightarrow N_B \sim 6 \times 10^{12} \text{ cm}^{-3}$)

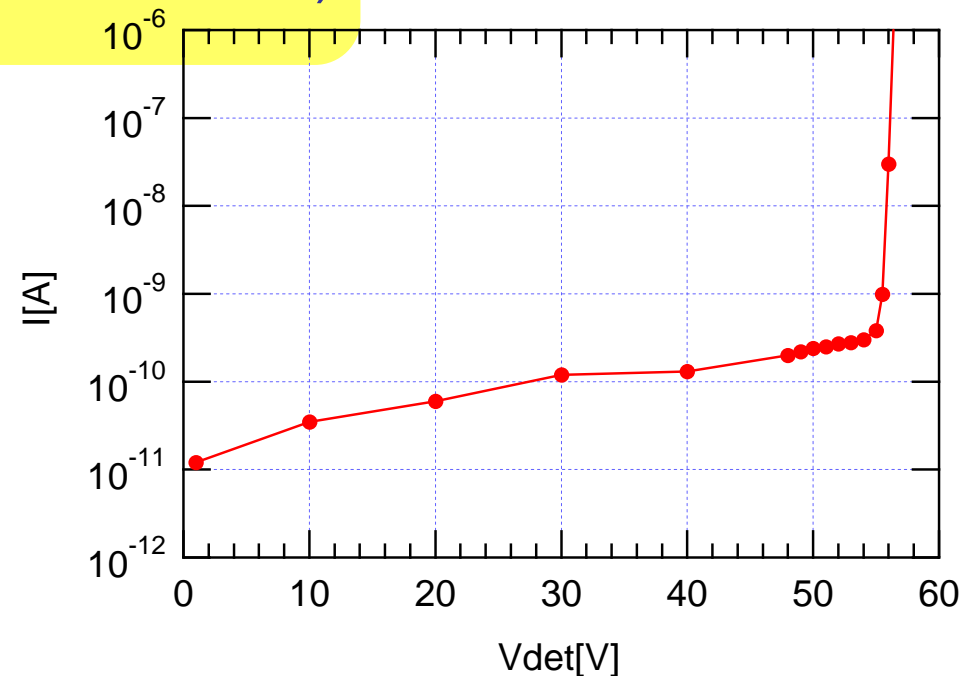
I-V Characteristic

10 μm x 460 μm strip

$I < 1 \text{ nA}$ @ $V = 56 \text{ V}$

Depletion $\sim 100 \text{ }\mu\text{m}$?

Very Preliminary!



5. Summary

- We have started development of Monolithic SOI Pixel Detector.
- The detector has sensor in high-resistive Si and CMOS circuit in low-resistive Si.
- We are using commercial (OKI 0.15 μm SOI) process with commercial wafer (SOITEC Hi-R) with only adding 3 masks.
- 3-D TCAD simulations for sensor/device study are being done with ENEXSS.
- Good substrate contact and p-n junction are confirmed with the first run wafer.
- We found type of handle wafer is 'n', and have enough resistivity.
- 9 kinds of TEG chips are received at the end of March, and showing promising results. Detailed tests will be done soon.
- We would like to apply this technique to Super-B, SLHC, ILC and X-ray detectors.