Total Dose Effects for 0.15μm FD-SOI CMOS Transistors

Y. Ikegami[1], Y. Arai[1], K. Hara[2], M. Hazumi[1], H. Ikeda[3], H. Ishino[4], T. Kohriki[1], H. Miyake[2], A. Mochizuki[2], S. Terada[1], T. Tsuboyama[1], Y. Unno[1]

[1]IPNS, KEK, Tsukuba, Ibaraki, Japan
[2]Inst. for Pure and Applied Sciences, University of Tsukuba, Tsukuba, Ibaraki, Japan
[3]ISAS, JAXA, Kanagawa, Japan
[4]Department of Physics, Tokyo Institute of Technology, Tokyo, Japan

Motivation

- The silicon-on-insulator (SOI) CMOS technology has a number of advantages over the standard bulk CMOS technology, such as no latch-up effect, high speed and low power dissipation.
- A monolithic pixel detector featuring of these advantages is being developed under KEK Detector Technology Project.
- The fully depleted SOI (FD-SOI) CMOS technology provided by OKI Electric Industry Co., Ltd. is realizing the full features of the advantages.
- High radiation tolerance is expected, since the devices are fabricated using a very thin silicon layer.
- We investigated the total dose effects for transistors fabricated using the OKI 0.15μm FD-SOI CMOS process.

OKI 0.15μm FD-SOI Transistor parameters

	Vth	Gate Oxide Thickness	Voltage Tolerance
Low VT (LVT) For analog	~ 0.2V	2.5nm	<1V
High VT (HVT) For logic	~ 0.4V	2.5nm	<1V
IO For I/O	~ 0.5V	5.0nm	<1.5V

Buried Oxide: 200 nm thick
Handle wafer: 650 μm thick (SOITEC)
Backside Thinned to 350 μm, and plated with Al (200 nm)
Body Control : floating body and body tie
Body is connected with source in the body tie transistor.

Transistor TEG

	L/W= 0.14/280	L/W= 0.2/400	L/W= 0.3/600	L/W= 0.5/1000
Low VT	Floating + Body Tie	Body Tie	Floating + Body Tie	Body Tie
High VT	Floating + Body Tie	Body Tie	Floating + Body Tie	Body Tie
IO			Floating + Body Tie	Floating + Body Tie

16 NMOS and 16 PMOS transistors
W/L ratio is fixed to 2000.
Sources were connected together in the TEG.
Gates were connected together and
Drains are selected by relays on a test PC board.

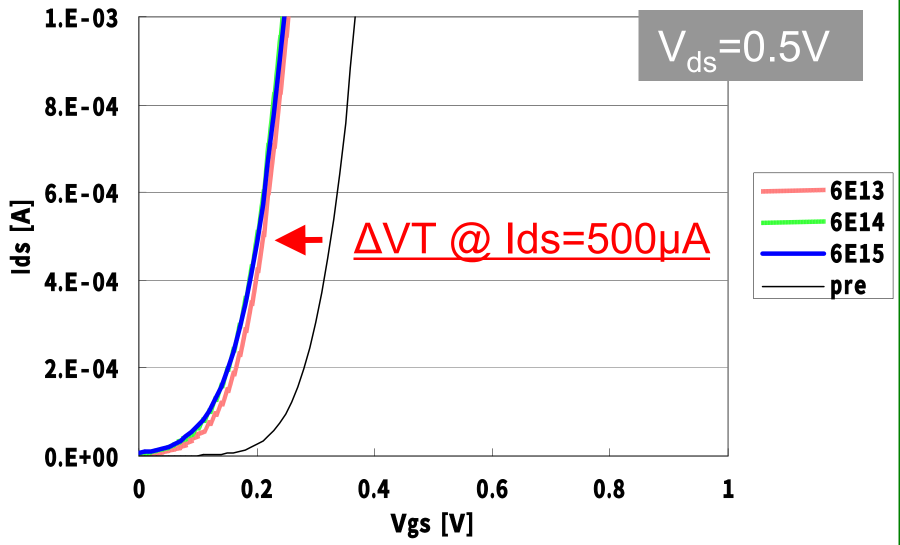
Irradiation

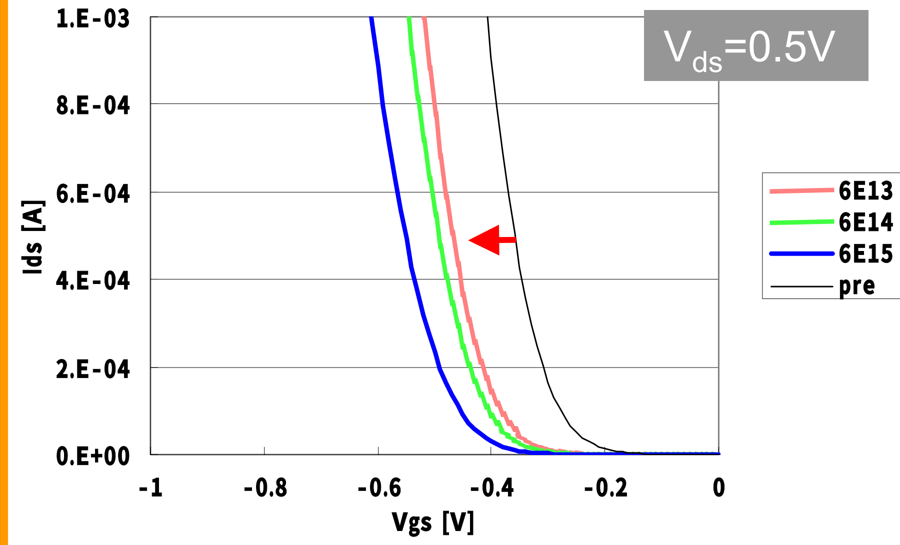
- Tohoku Univ. Cyclotron and Radioisotpoe Center (CYRIC)
- 70 MeV proton
- Beam profile x~15mm y~16mm
- Al Collimator Φ10mm x 30mm (length)
- Scan 15mm x 15mm (TrTEG size :5mm x 5mm)
- The fluence was calculated later by measuring the Na24 product from the Al foil attached toeach TEG chip.
- All terminals were shorted using conductive sponge.

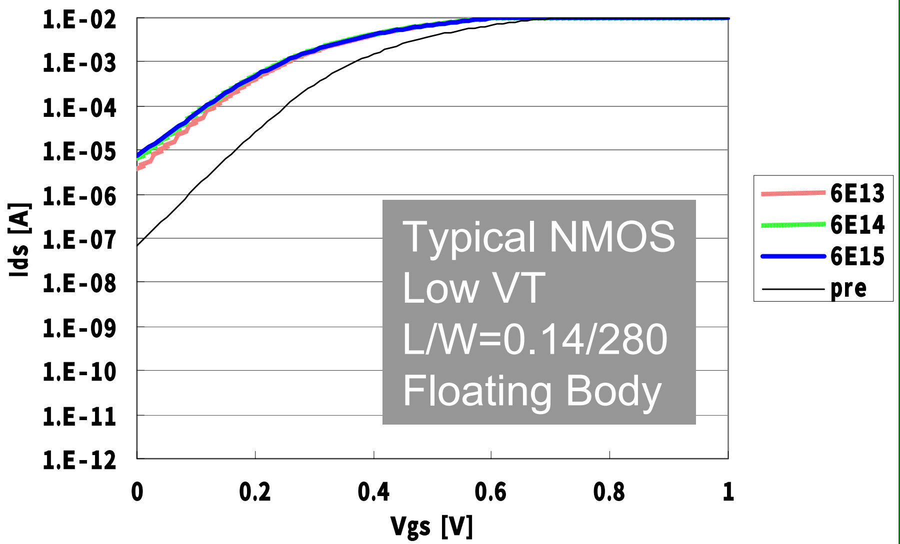
Expected 1MeV n-eq /cm^2	proton current [nA]	Irradiation time [min.]	Measured proton /cm^2	Measured 1MeV n-eq /cm^2	Ionization dose to SiO_2	# of chips
10^{14}	20	21	4.5×10^{13}	6.4×10^{13}	54 K Gy	1 chip
10^{15}	200	21	4.0×10^{14}	5.8×10^{14}	0.49 M Gy	1 chip
10^{16}	400	105	3.8×10^{15}	5.5×10^{15}	4.7M Gy	1 chip

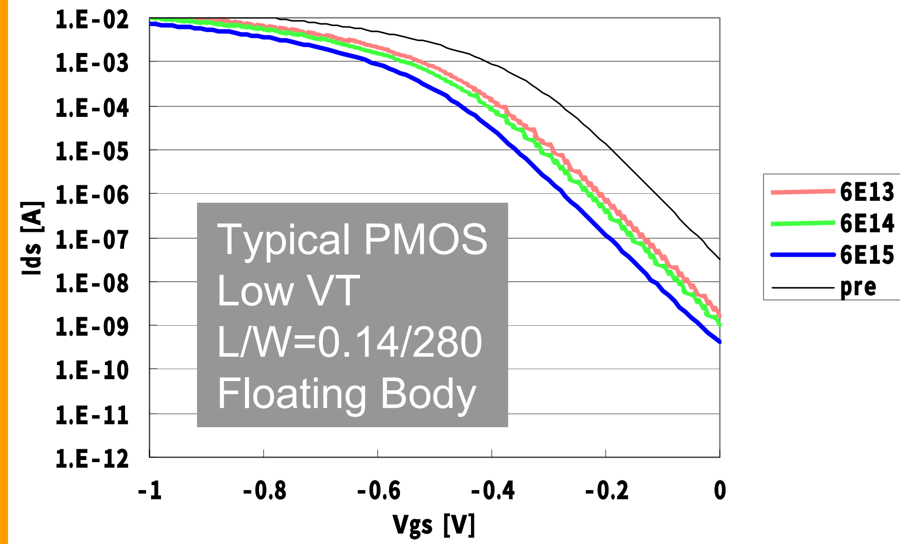
Total 3 TrTEG s

I_{ds}-V_{gs} Characteristics

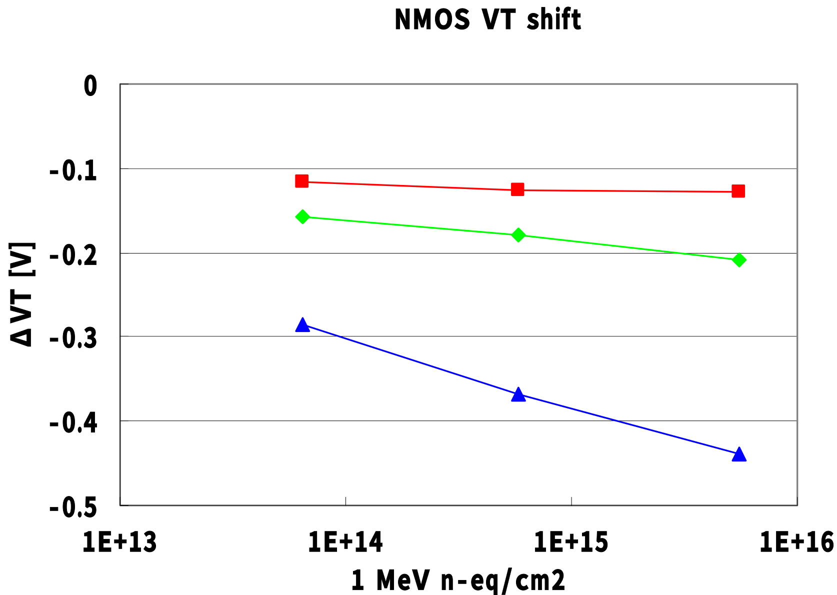


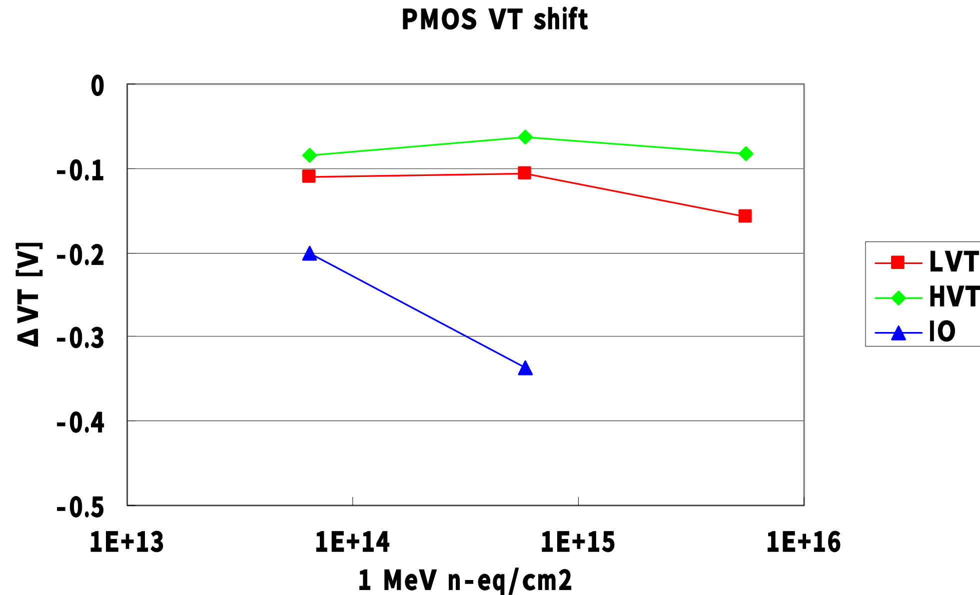






VT shift (Dose dependence)





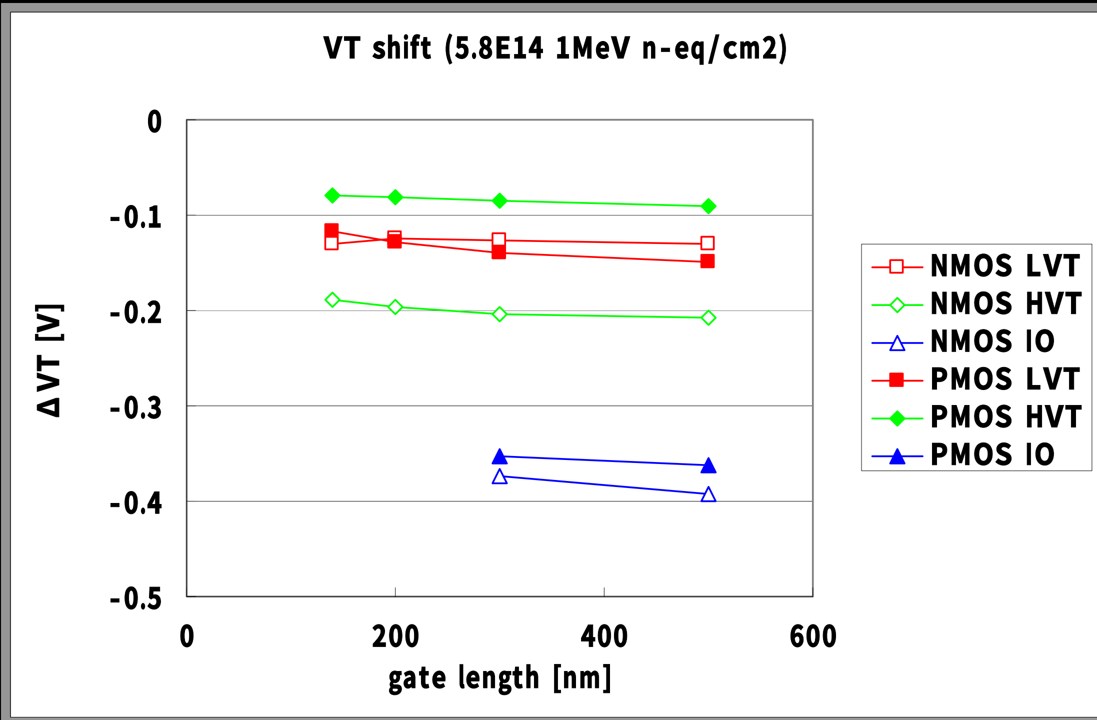
L/W = 0.14/280 for LVT, HVT
= 0.30/600 for IO
Body : Floating

A voltage reference is defined by V_{gs}, where I_{ds}=500μA.

ΔVT=V_{gs} after irradiation – V_{gs} before irradiation

ΔVT	=	-0.13 ~ -0.12 V	for NMOS LVT
	=	-0.21 ~ -0.16 V	for NMOS HVT
	=	-0.44 ~ -0.29 V	for NMOS IO
	=	-0.16 ~ -0.11 V	for PMOS LVT
	=	-0.08 ~ -0.06 V	for PMOS HVT
	=	< -0.5 ~ -0.20 V	for PMOS IO

VT shift (gate length dependence)



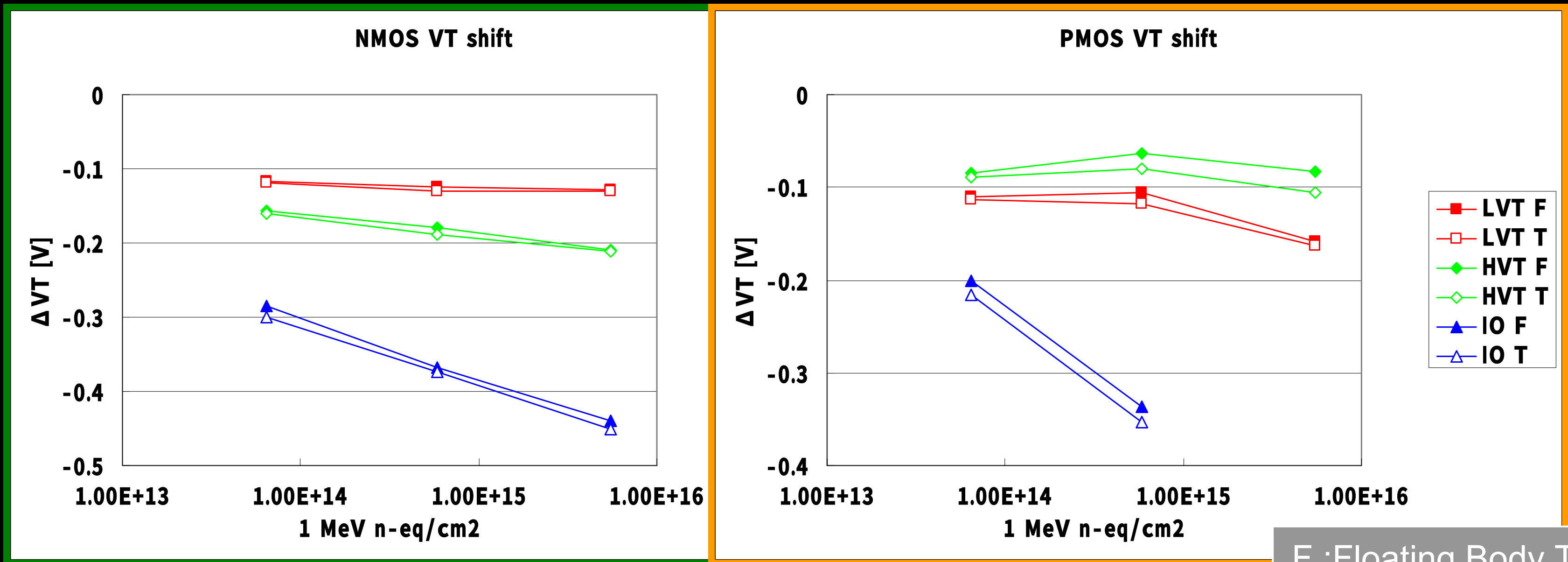
VT shifts slightly increased as gate lengths became longer, except LVT NMOS.

Table shows
ΔVTmax – ΔVTmin
with different gate lengths.

Dose [1MeV n-eq/cm^2]	NMOS LVT	NMOS HVT	NMOS IO	PMOS LVT	PMOS HVT	PMOS IO
6.4×10^{13}	18	28	21	32	12	10
5.8×10^{14}	5	19	20	32	12	10
5.5×10^{15}	35	25	18	18	16	

Unit [mV]

VT shift (Body Tie effect)



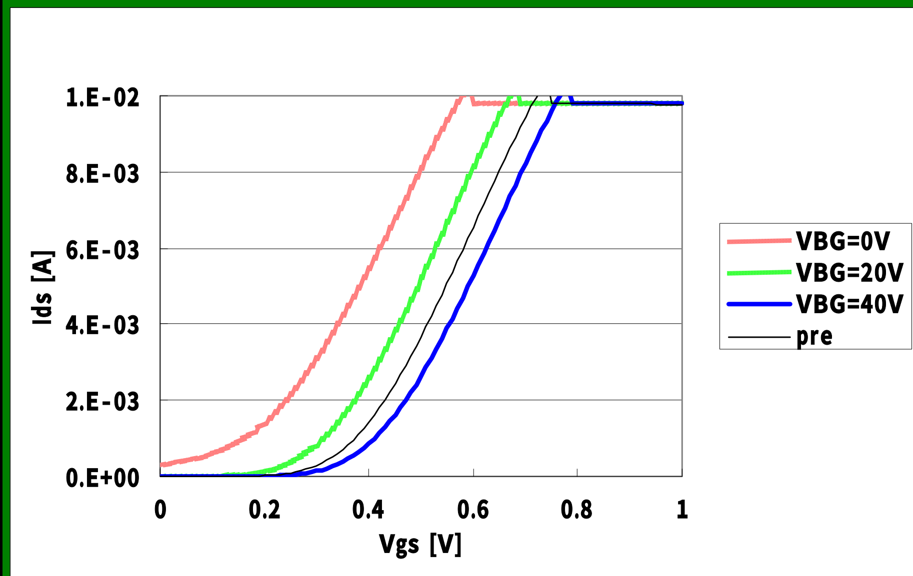
F :Floating Body Tr.
e Tr.

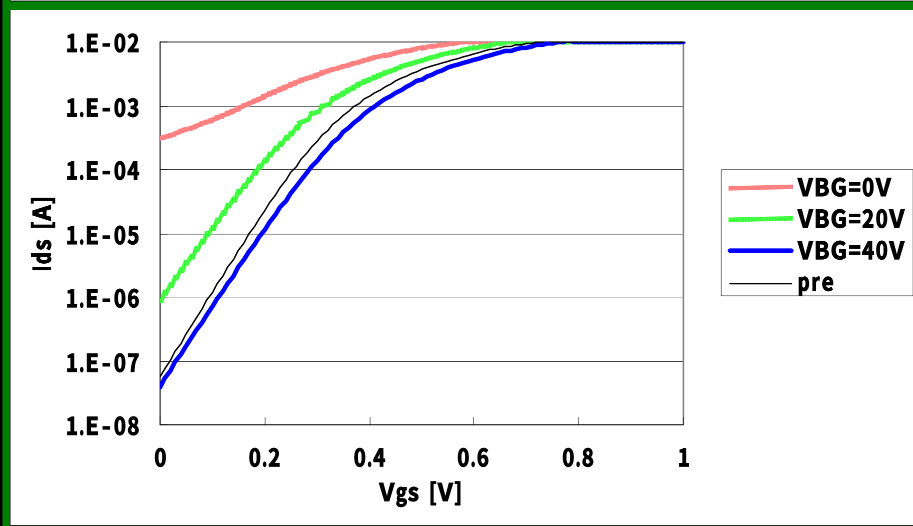
VT shifts of body tie transistors were slightly larger.
Table shows ΔVT(Body Tie) – ΔVT(Floating).

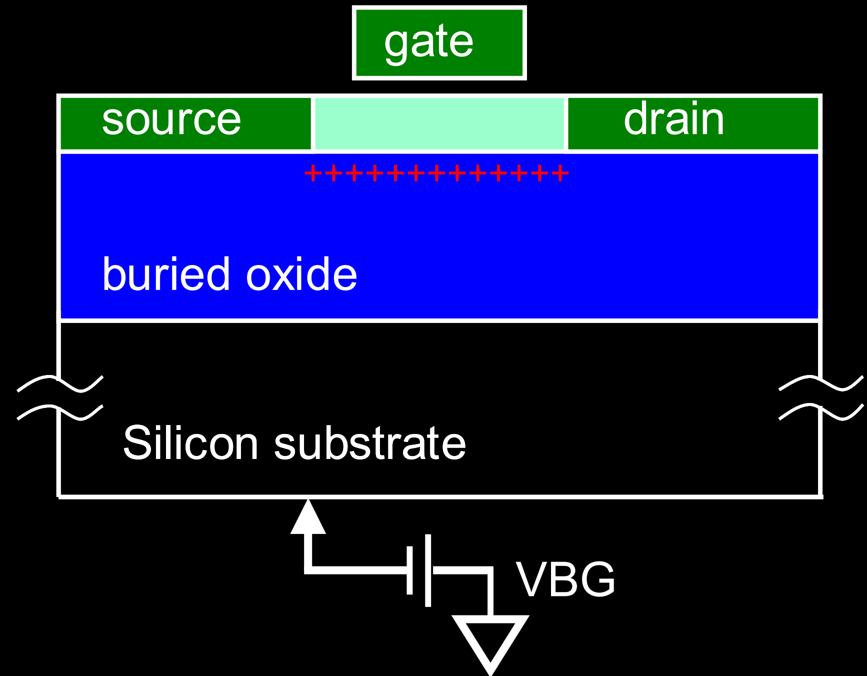
Dose [1MeV n-eq/cm^2]	NMOS LVT	NMOS HVT	NMOS IO	PMOS LVT	PMOS HVT	PMOS IO
$6.4x10^{13}$	3	4	14	3	5	15
$5.8x10^{14}$	4	9	5	11	16	16
$5.5x10^{15}$	1	2	12	5	23	

Unit [mV]

Back gate compensation



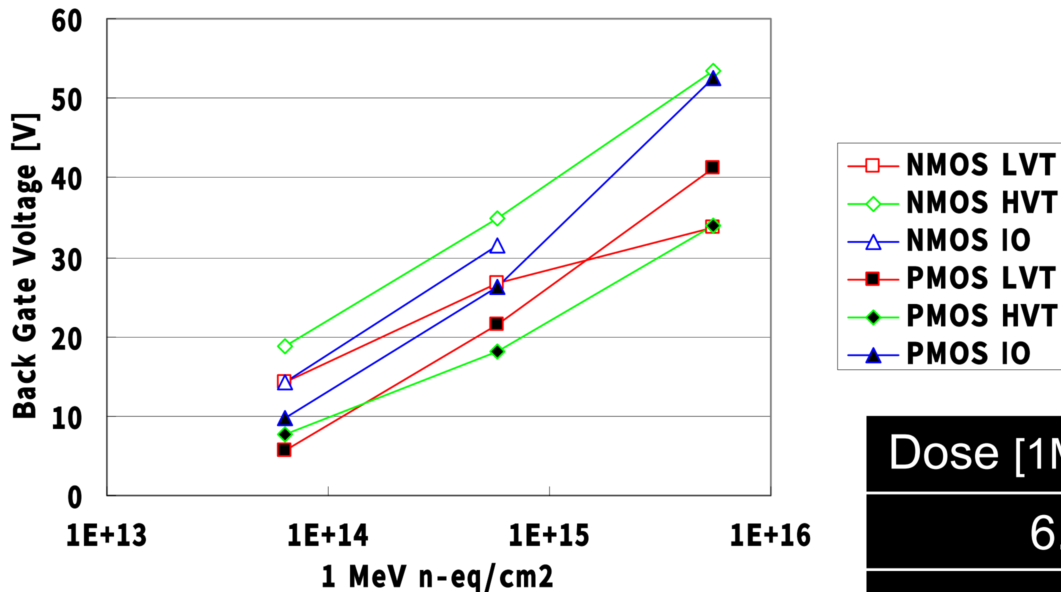




In order to reduce large VT shift, compensation by the back gate voltage is investigated.
This figure shows the I_{ds}-V_{gs} characteristics of typical NMOS transistor for some back gate voltages (Low VT; L/W=0.14/280; Floating) .

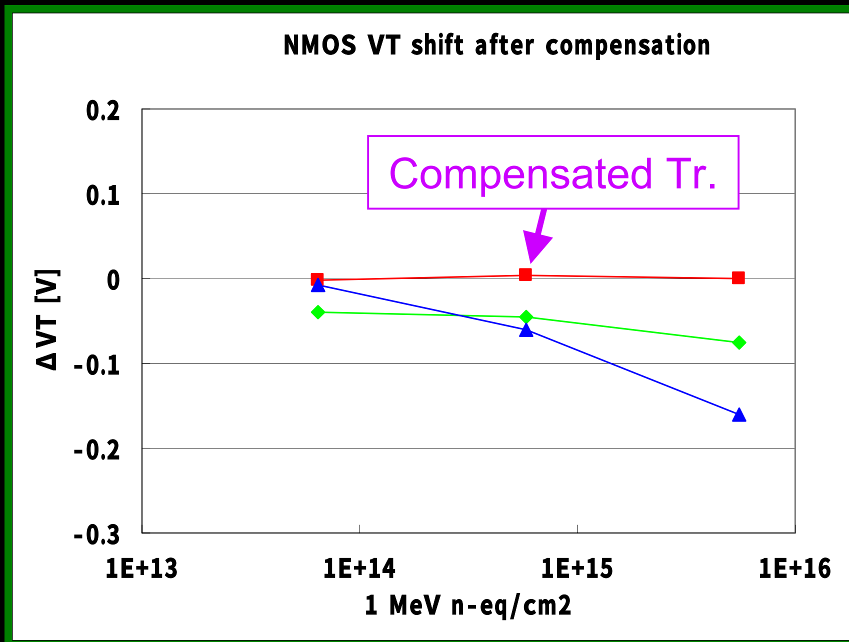
Back Gate Compensation Voltage

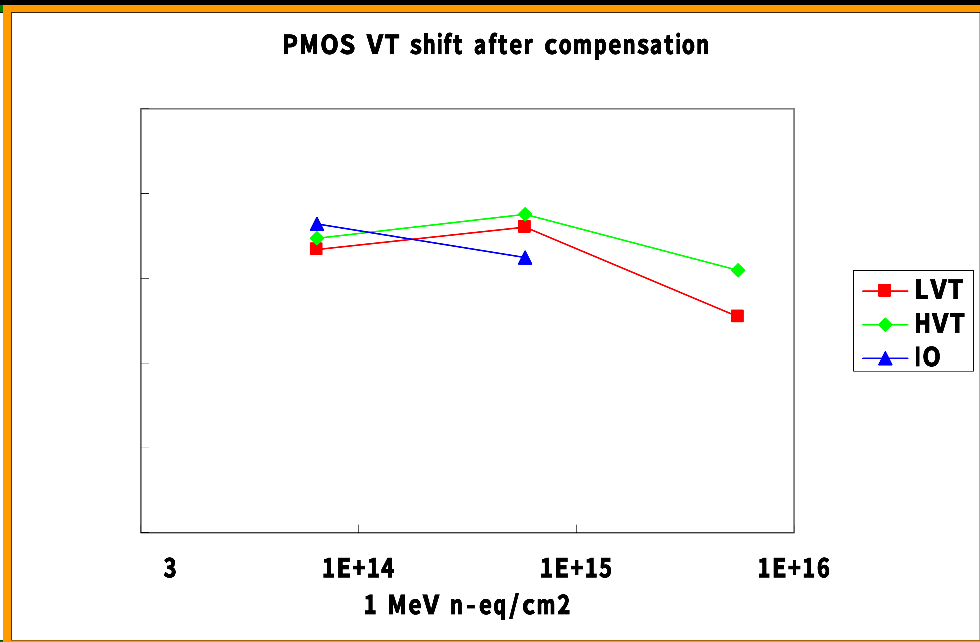
A voltage reference is defined by V_{gs}, where I_{ds}=500μA.
ΔVT=V_{gs} after irradiation – V_{gs} before irradiation
A back gate compensation voltage is defined by V_{BG}, where ΔVT=0V.



Dose [1MeV n-eq/cm^2]	V_{BG} [V]	Δ V_{BG} [V]
6.4x10^{13}	6 ~ 19	13
5.8x10^{14}	18 ~ 35	17
5.5x10^{15}	34 ~ 53	19

Back Gate Compensation (VT shift)





When LVT (L/W=0.14/280; Floating Body) w/o bias condition was compensated by its V_{BG}, VT shifts for other type transistors were investigated.

ΔVT	=	-0.08 ~ -0.04 V	for NMOS HVT
	=	-0.16 ~ -0.01 V	for NMOS IO
	=	-0.05 ~ +0.06 V	for PMOS LVT
	=	+0.01~ + 0.08 V	for PMOS HVT
	=	< -0.5 ~ +0.06 V	for PMOS IO

Summary

- Irradiation tests up to 5.5×10^{15} p/cm^2 for OKI SOI MOS transistors were performed.
- Maximum threshold shifts were found to be

  $\Delta VT = -0.13V$ for NMOS (LVT)
  $\Delta VT = -0.19V$ for NMOS (HVT)
  $\Delta VT = -0.44V$ for NMOS (IO)
  $\Delta VT = -0.14V$ for PMOS (LVT)
  $\Delta VT = -0.08V$ for PMOS (HVT)
  $\Delta VT > -0.5V$ for PMOS (IO)
- Minor difference (~20mV) was found in different gate length.
- Minor difference was (~9mV) found in different body tie structure
- Compensation with biasing back gate worked effective in recovery of radiation damage.