Summary of 08.1 OKI SOI CMOS 0.2um Submission

Jan. 15, 2008, Yasuo Arai (KEK)
v2.0(Jan. 18) yasuo.arai@kek.jp

1. Submitted Chips

5.0 mm x 5.0 mm ---- 8 chips (2 chips include four 2.4 x 2.4 mm^2 chips in each chip)
10.2 mm x 10.2mm --- 1 chip

Top Cell Name	GDS file	Chip size	Affiliation	Designer(s)
TOP_JAXA	TOP_JAXA.gds	5.0 mm		
	ADC_TEG.gds	2.4 mm	JAXA/ISAS	Ikeda
	CCD_TEG.gds	2.4 mm	JAXA/ISAS	Ikeda
	ISAS_SET_0801.gds	2.4 mm	JAXA/ISAS	Kobayashi
	Chip080113.gds	2.4 mm	U of Tokyo	Shimazoe
TOP_KEK	TOP_KEK.gds	5.0 mm		
	RINGS.gds	2.4 mm	KEK	Miyake
	TDCTOP.gds	2.4 mm	KEK	Tauchi
	TOPCELL2.gds	2.4 mm	KEK	Ikemoto
	top_tpix.gds	2.4 mm	KEK	Arai
Achip2	Achip2.gds	5.0 mm	LBNL	P. Denes
WorkingIORing	CAP7-Hawaii.gds	5.0 mm	U of Hawaii	M. P. Cooney
OKI_TOP	OKI02_FNAL.gds	5.0 mm	FNAL	G. Deptuch, M. Trimpl
TOP_TRTEG3	TOP_TRTEG3.gds	5.0 mm	KEK	Arai, Ikegami
top_spix1	top_spix1_v4.gds	5.0 mm	KEK	Arai
top_ipix2	top_ipix2_v4.gds	5.0 mm	KEK	Arai
top_cpix2	top_cpix2_v4.gds	10.2 mm	KEK	Arai

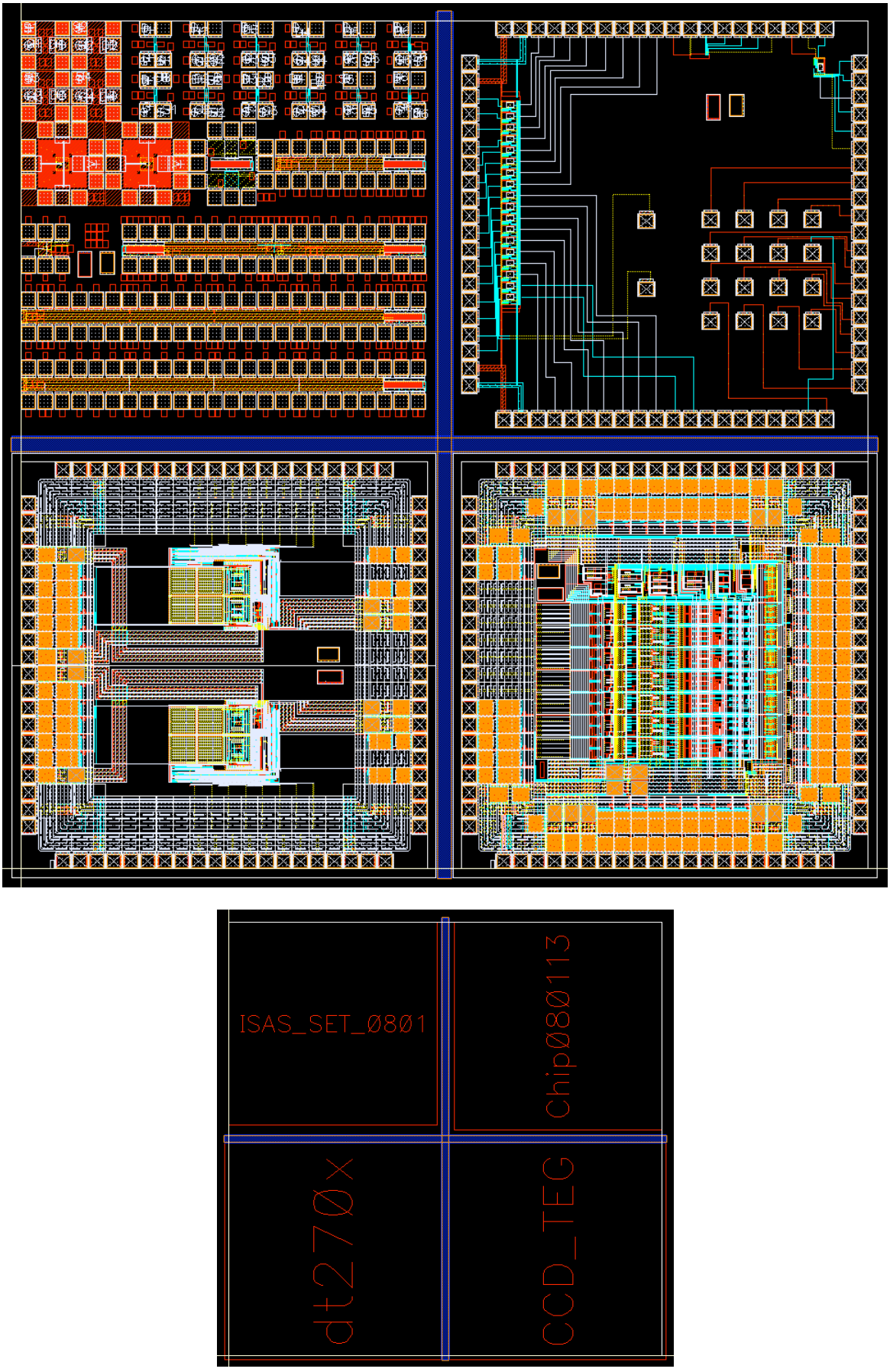
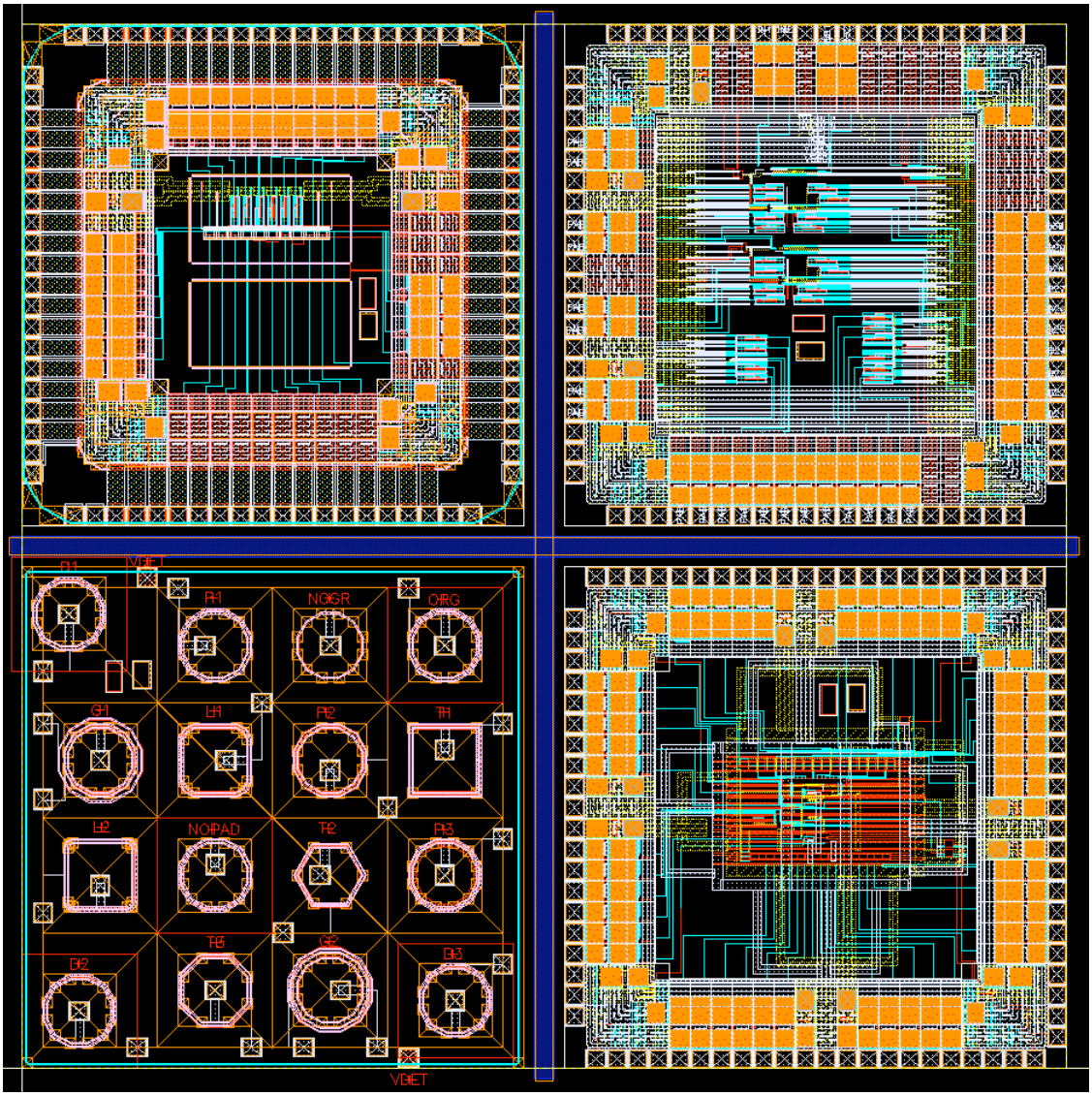


Fig. 1 TOP_JAXA



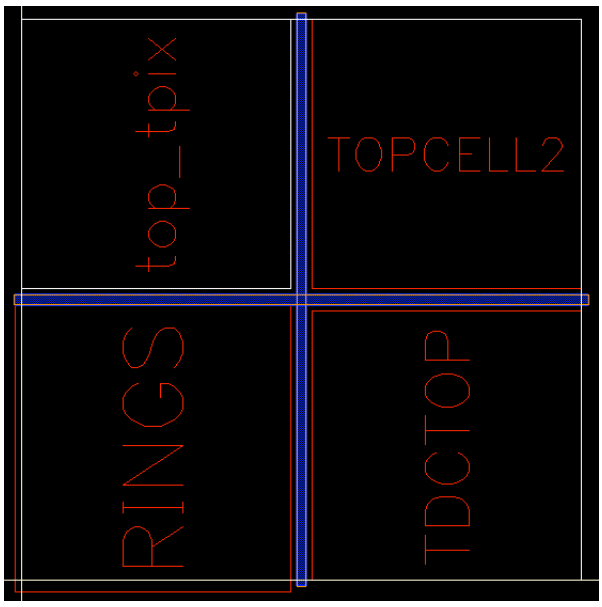


Fig. 2 TOP_KEK

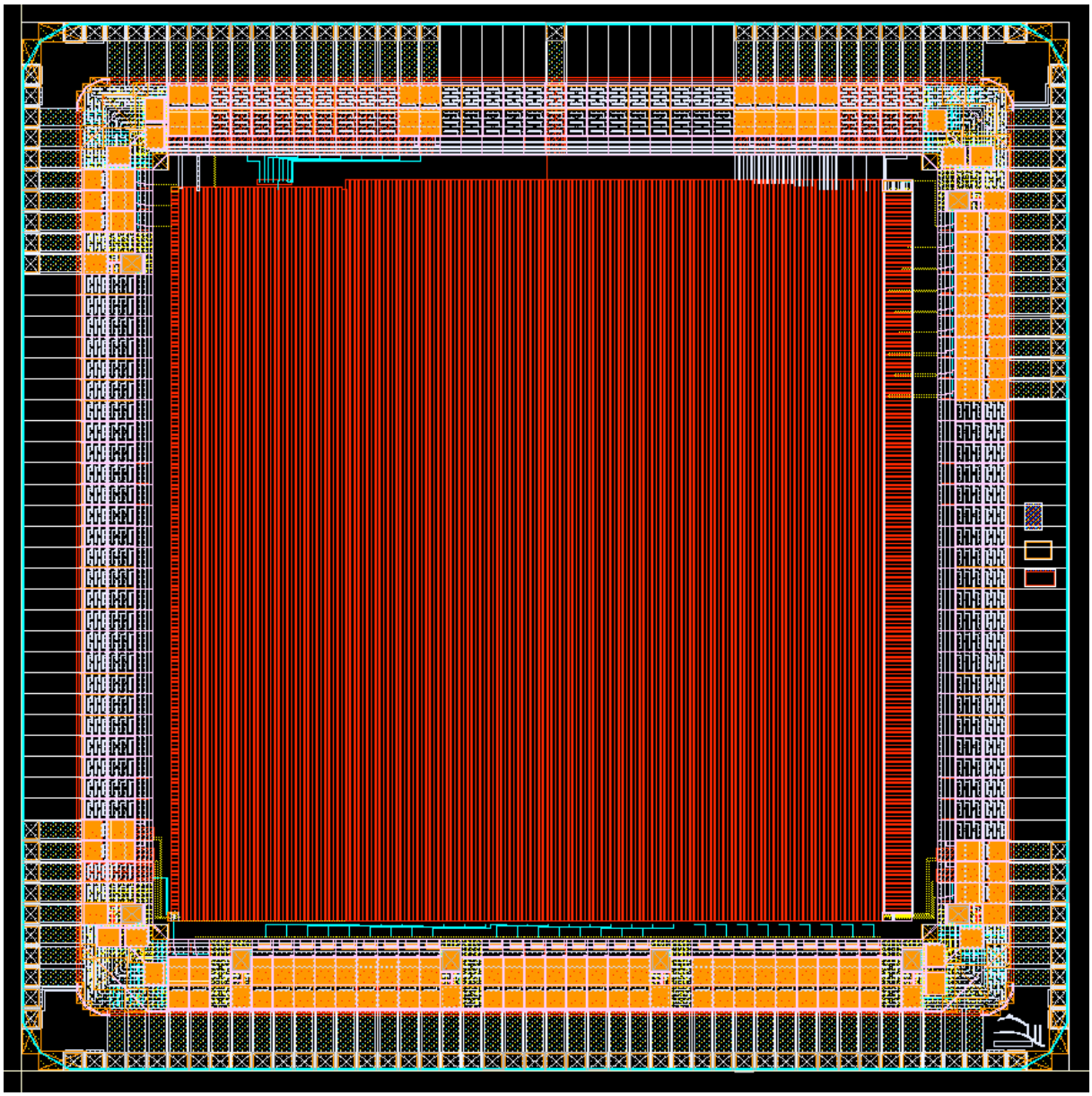


Fig. 3 Achip2

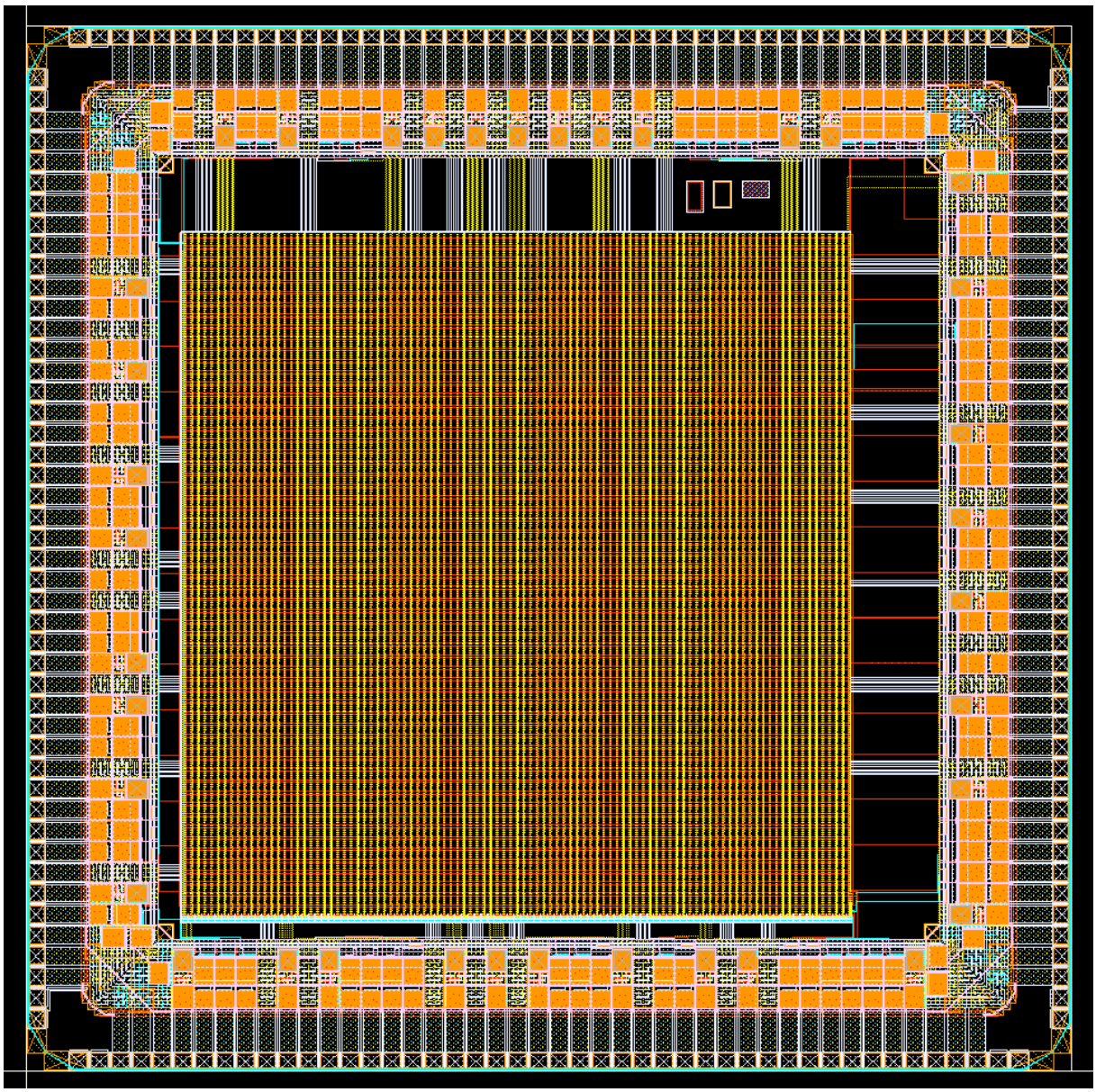


Fig. 4 WorkingIORing

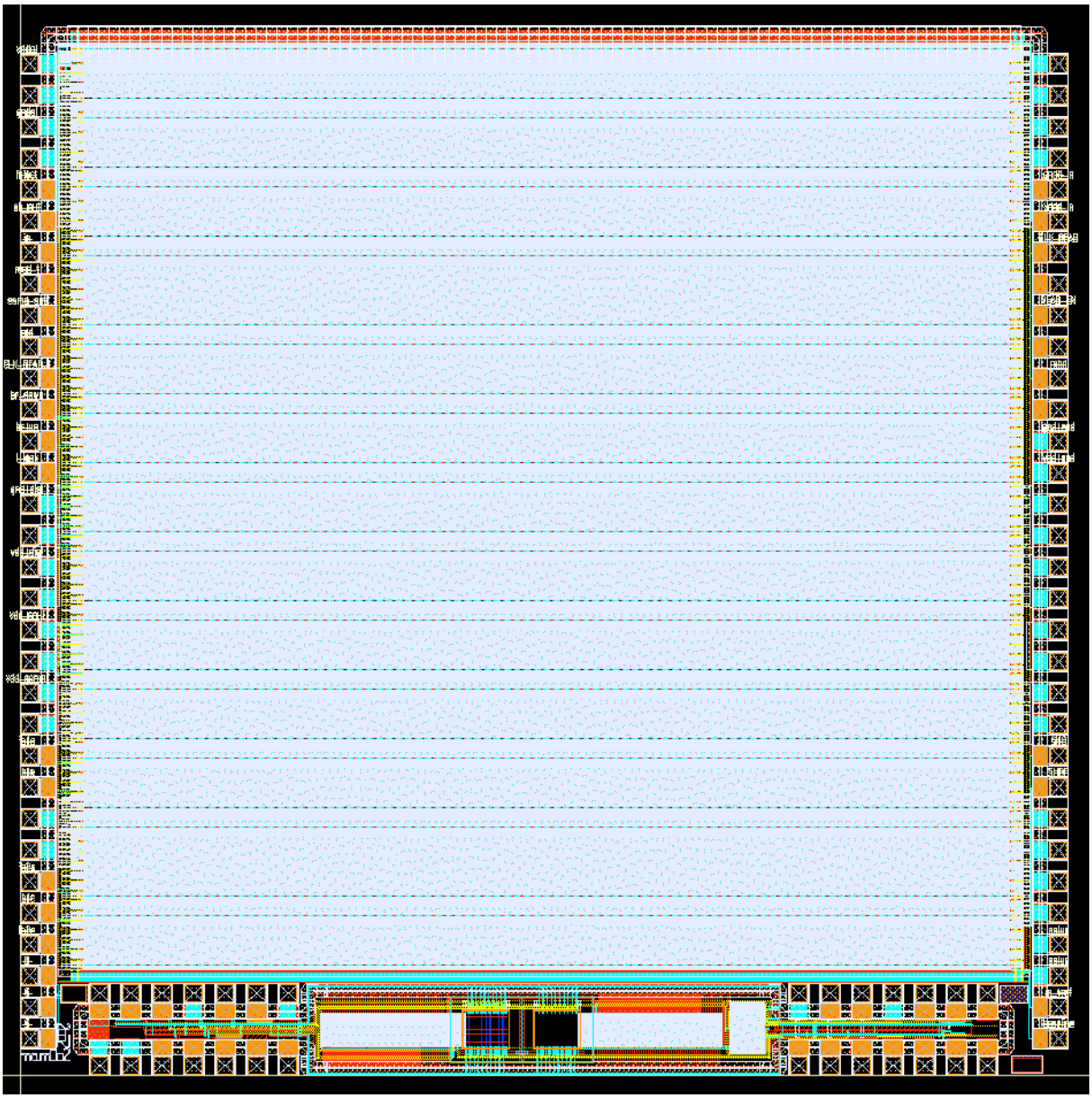


Fig. 5 OKI_TOP

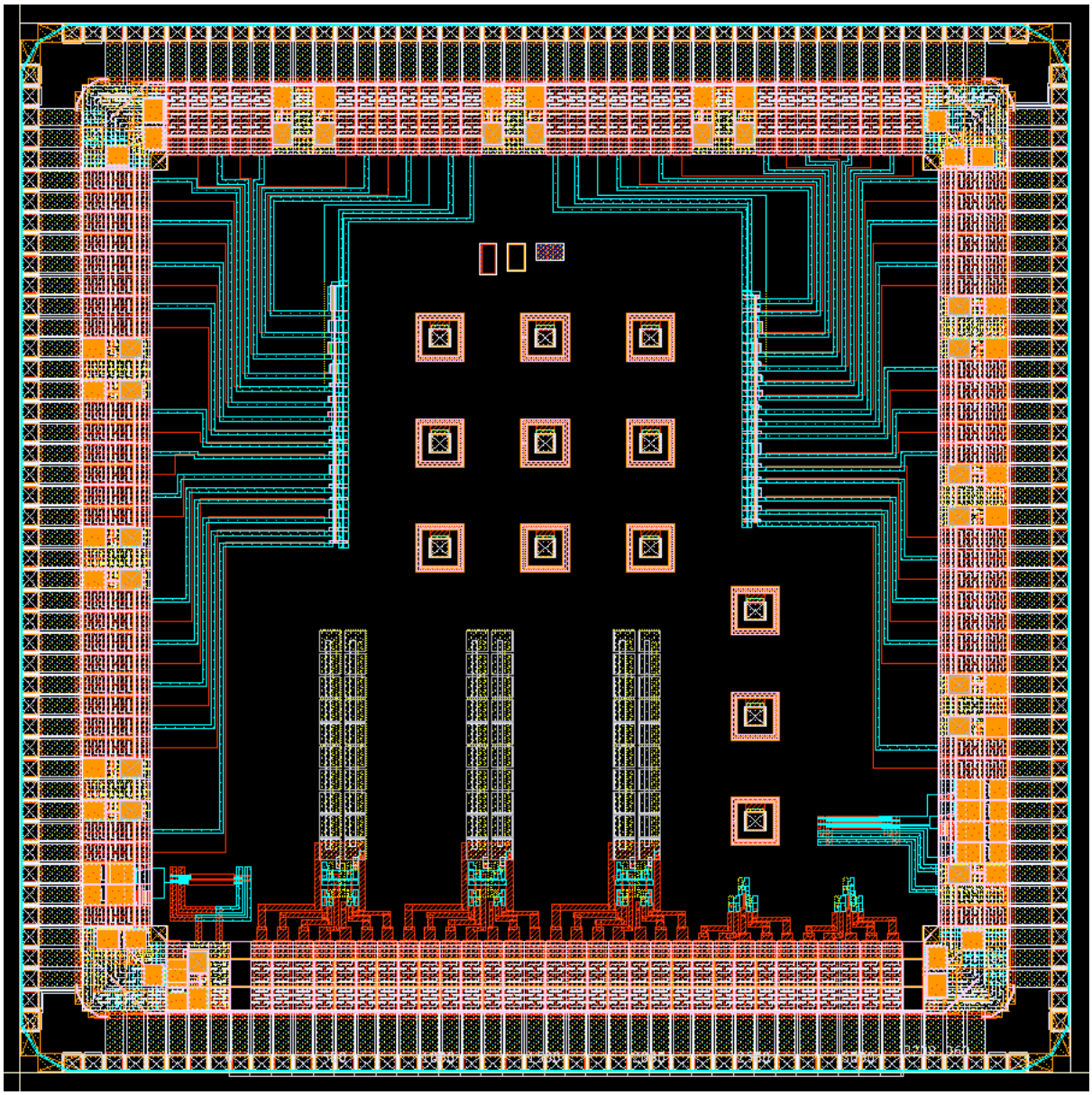


Fig. 6 TOP_TRTEG3

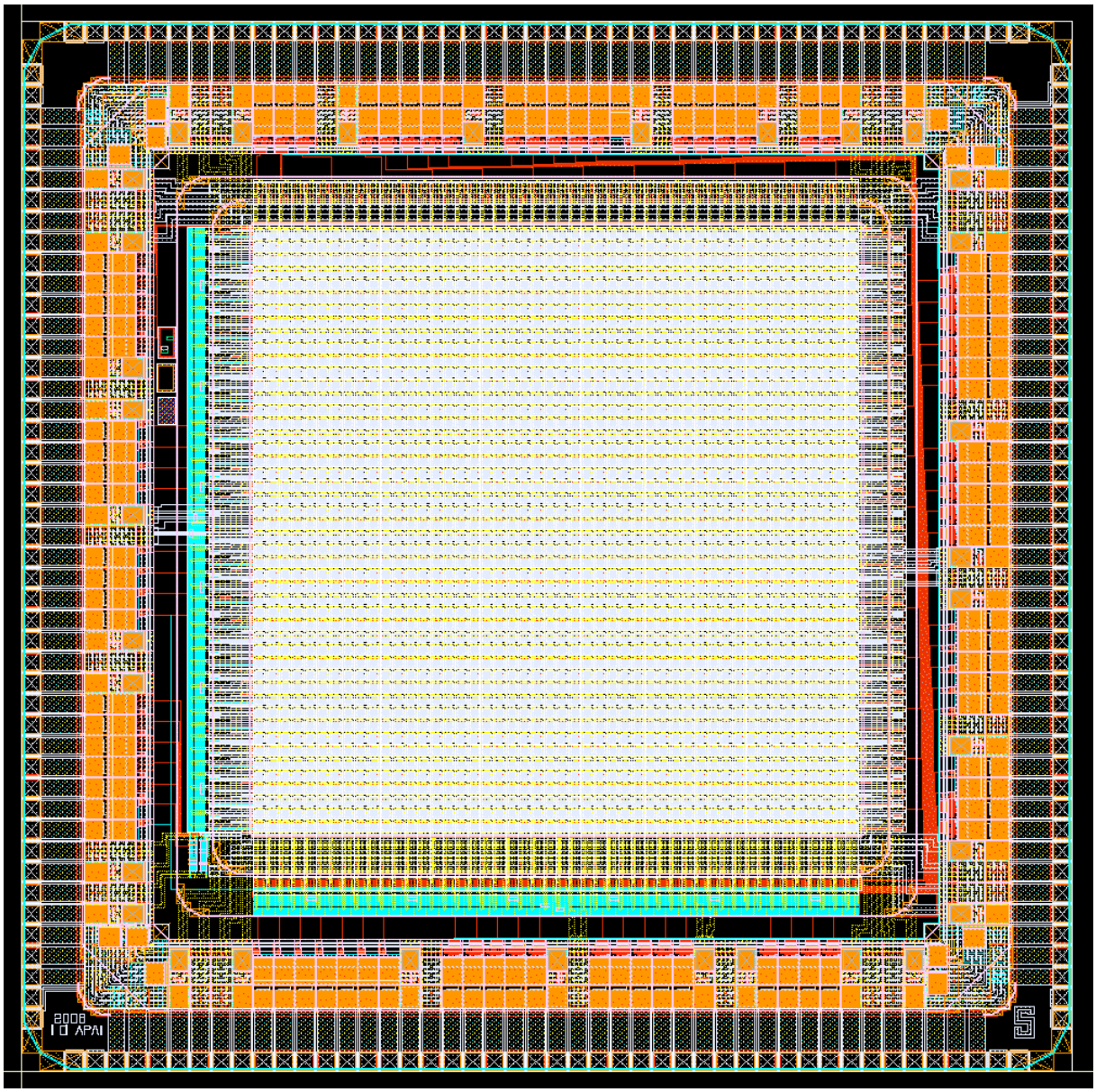


Fig. 7 top_spix1

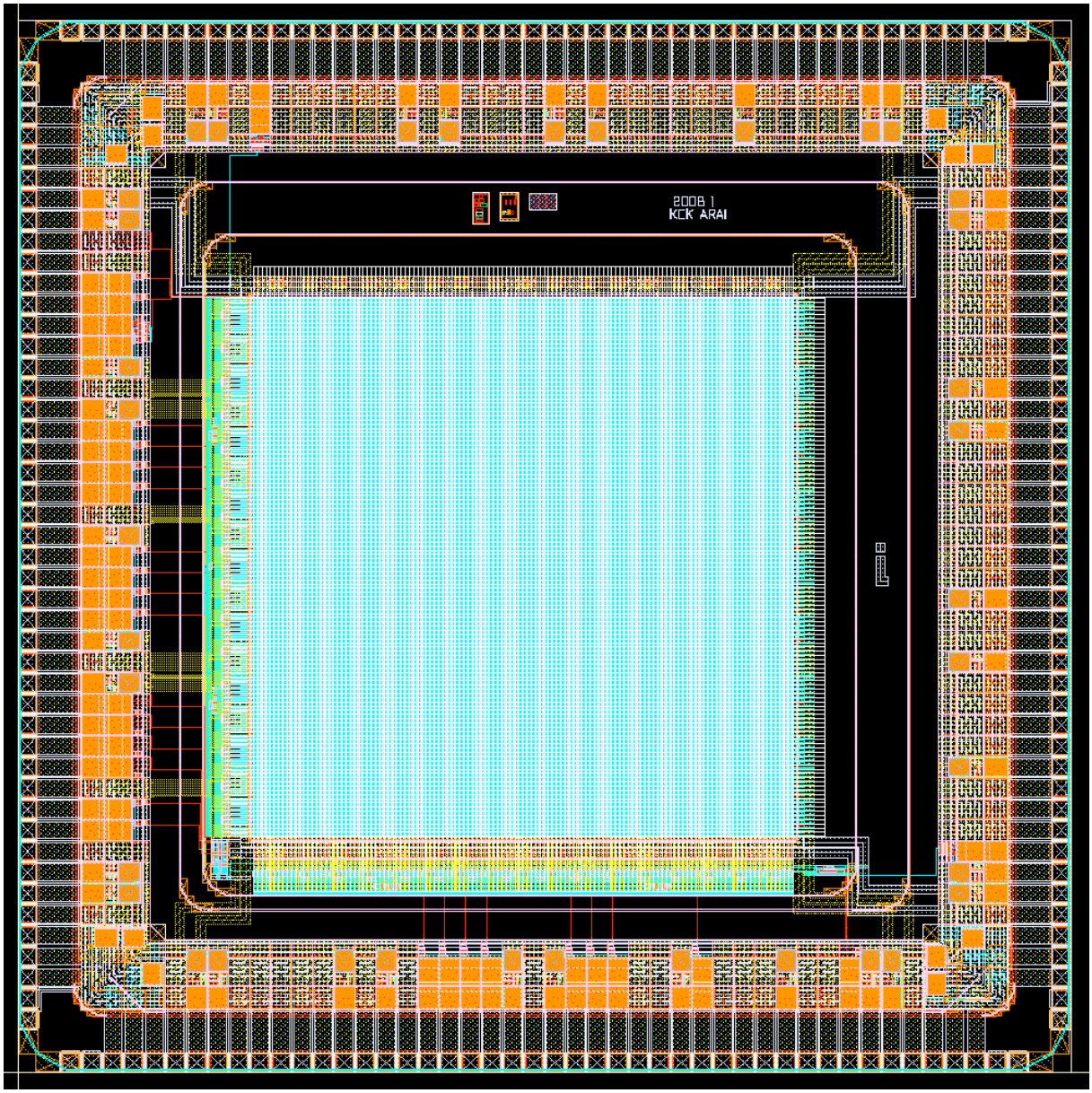


Fig. 8 top_ipix2

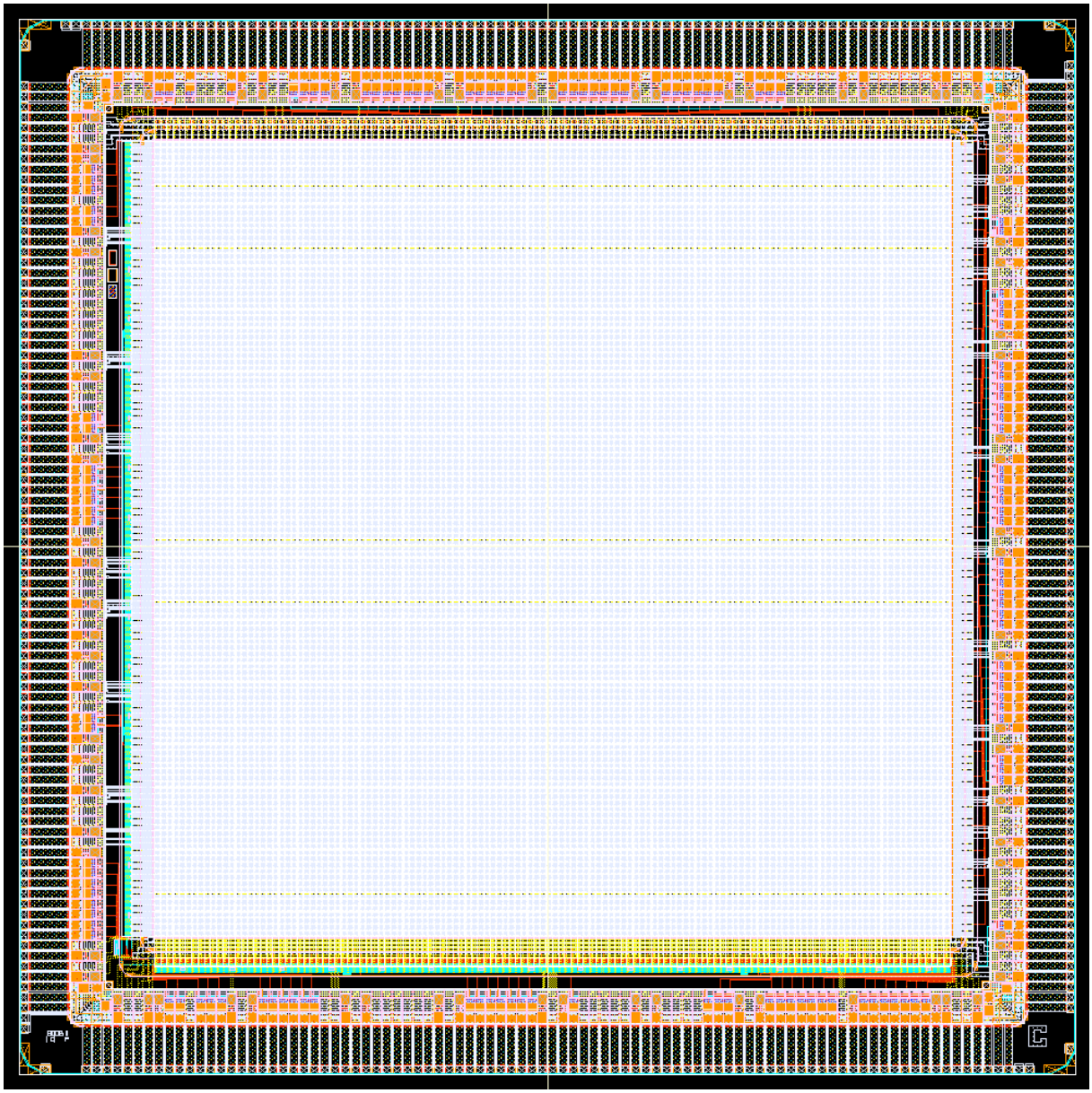


Fig. 9 top_cpix2