Introduction of SOI Pixel Development

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OUTLINE

• Introduction of SOI Technology
• SOI Pixel Detector Development
• On-Going R&D’s
• Summary
SOI Wafer Production (Smart Cut by SOITEC)

1. Initial silicon
2. Oxidation
3. Implantation
4. Cleaning and bonding
5. Splitting
6. Annealing and CMP touch polishing
7. Donor wafer becomes new wafer A

CMOS (Low R)
Sensor (High R)
In SOI, Each Device is completely isolated by Oxide.
Industry move: Bulk CMOS to PD-/FD- SOI CMOS

Faces many barriers to further miniaturization

Bulk Transistor

Channel Forms in Bulk Silicon

PD-SOI Transistor

Body

Is Partially Depleted and ‘floats’ independent from Bulk substrate

Fully-Depleted

Ultra-Thin Body is Fully Depleted

Box can optionally be ultra-thin, too

Partially-Depleted

Floating Body boosts performance but introduces some peculiarities (History Effect, kink)

Addresses scalability issues

No History Effect

No kink effect

Tsi ~ 70 nm . Tbox ~ 145 nm

Our SOI

Tsi ~ 5-10 nm (e/o process)
Tbox ~ 145nm / Tultbox ~ 10-30nm

(from "Fully DepletedSOI", Xavior Cauchy, SOI Industry Consortium)
Steep Sub Threshold Slope

Gate voltage is not wasted to deplete the bulk.

Lower Threshold (Leakage Current) is possible without increasing Leakage Current (Vth).
SOI Performance: Smaller Junction Capacitance

Cj is 1/10 of Bulk technology. Gate Capacitance is 30-40% Lower.

High Speed / Low Power
Radiation Tolerance

SOI is Immune to Single Event Effect

But not necessary strong to Total Ionization Dose due to thick BOX layer

This must be remedy for the application under high radiation environment.
Operation at Cryogenic Temperature

Bulk MOS  →  4.2K  →  SOI MOS (worked in 1.4K)
Monolithic Detector having fine resolution of silicon and data processing power of CMOS LSI by using Silicon-On-Insulator (SOI) Technology.

**SOI Pixel Detector (SOIPIX)**

- **Si Sensor** (High Resistivity Substrate)
- **BPW (Buried p-Well)**
- **PMOS**
- **NMOS**
- **BOX (Buried Oxide)**
- **n+(p+)**
- **p+(n+)**
- **n-(p-)**

Backside Implant, Laser Annealing, Al deposit

Charged Particle (X-ray, Electron, Alpha, ...)

LSI Circuit
Feature of SOI Pixel Detector

- No mechanical bonding. Fabricated with semiconductor process only, so high reliability, low cost are expected.

- Fully depleted thick sensing region with Low sense node capacitance.

- On Pixel processing with CMOS transistors.

- Can be operated in wide temperature (4K-570K) range, and has low single event cross section.

- Based on Industry Standard Technology.
**Lapis (*) Semiconductor 0.2 µm FD-SOI Pixel Process**

<table>
<thead>
<tr>
<th>Process</th>
<th>0.2µm Low-Leakage Fully-Depleted SOI CMOS 1 Poly, 5 Metal layers. MIM Capacitor (1.5 fF/um²), DMOS Core (I/O) Voltage = 1.8 (3.3) V</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOI wafer</td>
<td>Diameter: 200 mmφ, 720 µm thick Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz (n) ~700 Ω-cm, FZ(n) &gt;1 k Ω-cm, FZ(p) &gt;1 k Ω-cm</td>
</tr>
<tr>
<td>Backside process</td>
<td>Mechanical Grind, Chemical Etching, Back side Implant, Laser Annealing and Al plating</td>
</tr>
</tbody>
</table>

(*) Former OKI Semiconductor Co. Ltd.
Regular Multi-Project Wafer (MPW) run. (~twice/year)
Submission from Chinese Coleague

- 2013.1 MX1594
  IHEP (Lu Yunpeng) 6x6 mm² + 2.9x2.9 mm²
  SARI (Ning, Wang, Li Tian) 2.9x2.9 mm²
- 2012.7 MX1542
  IMECAS(Zhao Kai) 12.2x12.2 mm² + 2.9x2.9mm²
- 2011.10 MX1501
  IHEP (Liu Gang, Lei Fan) 2.9x2.9 mm²
  IHEP (Lu Yunpeng) 2.9x2.9mm²
- 2011.1 MX1442
  IHEP(Liu Gang) 2.4x2.4mm²
- 2010.8 MX1413
  IHEP(Zheng Wang, Lei Fan) 2.4x2.4 mm² x2
Transistor Type

Core Transistor (1.8V) : Normal Vth & Low Vth
I/O Transistor   (3.3V) : Normal Vth & High Vth

Body Floating  Source-Tie (Type 1)  Source-Tie (Type 2)
Structure of Top Si

1 Poly + 5 Metal

MIM Capacitor on 3M
Sensor Structure

- **PS & NS --- High Doping Density Layer (Top Si is removed)**
- **BPW, BP2, BP3 & BNW --- Low Doping Density Layer (Top Si is not removed)**
Trace Fuse (option)

You can chase the chip location where it come from if you include this fuse in your design.

Number of Fuse (total 16 lines)
* Lot No. : 4 lines (1~15)
* Wafer No. : 5 lines (1~31)
* Chip Location in wafer : 7 lines (1~127)

Laser Cut
**I/O Cell Libraries**

We prepared several I/O frames for your convenience.

- **Chip Frame for Pixel**
  - I/O Buffers
  - + Vdet ring
  - + Vbias ring
  - + BPW

- **2.9 mm Frame**

- **6 mm Frame**
We get minimum number of I/O cells from Lapis. Then we have created many more for users. Please provide us your I/O cells if you develop new one.
• We are using relatively large mask to enable many designs and large sensors
• Low cost per area.
• Smallest chip area: 2.9 x 2.9 mm²
Stitching Exposure

Mask Layout

Exposed Layout

If you want much larger detector …
Riken SOPHIAS detector

- Width of the Buffer Region can be less than 10um.
- Accuracy of Overwrap is better than 0.025um.
It was difficult to process 8” FZ-SOI wafer in CMOS process.

<table>
<thead>
<tr>
<th>Before Oxidation</th>
<th>Conventional SOI Process</th>
<th>Improved SOI Process</th>
</tr>
</thead>
</table>

![Images of wafer with and without slips]

We optimized the process parameters, and succeeded to perform the process without creating many slips.
High Resistive wafers

CZ(n) 0.7 kΩcm 260 μm
Mechanical Grind

FZ(n) 7 kΩcm 500 μm

FZ(p) 40 kΩcm 500 μm
Chemical Etch

Leakage Current [A]

Wdepletion[um]
Data Acquisition Board

- Soi Evaluation Board with SITcp (SEABAS)
- A FPGA controls the SOI Pixel chip
- Directly transferred to Ethernet
On-Going SOI Projects in Japan

- INTPIX : Genera Purpose Integration Type
- CNTPPIX : General Purpose Counting Type
- SOPHIAS : Large Dynamic Range for XFEL
- PIXOR : Belle II Vertex Detector
- XRPIX : X-ray Astronomy in Satellite
- MALPIX : TOF Imaging Mass Spectrometer
- TDIPIX : Contamination Inspection
- LHDPIX : Nuclear Fusion Plasma X-ray
- ...

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Integration Type Pixel (INTPIX)

\[ V_{\text{sense}} = \frac{Q}{C} \approx \frac{0.6 \, fC}{8 \, fF} = 70 \, mV \]

Size: 14 \( \mu m \) x 14 \( \mu m \) with CDS circuit
INTPIX6 Pixel
2 Gain
12 x 12 um²
INTPIX4
Pixel Size: 17 um x 17 um
No. of Pixel: 512 x 832 (= 425,984)
Chip Size: 10.3 mm x 15.5 mm
Vsensor=200V, 250us Int. x 500
X-ray Tube: Mo, 20kV, 5mA

X-ray Image of a small dried sardine taken by a INTPIX4 sensor (3 images are combined).

Fine resolution & High Contrast

(A. Takeda)
Cu $K_\alpha$ and $K_\beta$ is separated
Noise $\sim 23$ electrons $@ -50^\circ C$

X-ray Energy Spectrum

Al-$K_\alpha$ (1.49 keV)

188 eV (FWHM)

(Cu-$K_\alpha$ 8.04 keV)

SE Escape?

Cu-$K_\beta$ 8.90 keV

Mo-$K_\alpha$ 17.44 keV

XRPIX1 (Kyoto Univ.)
Compton Electrons from High-Energy X-rays
Issues in SOI Pixel

Sensor and Electronics are located very near. This cause...

We need additional back-plane to suppress these effects.
• Suppress the Back Gate Effect.
• Shrink pixel size without losing sensitive area.
• Increase breakdown voltage with low dose region.
• Less electric field in the BOX which improves radiation hardness.
$I_d-V_g$ and BPW

NMOS

w/o BPW

with BPW=0V

Back gate effect is suppressed by the BPW.
Double SOI Wafer

- Shield transistors from bottom electric field
- Compensate electric field generated by the trapped hole in the BOX.
- Reduce crosstalk between sensors and circuits.
Cross Talk from the circuit to the sensor can be reduced 1/10, and signal shape will be bipolar. → disappear in charge amp.
Suppression of Back-Gate Effect with Middle-Si layer

a) Middle-Si Floating

b) Middle-Si = GND

Back-Gate Effect is fully suppressed with the Middle Si Layer of fixed voltage.

Nch Core Normal-Vt
L / W = 0.2 / 5.0um
Vd=0.1V
Trapped Charge Compensation (Threshold Control) with Middle-Si Layer

Threshold voltage of a transistor is controlled with the bias voltage of the Middle-Si layer. This indicates that effects of the trapped charge in the BOX can be compensated with the bias voltage.

Nch Core Normal-Vt
L / W = 0.2 / 5.0 um
Vd=0.1V, Vback: floating
We could observe restoration of the threshold shift with applying negative voltage to the SOI2 layer.
Summary

• SOI technology has many good features; low power, low variability, large operating temperature range, no latch up..., and Industries are moving to extremely thin SOI.

• SOIPIX is monolithic detector, and many kinds of detectors are already working.

• We have ~twice/year regular MPW runs with increasing no. of users.

• The process technology is still progressing; Higher resistivity wafer, Nested well structure, Larger mask size, Stitching, and Double SOI, etc. …

• We welcome new collaborators to the SOI pixel development!