Waveform Observation of Digital Single-Event Transients Employing Monitoring Transistor Technique

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***Abstract*—Waveforms of digital single-event transients, radiation-induced voltage transients in logic gates, can be observed by connecting two transistors to a target logic gate. Additional transistors monitor voltage transients through their drain currents, which can be measured using the conventional 50-Ω transmission-line technique widely used for measuring transient currents in single elementary transistors. Experimental results obtained in pulsed-laser irradiation tests demonstrate the validity of the observation technique and clearly reveal the pulse evolution as a function of the laser pulse energy.**

***Index Terms*—integrated circuit radiation effects, pulsed laser irradiation, semiconductor device radiation effects, single event transients (SETs), soft errors, waveform observations.**

I. Introduction

DIGITAL single-event transients (DSETs) are voltage perturbations generated at logic gates by irradiation. They are likely to become the dominant source of soft errors for advanced CMOS logic very-large-scale-integrations (VLSIs) [1]–[6]. We should precisely obtain their waveform information to investigate their physical mechanisms, build accurate models, and develop highly optimized countermeasures.

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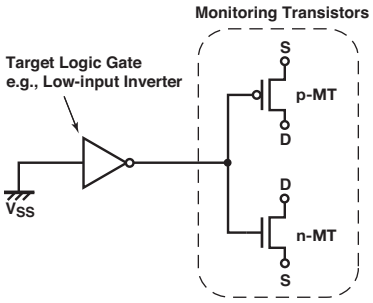

Fig. 1. Proposed circuitry. The output of a target logic gate is connected to the gate inputs of two elementary MOS transistors, one of which is an n-type transistor and the other of which is p-type. The connected transistors named "monitoring transistors (MTs)" fulfill the roles of a DSET monitor.

Previous measurement techniques with built-in circuits like variable temporal latches [7], [8], self-triggering latches/flip-flops [9]–[11], and high drive-capability output-buffers [12], have been achieving remarkable success. For example, they have revealed detailed temporal-width distributions of DSETs and drawn our attention to serious broadening phenomena induced by supply voltage reduction [8] and propagation in circuits [12].

The previous techniques, however, detect only pulse-widths at a specific voltage level because they are based on digital logic circuits. DSETs were digitized while propagating thorough the circuits, thus losing their waveform information except for pulse widths. Other parameters like voltage magnitude and rise/fall times are still unrevealed experimentally.

In this paper, we have developed a technique for observing waveforms of DSETs, hereinafter called the "monitoring transistor (MT) technique". It enables us to obtain DSET signals graphically as voltage versus time curves and thus investigate their various waveform parameters. We have fabricated test chips and performed pulsed-laser irradiation tests. Experimental results have demonstrated its validity.

II. Principle of the MT Technique

A. Circuitry

Fig. 1 illustrates a proposed circuitry. It is a simple and compact structure that consists of one target logic gate, e.g. a low-input inverter, and only two elementary MOS transistors,

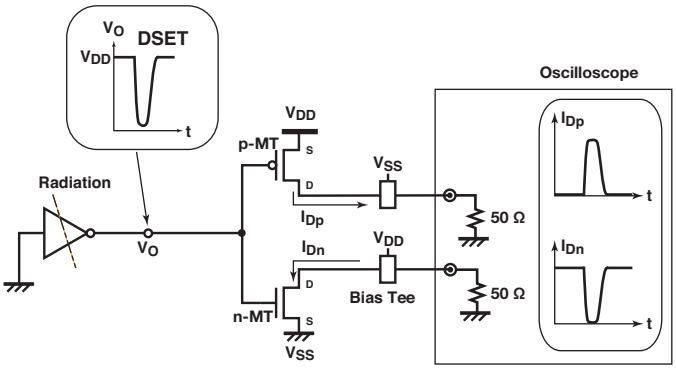

Fig. 2. 50-Ω transmission line measurement technique. The drain terminal of each MT is connected to a 50-Ω input of an oscilloscope through a bias tee, which supplies a constant drain-source voltage. When a DSET is generated, the output voltage V_O changes from its steady state (e.g. V_{DD} in this circuit case). This V_O perturbation defined by a V_O versus t curve generates drain current changes in the MTs. We can record those current signals by the oscilloscope and obtain $I_{Dp(n)}$ versus t curves.

hereinafter called "monitoring transistors (MTs)". One MT is an n-type transistor (n-MT) and the other is p-type (p-MT). Both MTs' gate inputs are connected to the target's output.

The MTs fulfill the roles of a DSET monitor and an output load capacitance for the target logic gate. Note that the output load capacitance is also an important factor determining DSET waveforms, as mentioned in our previous study [13]. It is thus imperative that the gate lengths and widths of the both MTs are adequately designed to obtain a desired output load capacitance.

B. Measurements

As illustrated in Fig. 2, measurements are performed using a conventional 50-Ω transmission line technique, which is widely used for measuring transient characteristics of transistors including radiation-induced transient currents in single MOSFETs [14]–[16].

The drain terminal of each MT is connected to a 50-Ω input of an oscilloscope through a bias tee, which supplies a constant drain-source voltage. For the n-MT, for example, its drain terminal is biased at a power supply voltage V_{DD} while its source is tied to the ground voltage V_{SS}. The bias condition of the p-MT is similar to that of the n-MT but with all of the polarities reversed as shown in the figure.

A DSET is generated at the target logic gate when it is irradiated. In this example, its output voltage V_O becomes lower than its steady state voltage V_{DD} for a short time. Because the output is connected to the MT gate inputs, such V_O perturbation directly changes the MT gate-source voltages, which determine the drain currents I_{Dn} and I_{Dp}. Therefore, the DSET produces transient changes in the drain currents.

The transient I_D-changes can be recorded by the oscilloscope as a function of the elapsed time t. As a result of this measurement, for each MT, we can obtain an I_D versus t curve by adding the recorded I_D-change to its standby current.

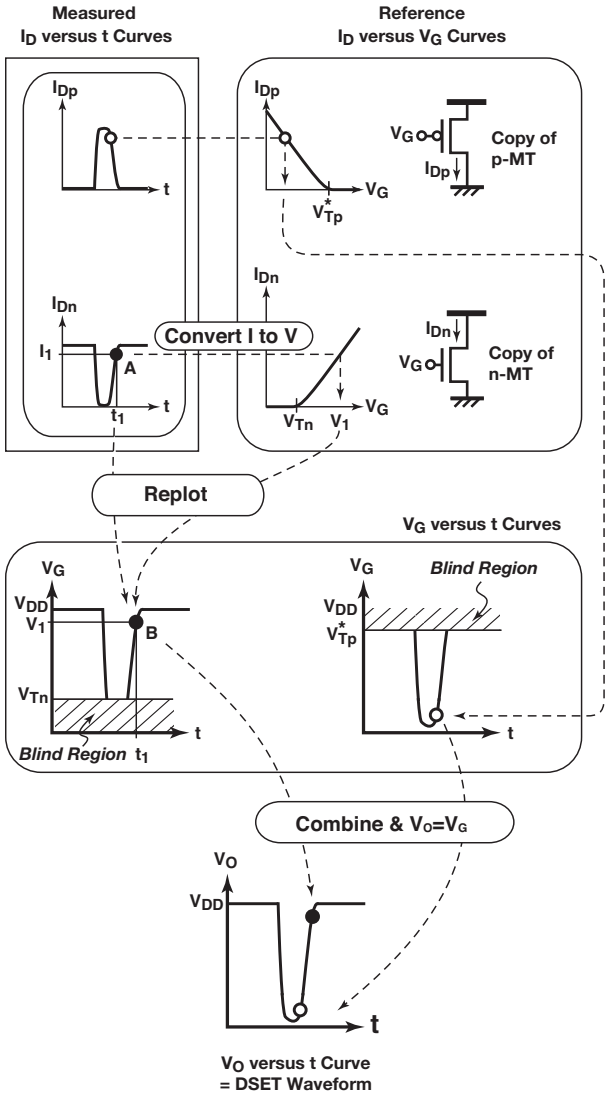

Fig. 3. Conversion from I_D versus t curves to DSET waveform (V_O versus t curve). Using I_D versus V_G curves measured with copies of the MTs, we convert an I_D value for each point in time into a gate-voltage value V_G. By repeating this conversion, we obtain V_G versus t curves. Because each of the curves describes DSET imperfectly due to their threshold effects, we combine the two curves and finally obtain the waveform of the DSET using a relationship $V_O = V_G$. Note that V^*_{Tp} represents $V_{DD} - |V_{Tp}|$, where V_{Tp} represents the threshold voltage for p-MT.

C. Conversion

By converting the measured I_D versus t curves as illustrated in Fig. 3, we obtain the original DSET waveform; i.e. the V_O versus t curve. This conversion uses a conventional technique to make measurements, such as those of the potential of floating-gates in floating-gate MOS memories [17], [18] and pass leak-currents in transistors [19], [20].

For ease of explanation, we first focus on the I_{Dn} versus t curve for the n-MT. As mentioned in the Sec. IIB, the drain current I_D is determined by the gate voltage V_G, and their relationship, i.e. the I_D versus V_G curve, can be measured with a copy of the n-MT. Using this curve as a reference, we convert an I_{Dn} value for each point in time into a gate-voltage value V_G.

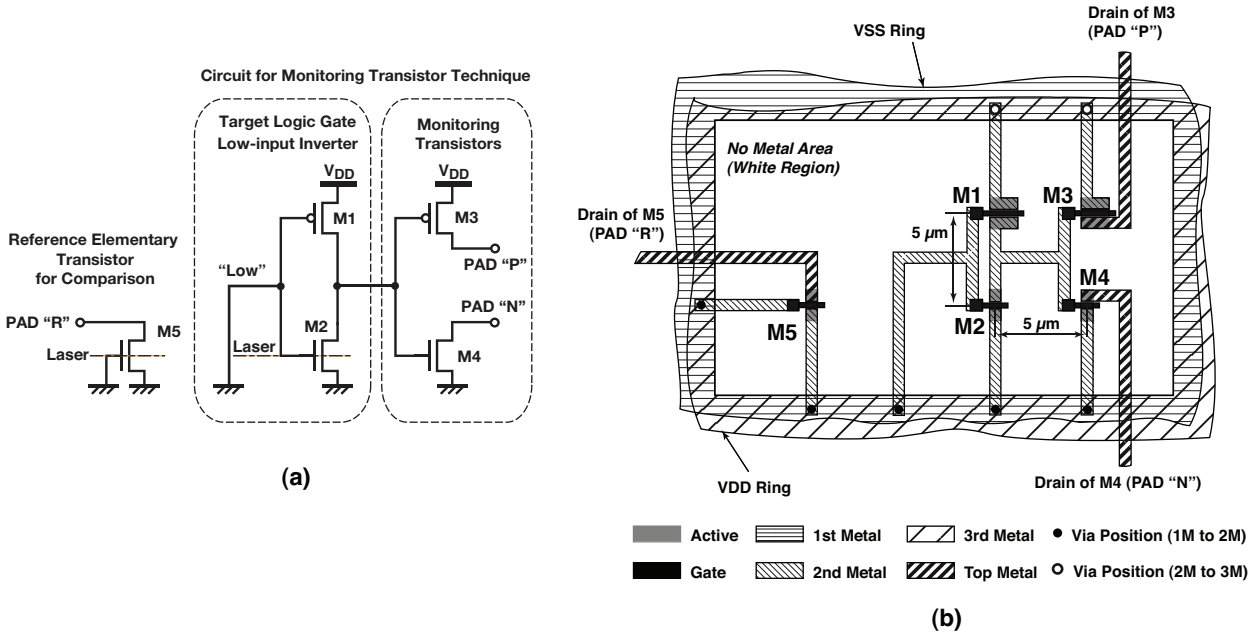

Fig. 4. Fabricated test circuits: schematic drawing (a) and pattern layout (b). The inverter that consists of M1 and M2 was designed as a target logic gate. M3 and M4 worked for p-MT and n-MT, respectively. M5 was a reference transistor used for discussing the validity of the MT technique. The all p-type transistors (M1 and M3) had drawing dimensions of 0.2-μm gate length and 1.46-μm width, and the all n-type (M2, M4, and M5) had 0.2-μm gate length and 0.6-μm width.

For example, I_1 at t_1 (Point A on the I_{Dn} versus t curve) can be converted into V_1 through the reference I_{Dn} versus V_G curve. The point A can be then replotted onto the V_G versus t plane as the point B. By repeating this I_D to V_G conversion, we obtain a V_G versus t curve.

Because $V_G = V_O$, the resultant V_G versus t curve describes the DSET waveform, but imperfectly in some cases. As shown in this example, for voltages below the n-MT threshold voltage V_{Tn}, we cannot trace the V_G versus t curve because the n-MT is in the off-state where $I_{Dn} \approx 0$.

In this blind region for the n-MT, on the other hand, the p-MT operates in the on-state and provides a clear V_G versus t curve. By combining the two complementary V_G versus t curves, we can obtain a full V_O versus t curve; i.e. a DSET waveform. This is one of the most important reasons why we design MTs with the p-type and n-type transistors complementarily.

III. Experimental

We fabricated test circuits and performed pulsed-laser irradiation experiments.

A. Test Circuits

Through the KEK detector technology project [21], we fabricated the test circuits using 0.2-μm fully depleted silicon-on-insulator (SOI) technology provided by OKI Electric Industry [22]. Fig. 4 shows their schematic diagram (a) and pattern layout (b).

We designed an inverter as a target logic gate. It consisted of a p-type transistor and an n-type transistor, respectively indicated by M1 and M2 in the figure. The n-type transistor had drawing dimensions of 0.2-μm gate length and 0.6-μm gate width, and the p-type had 0.2-μm length and 1.46-μm width. We grounded the inverter's input to keep it in the "low-input state".

We designed p-MT (M3 in the figure) with a copy of the p-type transistor in the inverter (M1), and n-MT (M4) with the n-type (M2). In this experiment, DSETs were thus obtained in the equivalent condition that the target inverter's output was connected to a copy of the inverter. This is the most basic circuit configuration named "FO1 (fanout of one) [23]" or "Load 1 [12]", widely used in previous DSET measurements. We placed the transistors with 5-μm spacing to ensure that the laser spot only fell on the target transistor.

M5 was a gate-grounded n-type transistor used for discussing the validity of our technique. It was a copy of M2, the n-type transistor in the inverter.

B. Pulsed Laser Irradiation

We performed laser irradiation tests at the pulsed laser SEE facility in the Naval Research Laboratory [24]–[26]. The experimental system in this study is basically the same as that in a previous study [27].

We mounted the circuits in a high-frequency package with short bonding wires from pads to package outputs. We used a sampling oscilloscope TDS8200 with high-bandwidth heads and bias tees. The maximum bandwidth of this system was around 20 GHz.

We focused the laser beam on the off-state n-type transistor in the target inverter (M2) and concurrently recorded both MTs' responses while the power supply voltage V_{DD} was set at the nominal value for the fabrication process, 1.8 V. The laser centered at 590 nm (2.1 eV) with 1.2-μm FWHM

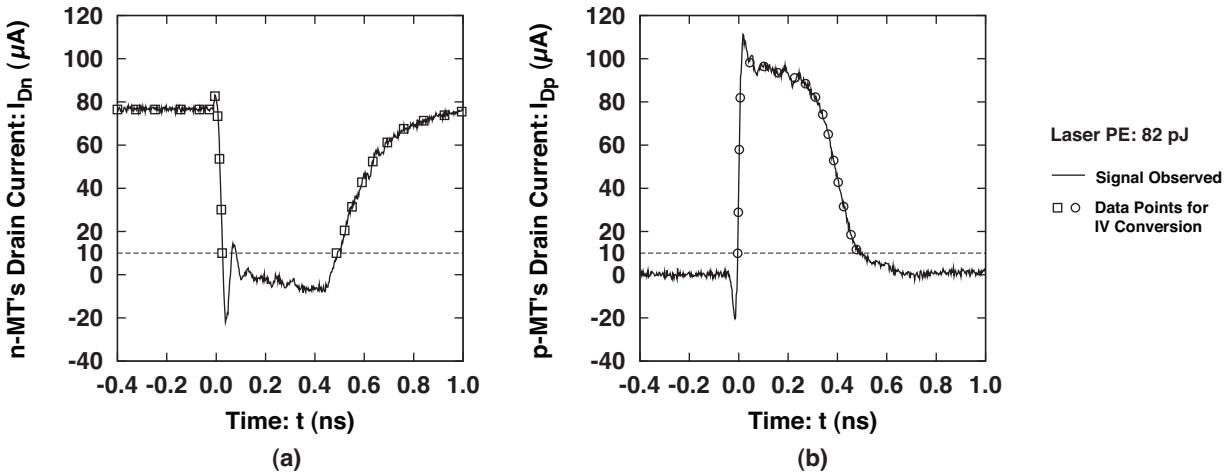

Fig. 5. I_D versus t curves measured through the n-MT (a) and p-MT (b) while the target inverter was irradiated by a 82-pJ pulsed-laser beam. In the conversion process, we used data points, which are represented by the symbols, for currents larger than 10 μA. See the text.

Gaussian spot was applied to the transistor with 1-ps duration at a 10-kHz repetition rate.

For comparison, we also measured transient drain-currents induced by irradiation in the single elementary n-type transistor M5. From the transients, we estimated DSET parameters using two techniques: on-current-based pulse-width estimation [16] and table-based waveform estimation [13], [28], [29].

IV. Results and Discussion

A. Validation

Fig. 5 shows the measured MT responses, I_D versus t curves, while the target inverter was irradiated by a 82-pJ pulsed-laser beam.

As expected, we observed complementary responses; i.e. the p-MT turned on while the n-MT turned off. The n-MT's steep falling edge and p-MT's rising one had a transit time of around 20 ps, which was close to the minimum transit time of 18 ps theoretically calculated for this 20-GHz system. Thus, the sharp edges were probably determined by the system. Because these slight edge deformations have little influence on the entire waveforms, we directly used data on the curves including the sharp edges.

Fig. 6 shows reference I_D versus V_G curves. In this test, the curves were obtained in a conventional static (dc) way, not in a dynamic (transient) manner. There are several factors that could possibly result in differences in the dynamic and static curves: the transit-time effect [30], floating-body-charge effect [31], channel-charge injection effect [32], and self-heating effect [14]. We theoretically examined these effects and concluded that the discrepancies between the static and dynamic curves were negligibly small when currents were significantly greater than those corresponding to the threshold voltages. This is the reason why we used data points for currents larger than 10 μA.

Fig. 7 shows a resultant V_O versus t curve; i.e. a DSET waveform. The open squares and circles represent the p-MT and n-MT responses, respectively. We also superimposed an estimated waveform from single transistor responses using

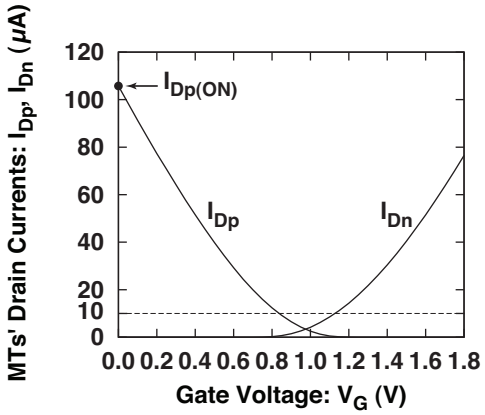

Fig. 6. Reference I_D versus V_G curves. The curves were measured with copies of the MTs, which copies were fabricated on the same chip. The value of $I_{Dp\,(\mathrm{ON})}$ is replotted in Fig. 9.

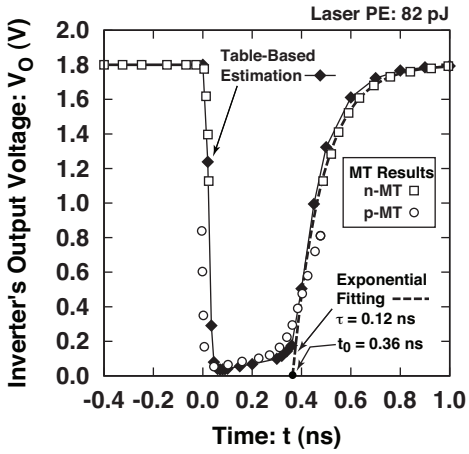

Fig. 7. DSET waveform (V_O versus t curve). The open squares and circles represent the p-MT and n-MT responses, respectively. The table-based estimation result (black lozenges) and exponential fitting line (dashed line) are also superimposed. The curve was fitted to the data points on the recovery tail observed through the n-MT and expressed as $V_O = 1.8\left[1 - \mathrm{e}^{-(t-t_0)/\tau}\right]$, where t_0 and τ were the fitting parameters and determined by the least square fitting technique.

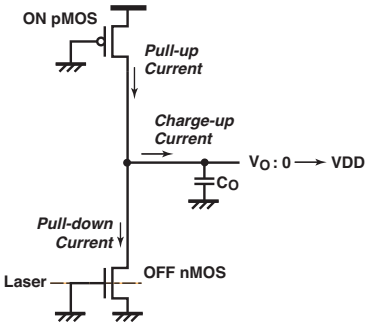

Fig. 8. Equivalent circuit model for waveform analysis.

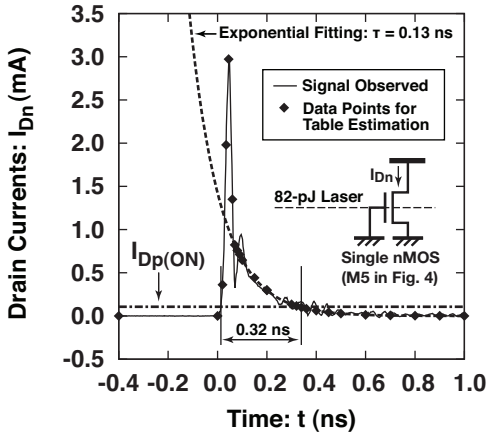

Fig. 9. Transient drain current induced by laser irradiation in the single n-type transistor (M5). The transistor was in an off-state when its gate was grounded and the drain was biased at a power supply voltage V_{DD} of 1.8 V. The laser pulse energy (PE) was 82 pJ. The on-current in the p-type transistor $I_{Dp\,(\mathrm{ON})}$ labeled in Fig. 6 and an exponential fitting line are superimposed. Symbols indicate the data points used in the table-based estimation. See also the appendix.

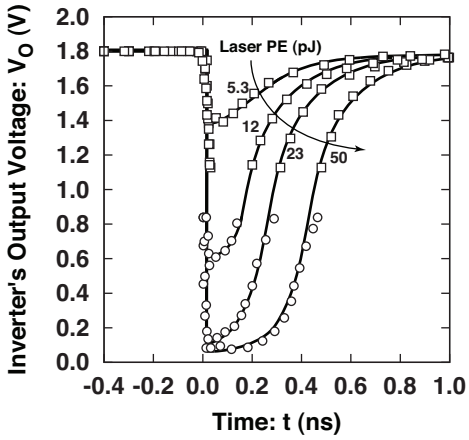

Fig. 10. DSET waveforms obtained when the target inverter was irradiated with various laser PEs.

the table-based approach [13], [28], [29]. Models used in this estimation are described in the appendix. Fairly good agreement was observed between the results from the MT technique and estimation. We found that the value of the root mean square error (RMSE) was small, 0.09 V, for the entire waveform except for the steep falling edge distorted due to the bandwidth limitations. We thus concluded the validity of our observation technique was demonstrated.

We also found that we can explain the slow recovery tail of the obtained waveform with an exponential line. Its time constant was 0.12 ns. We obtained another temporal parameter, the duration of the bottom of the pulse. This value was determined as 0.36 ns by reading the point where the fitting line crossed the horizontal axis ($V_O = 0$). We discuss these temporal parameters in the following section.

B. Waveform Analysis

As illustrated in Fig. 8, the recovery tail of the DSET is determined by a power balance between a pull-up current provided by the on-state p-type transistor, a pull-down current induced by irradiation in the n-type transistor, and a charge-up current for the output capacitance C_O.

Assuming the pull-down currents induced by irradiation were negligibly small, we obtained by SPICE simulations a quick recovery tail with a time constant of several tens of picoseconds, which is too short to explain the experimental result.

Fig. 9 shows a transient current induced by irradiation measured in the single elementary n-type transistor M5. It has a clear exponential decay with a time constant of 0.13 ns agreeing with the time constant of the DSET's recovery tail. We can thus conclude that the slow recovery tail of the DSET waveform observed in this test was determined by the slow decay of the pull-down current induced by irradiation. We would like to emphasize that we can perform such a detailed analysis because we have obtained the waveform entirely.

In addition, from Fig. 9, we read the temporal duration where the radiation-induced transient currents were larger than the on-current of the p-type transistor $I_{Dp\,(\mathrm{ON})}$. Ferlet-Cavrois *et al.* reported that such a duration well indicates a DSET width — more precisely, a bottom-width of the waveform as shown in their simulation result [16]. The resultant duration was 0.32 ns and matched the bottom-width of 0.36 ns in Fig. 7. This result also demonstrates the validity of our measurement technique.

C. Laser PE Dependency

Fig. 10 shows waveforms of DSETs under various laser pulse energy (PE) conditions. As reported in a simulation study by Dodd *et al.* [33], pulse widths broadened and bottom voltages became lower as the laser PE increased. The bottom of the pulse finally arrived and plateaued at the ground rail because a parasitic bipolar transistor turned into saturation mode [34]. Our technique experimentally revealed the DSET evolution as a function of the laser PE for the first time. We would like to report detailed discussions on this result elsewhere.

D. Circuit Variation: Single MT Approaches

In this paper, we used both p-type and n-type MTs to eliminate regions that are blind owing to their threshold effects.

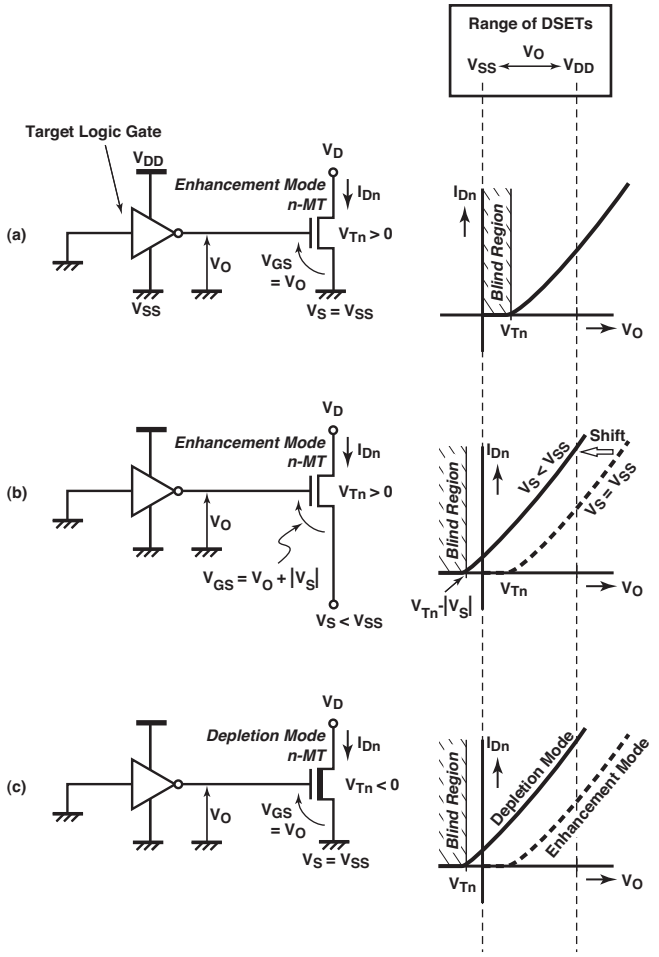

Fig. 11. Single MT approaches. The voltage swing of DSETs in SOI CMOS logic gates basically ranges from its power supply voltage V_{DD} to ground voltage V_{SS}; i.e. $V_{SS} \leq V_O \leq V_{DD}$. (a) circuit configuration used in this study. This is illustrated again for comparison. (b,c) single MT approaches. We can observe DSETs only with the single n-MT in the cases where it is possible to apply a negative voltage the magnitude of which is larger than $|V_{Tn}|$ to the source terminal of the enhancement mode n-MT or where a depletion mode (normally-on type) transistor is available for the n-MT.

We would like to mention that we can observe DSETs using only a single MT in some cases. Such single MT approaches are attractive for its simple circuit structure and measurement setup. Hereinafter, for simplicity, we would like to explain them taking an n-type MT for example.

The voltage swing of DSETs in SOI CMOS logic gates basically ranges from its power supply voltage V_{DD} to ground voltage V_{SS}; i.e. $V_{SS} \leq V_O \leq V_{DD}$. In our test circuit, as shown in Fig. 11(a), we used an enhancement mode ($V_{Tn} > 0$) transistor as the MT and its source voltage V_S was kept constant at V_{SS}. In this case, the gate-source voltage V_{GS} of the MT is equal to V_O and the MT turns off while V_O is smaller than V_{Tn}. As a result, a blind region existed within the DSET voltage region.

As illustrated in Fig. 11(b), however, we can observe DSETs only with the single enhancement-mode n-MT in the case where it is possible to apply a negative voltage the magnitude of which is larger than $|V_{Tn}|$ to its source terminal. The MT never turns off in the full DSET range because V_{GS}, which is given by $V_O + |V_S|$, is larger than V_{Tn} even when $V_O = V_{SS}$.

Fig. 11(c) depicts another single MT technique. When an n-type depletion mode ($V_{Tn} < 0$) transistor is available for the n-MT, the single MT approach is also possible because the depletion-mode n-MT has a negative threshold voltage.

E. Applicability to Heavy Ion Testing

The proposed MT technique is applicable, in principle, to heavy ion testing as well as the laser testing performed in this study. Unlike the laser testing, in which repetitive signals can be generated and measured by a sampling oscilloscope, we need to use a single-shot oscilloscope for the heavy ion testing. Its bandwidth has been increasing so that we can now measure ion-induced transient currents in today's advanced devices [16], [35].

From the viewpoint of circuit configuration, the double MT configuration has an advantage over the single MT type for heavy ion testing. In the case where we use the MT technique for heavy-ion broad-beam tests, heavy ions may hit not only a target logic gate but also an MT. Such MT hits produce unwanted current transients, which are recorded in the scope as well as DSET (logic-gate hit) signals. Using the double MT approach, we can eliminate these unwanted signals as in [10]. We can obtain only DSET information by selecting only the signals concurrently recorded by both MTs, because DSETs basically generate transient responses in both MTs whereas MT-hits produce signals only in the struck MT.

V. Conclusion

We have developed a new DSET observation technique. By connecting only two elementary transistors to a target logic gate, waveforms can be observed through a conventional 50-Ω transmission line system widely used for measuring transient currents in single transistors.

We fabricated test circuits in a fully depleted SOI process and carried out pulsed-laser irradiation tests. Fairly good agreement (RMSE = 0.09 V) was observed between the obtained waveform and the estimation results, thus demonstrating the validity of the proposed technique. In addition, our technique clearly revealed the DSET evolution as a function of the laser PE.

We also discussed the variations of circuit configurations for measurements and the applicability of our technique to heavy ion testing.

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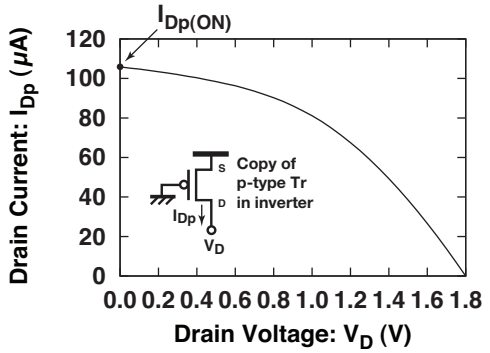

Fig. 12. I_D versus V_D curve for the p-type transistor in the target inverter. We fabricated a copy of the p-type transistor M1 and measured its drain currents as a function of the drain voltage.

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APPENDIX

We explain the models used in the table-based estimation. The circuit configuration was the same as that in Fig. 8.

For the on-state p-type transistor, we used the measured I_{Dp} versus V_D curve shown in Fig. 12. We implemented this curve with a piece-wise-linear-type voltage-controlled current-source.

We modeled the output capacitance C_O with a constant capacitance model. Its value of 4.4 fF was theoretically determined from design parameters of the MTs' gates and the metal interconnects between the target inverter's output and the two MT inputs. For calculating the interconnect capacitance, we used van der Meijs and Fokkema's empirical formula [36], [37].

For modeling the radiation responses of the n-type transistor, we used transient currents measured by 82-pJ irradiation in the single elementary transistor (M5 in Fig. 4) with various drain voltages. We changed the drain voltage from the ground to V_{DD} of 1.8 V in 0.2 V steps. We also used data for 0.01 and 0.02 V drain voltages. From a typical curve of the transient currents (Fig. 9), we read a sufficient number of data points and stored them in a look-up table.

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