IEEE Nuclear Science Symposium, Conference record, N34-4, Oct. 29 - Nov. 4, 2006, San Diego

Monolithic Pixel Detector in a 0.15µm SOI Technology

Y. Arai, *member, IEEE,* M. Hazumi, Y. Ikegami ,T. Kohriki, O. Tajima ,S. Terada, T. Tsuboyama , Y. Unno, H. Ushiroda, H. Ikeda, K. Hara, H. Ishino, T. Kawasaki, E. Martin, G. Varner, H. Tajima, M. Ohno, K. Fukuda, H. Komatsubara, J. Ida, H. Hayashi

***Abstract*– We describe a new pixel detector development project using a 0.15 µm fully-depleted CMOS SOI (Silicon-On-Insulator) technology. Additional processing steps for creating substrate implants and contacts to form sensor and electrode connections were developed for this SOI process. A diode Test Element Group and several test chips have been fabricated and evaluated. The pixel detectors are successfully operated and first images are taken and sensibility to β-rays is confirmed. Back gate effects on the top circuits are observed and discussed.**

I. Introduction

A monolithic pixel detector has been pursued for a long time, but has been difficult to implement due to the different silicon characteristics required for the radiation detector and for the readout electronics circuit. Recent advances in wafer bonding techniques [1] for SOI (Silicon-On-Insulator) technology enable us to use thick, high-resistivity Si and thin, low-resistivity Si on the same processed wafer.

Transistors fabricated on the SOI wafer have less parasitic capacitance compared with conventional bulk CMOS processes, enabling higher speed and lower power consumption circuits. Compared with hybrid pixel sensors [2], the SOI pixel detector does not require bump-bonding, thus a device with finer position resolution, less material and lower cost can be achieved.

Manuscript received Nobember 4, 2006. This work was supported by the KEK Detector Technology Development project.

Y. Arai (e-mail: yasuo.arai@kek.jp), M. Hazumi, Y. Ikegami, T. Kohriki, O. Tajima, S. Terada, T. Tsuboyama, N. Unno, and H. Ushiroda are with the IPNS, High Energy Accelerator Reserach Organization (KEK), Ibaraki 305-0801, JAPAN.

H. Ikeda is with the ISAS, Japan Aerospace Exploration Agency (JAXA), Kanagawa 229-8510, JAPAN.

K. Hara is with Institute of Pure and Applied Science, University of Tsukuba, Ibaraki 305-8571, JAPAN.

H. Ishino is with Department of Physics, Tokyo Institute of Technology, Tokyo 152-8551, JAPAN.

T. Kawasaki is with Graduate School of Science and Technology, Niigata University, Niigata 950-2181, JAPAN.

E. Martin, and G. Varner are with Department of Physics and Astronomy, University of Hawaii, Honolulu, HI 86822, USA.

H. Tajima is with Stanford Linear Accelerator Center, Stanford, CA 94307-4349, USA.

M. Ohno, K. Fukuda, H. Komatsubara, J. Ida, and H. Hayashi are with Oki Electric Industory Co. Ltd., Tokyo 193-8550, JAPAN.

SOI processes in general are known to be radiation hard and have been used in satellite instruments [3]. Furthermore, SOI is immune to latch up phenomena since each transistor is completely isolated with SiO_2, and there are no parasitic PNPN structures that can lead to latch-ups. Since the active transistor is very thin (~200 nm), there is very little charge generation in it, making it less sensitive to Single Event Upsets and Transients [4]. Due to ionization radiation damage, the transistors may have larger leakage current, though this can be mitigated by proper layout, which removes the leakage path [5].

We have started an SOI pixel detector [6, 7] development in collaboration with OKI Electric Industry Co. Ltd. in the summer of 2005. The basic technology for fabricating the pixel detector is OKI's fully-depleted 0.15µm CMOS SOI process [8]. Additional processing steps to create substrate implants and contacts were developed.

Fig. 1 illustrates a cross-section of the basic pixel detector structure we employed. Several TEG (Test Element Group) chips were designed and fabricated. Detailed structure and test results are described in the following sections.

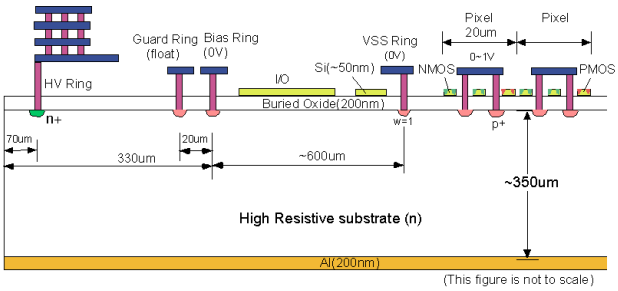

Fig. 1 Cross-sectional view of the SOI pixel detector (n-type substrate shown).

II. Process Development

A. SOI Process

The characteristics of our SOI process are summarized in Table 1. We used an SOI wafer of low resistivity p-type Si on top, and a high resistivity (>1 kΩ•cm) Si layer (called handle wafer or substrate) on the bottom. The

wafer manufacturer provides no type assignment for the handle wafer. In addition, type change could occur during processing, such as thermal donor generation by oxide contamination. Therefore we designed two kinds of TEG chips to work with p-type or n-type substrates.

Masks for the process are shared with other users (Multi Project Wafer) to reduce costs. To create p+ and n+ implants and contacts, we needed additional 3 masks.

Implantation of p+/n+ to the substrate is performed after cutting the BOX layer. The implant was done at the same time as formation of the transistor drain/source region (carrier density of ~10^{20} cm^{-3}) so as not to increase the number of masks and process steps.

The backside is ground mechanically from 650 µm to 350 µm, then plated with 200nm of aluminum. Detector voltage can be applied both from bottom and top pads, which are connected to a HV n+ implant ring.

There are 3 kinds of transistors in this SOI process; high voltage (for I/O purposes), high threshold (for normal logic), and low threshold (for high speed circuit) transistors. There are two types of body control in each transistor; floating body and body tie. High threshold transistors with body ties are used in the pixel circuit, while I/O transistors are used in the I/O buffers.

Table 1. Features of the OKI SOI CMOS process

Process	0.15µm Fully-Depleted SOI CMOS process, 1 Poly, 5 Metal layers.
SOI wafer	Diameter: 150 mmϕ Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz、>1k Ω-cm (*No type assignment by supplier)*, 650 µm thick (SOITEC)
Backside	Thinned to 350 µm, and plated with Al (200 nm).
p+/n+ Implant	simultaneous with drain/source formation
Supply Voltage	Core 1V, I/O 1~1.8V
Transistors	High Voltage Tr (I/O), High Threshold Tr, Low Threshold Tr. Floating body and body tie.

B. Diode TEG

Prior to processing pixel TEG chips, we have fabricated diode TEG with p+/n+ implants and contacts, and measured their characteristics.

Fig. 2 shows a TEM photograph of the cross section of the p+ implant to the substrate and contact to the 1st metal layer. Sheet resistance of the p+ (n+) implant is measured to be 136 (33) Ω/square, and the resistance of the 0.16 x 0.16 μm^2 contact to the p+ (n+) implant is 218 (87) Ω. These values agreed with expectation.

From I-V measurements of the diode TEG (Fig. 3), we determined that the substrate is n-type, and that backside wafer resistivity, measured with a 4-points probe, is about 700 Ω•cm (carrier density ~ 6 x 10^{12} cm^{-3}).

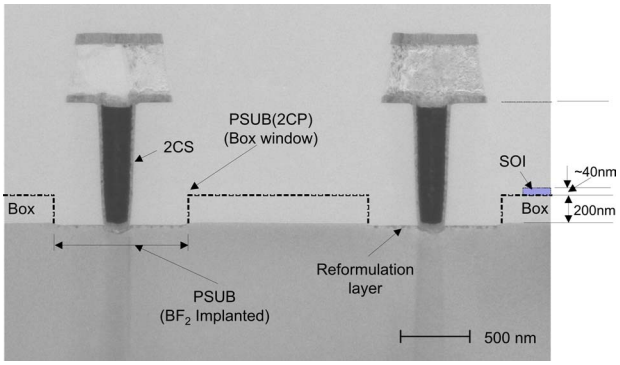

Fig. 2. TEM photograph of the p+ implant and contact cross section.

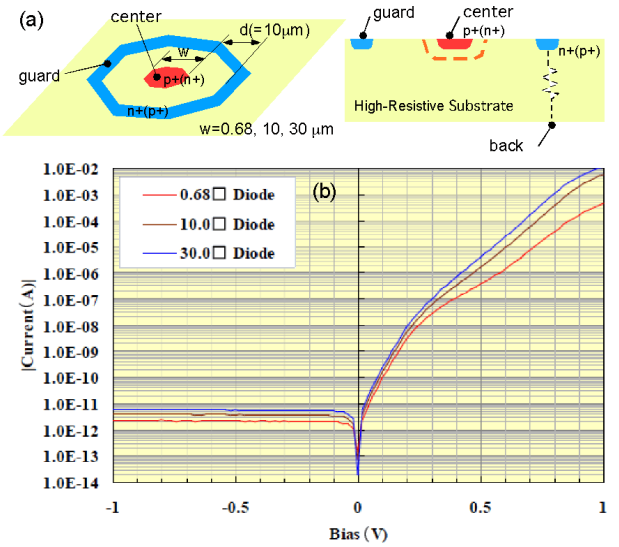

Fig. 3. (a) Structure of diode TEG, (b) I-V characteristics of the diode (p+ and backside) TEG for three different diode sizes.

III. PIXEL TEG

A block diagram and photograph of the pixel detector is shown in Fig. 5. Each pixel is 20 µm by 20 µm in size and an array of 32 x 32 of them are implemented. The pixel readout circuit is a standard active pixel type with a storage capacitor. At the periphery are row and column selects, control logic, and reference voltage generator circuits.

Layout of a single pixel cell is shown in Fig. 4. The center of each pixel (5.4 µm x 5.4 µm) is open (no metal)

to allow light illumination testing. Four p+(n+) junctions are implemented in each pixel, with each junction of octagonal shape and a width of 4.4 µm.

A. I-V Characteristics

I-V characteristics of the detector are shown in Fig. 6. Voltage is applied from the backside Al pad. Almost the same characteristics are obtained using the HV ring pad. We could apply up to 98V without breakdown. This corresponds to about a 140µm depletion depth assuming the 6 x 10^{12} cm^{-3} carrier density. We observed the chip with an infrared camera and found hot spots in the corners of the bias ring (see Fig. 1). This can be easily amended by smoothing the corner of the ring.

Due to the back gate effect, which will be discussed in the next section, detector voltage operation is limited to a much lower value to permit electronic circuit operation.

B. Light Test

Using the pixel detector, we took images of a plastic mask placed in front of the detector by illuminating red laser light (670 nm wavelength). One such image is shown in Fig. 7. Detector bias voltage is 10V and the integration time is 7 µs. Pedestal voltages soon after the reset are subtracted in each pixel. This reduces fixed pattern noise due to the column amplifiers. Good contrast implies good signal separation between neighboring pixels. Collected signal in the white (saturated) part of the pixel is estimated to be about 20,000 photons from laser intensity and pixel geometry. Pixel capacitance is estimated as roughly 8 fF, so the induced voltage of the sensor node is about 400 mV. This is consistent with the observed signal amplitude.

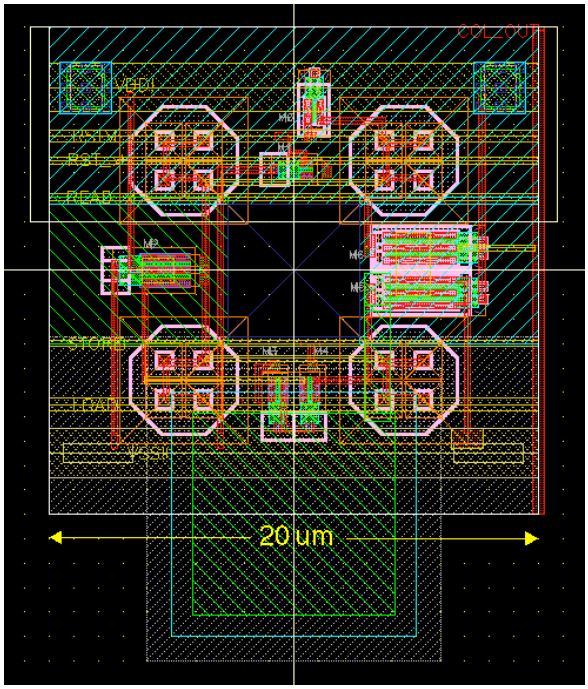

Fig. 4. Layout of a pixel cell. Each pixel has 4 p+(n+) implants of octagonal shape. At the lower middle of the cell is the storage capacitor. The pixel center is left free of metal to allow light illumination testing.

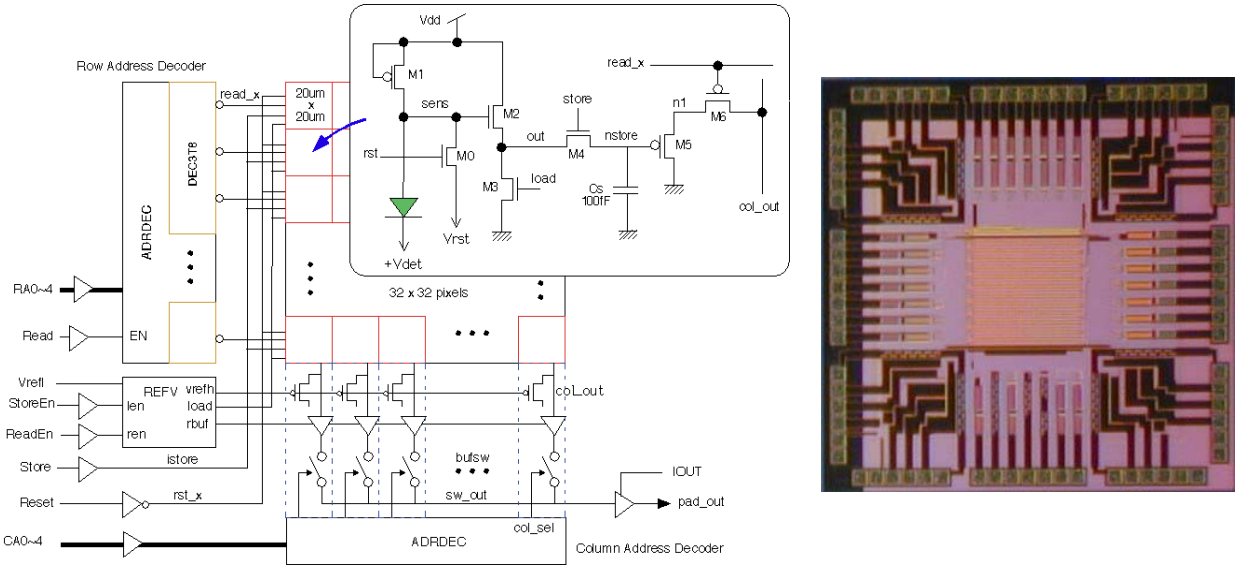

Fig. 5. Block diagram (left) and photograph (right) of the pixel detector. Pixel size is 20 µm by 20 µm, arranged into a 32 x 32 array of pixels. Chip size is 2.5 mm by 2.5 mm.

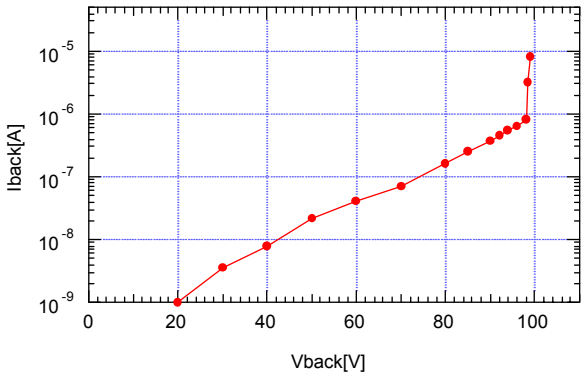

Fig. 6. Vback - Iback characteristic of the pixel detector.

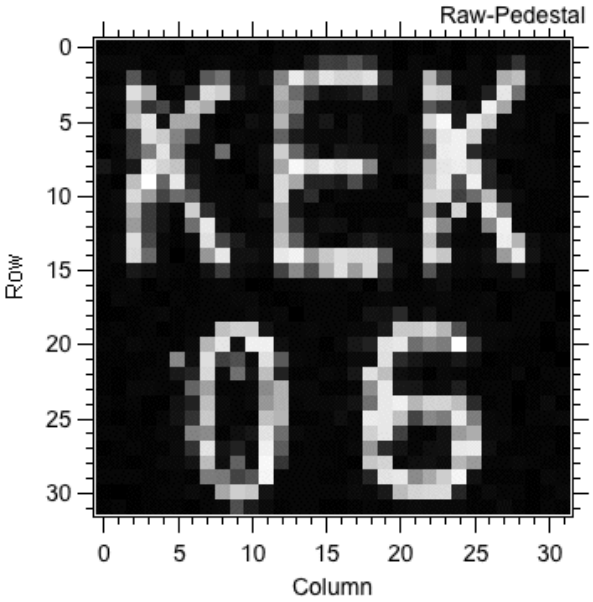

Fig. 7. An image taken by the pixel sensor with a 'KEK06' mask. Exposure time is 7 μs, and detector bias voltage is 10V.

C. β-ray measurement

We confirmed the sensitivity to b-rays by using ^{90}Sr β-ray source. Fig. 8 shows output signal of a pixel when β-ray is irradiated. Clear signal jump is observed. The voltage jump corresponds to an increase of 70mV in the sensor. This is consistent with the depletion depth of 44 μm and generated charge of 3500 e (0.6 fC).

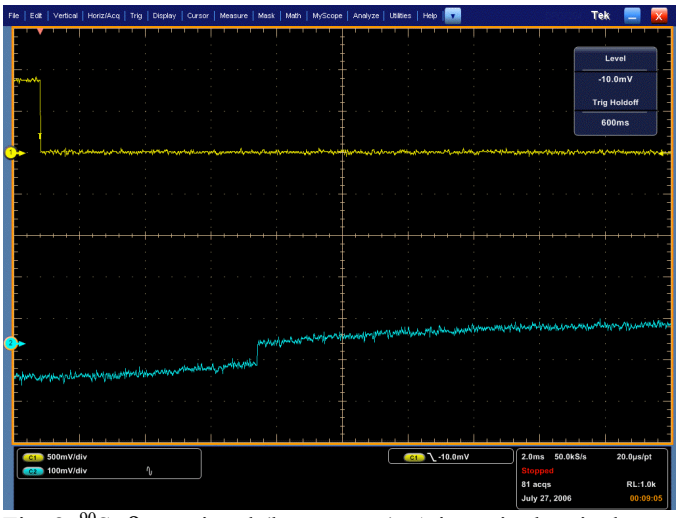

Fig. 8. ^{90}Sr β-ray signal (lower trace). A jump in the pixel output signal shows the β-ray signal. Upper trace is a reset signal. Horizontal scale is 2msec/div. Gradual increase of baseline is due to leakage current.

D. Back Gate Effect

The potential under the BOX acts as a back gate of the transistors in the top Si. Threshold shifts due to this back gate voltage are plotted in Fig. 9. As the back gate voltage is increased, the threshold voltage of NMOS transistors are decreased and that of PMOS are increased. Finally the circuit stops working for excessive back gate voltage.

This is confirmed in the TEG chip by observing an input-output signal of the I/O buffers where no p+ implant exists so the detector voltage is applied to the back gate. The output signal from an input buffer is directly connected to the input of an output buffer. Waveforms of the input-output buffer are shown in Fig. 10. The output waveform amplitude becomes small when the back gate voltage exceeds 15V. This is also confirmed with SPICE simulation using the threshold shifts shown in Fig. 9.

To circumvent this back gate effect, we should make p+ implant to the substrate and connect them to the ground level to keep the back gate potential low enough.

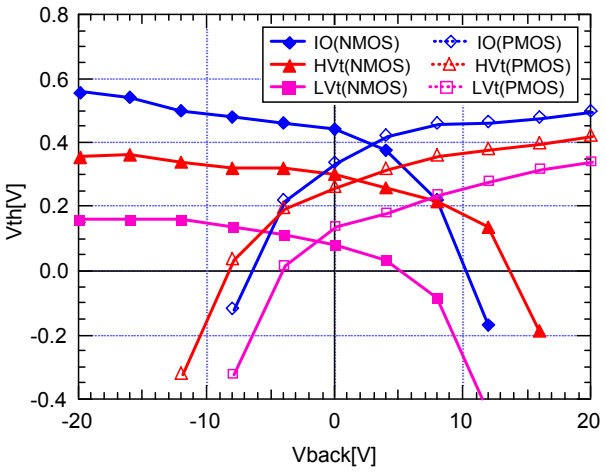

Fig. 9. Measured threshold Voltage (Vth) shifts due to back gate voltage (Vback) for NMOS and PMOS transistors of the three different types available.

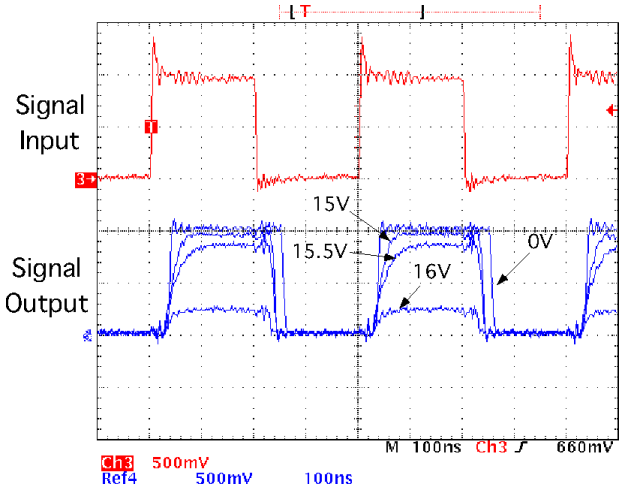

Fig. 10. Output signal variation due to the back gate voltage. The input buffer signal is directly connected to an output buffer inside the chip. With a back gate voltage of 16V, the output signal is reduced to one fifth of its original amplitude.

IV. SUMMARY

We have started a development of a monolithic SOI pixel detector. The detector consists of a wafer-bonded sensor in high-resistivity Si mated to a CMOS circuit in low-resistivity Si. We use a commercial (OKI 0.15 μm SOI) process with commercial wafers (SOITEC Hi-R) by adding only 3 additional masks.

Good substrate contacts and p-n junctions are confirmed. We have determined that the handle wafer is 'n' type, and has sufficient resistivity for radiation detection. Several TEG chips have been fabricated and tested. By illuminating light through a mask we successfully obtained a first image with this pixel detector. Furthermore, we also observed expected signal for the β-ray irradiation.

The SOI pixel detector has many good features, such as fine segmentation, low material thickness, good radiation hardness, and low power consumption. In addition, lower cost compared with hybrid pixel detector can be expected. Our results demonstrate a great potential for future high energy physics and satellite experiments.

ACKNOWLEDGMENT

The authors wish to thank F. Takasaki, T. Kondo and J. Haba for their continuing support to this project. We are also grateful to Y. Sugimoto and K. Hirose for their fruitful discussions.

REFERENCES

[1] SOITEC, http://www.soitec.com/
[2] X. Llopart et al., "Medipix2: a 64-k Pixel Readout Chip With 55-um Square Elements Working in Single Photon Counting Mode", IEEE Trans. Nucl. Sci., Vol. 49, (2002)2279-2283.
[3] J. R. Schwank, V. Ferlet-Cavrois, M. R. Shaneyfelt, P. Paillet, and P. E. Dodd, "Radiation Effects in SOI Technologies", IEEE Trans. on Nucl. Sci., Vol. 50, (2003) 522-538.
[4] A. Makihara et al., "Hardness-by-Design Approach for 0.15 mm Fully Depleted CMOS/SOI Digital Logic Devices With Enhanced SEU/SET Immunity", IEEE Trans. on Nucl. Sci. Vol. 52 (2005) 2524-2530.
[5] B. W. Offord and J. S. Ruthberg, "Radiation-Hardened Silicon-on-Insulator 0.8-um Technology Design Rules", Technical Document 3065, 1999, http://www.spawar.navy.mil/sti/publications/pubs/td/3065/td3065.pdf
[6] SOI Pixel detector R&D, http://rd.kek.jp/project/soi/
[7] Y. Arai et al., "First Results of 0.15um CMOS SOI Pixel Detector", SLAC Electronic Conference Proceedings Archive. http://www.slac.stanford.edu/econf/C0604032/papers/0016.PDF
[8] K. Morikawa and M. Mitarashi, "Low-Power LSI technology of 0.15 um FD-SOI", OKI Technical Review Issue 196, Vol. 70, No. 4, pp. 60-63, Oct. 2003. http://www.oki.com/en/otr/196/downloads/otr-196-R15.pdf