Ingrid devices for UV photon detection

Joost Melai
MESA+ institute for Nanotechnology, University of Twente, the Netherlands
in collaboration with the Weizmann Institute of Science, Rehovot, Israel
and NIKHEF, Amsterdam, the Netherlands
Overview

• Post-Processing on CMOS
• InGrid concept and technology
• InGrid performance
• Photon detection, photocathodes on InGrid
• Experimental results
  – Charge pulses
  – Imaging
• Summary and outlook
The beginning of Moore’s law

CMOS

Oxide

Metal

N+ P

N+ P+

P+ N

Semiconductor

NMOS PMOS

Source: www.intel.com

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The state of the art: CMOS

- Nanometer precision
- Sub-ppm materials purity
The state of the art: DRAM

- 58-nm DRAM technology

- Nanometer precision
- Sub-ppm materials purity
Moore’s law
More Moore and More than Moore

Source: ENIAC

Industry & academia

Industry & academia

Industry
Post-processing CMOS

- Chip fabrication: standard, at any regular (CMOS) fab
- Post-processing: special, in a custom CR laboratory
- Wafer dicing, packaging: specialized work like MEMS packaging, e.g. Amkor, Boschman
Pros and cons

• We do not interfere with the (CMOS) fab process
• We can buy good quality chips
• We can use any lab for this
• We must keep the CMOS intact
• We have to think the final stages through very carefully!

→ Flexible for R&D; potential for mass-scale manufacturing
Example: Liquid-Crystal-on-Silicon
Example: Digital MicroMirror™

Texas Instruments (1987), used in every DLP projector
Samsung CMOS image sensor
Micro lenses and color filters
Rohmcorp.: CIGS image sensor on CMOS (IEDM 2008)

[Image of CIGS image sensor layers and micrographs]

1. ZnO
2. CdS
3. CIGS
4. Mo

Pixel
Photodiode
LSI circuits

(a) CIF type
(b) VGA type
CMOS on top of CMOS!
3D integration

T ≤ 450 °C

B. Rajendran et al.,

I. Brunets et al.,
IEEE Trans. El. Dev. 56 (8) 1637

A. W. Topol et al.,
IBM J. Res. & Dev. 50 (4/5) 491

Stacking of active device regions
→ new technology
CMOS post-processing

Careful treatment of the underlying CMOS:

• Temperature $\leq 450 ^\circ C$
• Mild (or no) plasmas
• Maintain the H balance in the MOSFET
• Limited mechanical stress
• Prevent material contamination (spec. metals)

The CMOS properties must be unchanged:
then the standard infrastructure can be used
Overview

• Post-Processing on CMOS
  – Can we also miniaturize the MWPC?
  – Can we use CMOS as the readout anode?

→ InGrid concept and technology
→ InGrid performance
Overview

• Post-Processing on CMOS
  – Can we also miniaturize the MWPC?
  – Can we use CMOS as the readout anode?

→ InGrid concept and technology
→ InGrid performance

• Detector elements
  – The chip: Timepix
  – The MPGD: grid and pillars
TimePix
variation of Medipix2,
designed by the Medipix2
collaboration headed by CERN

- 256 × 256 pixels of 55 × 55 μm², charge sensitive
- Different readout modes:
  - MediPix mode: nr of hits per pixel
  - TimePix mode: time of arrival within shutter window
  - TOT mode: estimation of total charge per pixel
- 0.25 μm CMOS, size 14 × 16 mm
- Post-processing done on chip level or multi-chip cluster level
SiRN: New anti-spark material

- Sparks cause permanent damage
- Originally a-Si:H, now Si-rich Nitride
- $\text{Si}_3\text{N}_4$ typical anti-scratch layer on CMOS
- SiRN, excess of Si to tune resistivity and mechanical stress
- Deposited by PECVD at 300 °C or lower
Spark protection

• Protection layer quenches discharges, removing the built up E-field
• Signal still fast by induced mirror charge
• Timepix with 7.2 μmSiRN + InGrid
• Operation in Ar/Iso 80/20, with alphaparticles induce sparks
• No damage observed, spark protection is effective
InGrid: postprocessed Micromegas

- Metal grid (Al) supported by insulating pillars (SU-8)
- Pillars in the middle of four pixels
- Perfect alignment hole to pixel, pillar to pixel
- Arbitrary hole geometry
- Integrated MPGD: Micro Patterned Gaseous Detector
InGrid: Integrated Grid

1) Pre-process chip
2) Spin SU-8
3) UV exposure
4) Deposit metal
5) Pattern metal
6) Develop resist

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SU-8 material

• Negative tone photoresist (developed by IBM Research)
• Polymer based (EPON SU-8 from Shell Chemical)

Available in many viscosities
Thickness ranges from 1 to 1000 µm
Processing similar to normal UV lithography
Examples of SU-8 use

• Permanent, high aspect ratio structures

Krijnen et al., MESA+, UT

Conradie et al., (Cambridge univ.)
J. Micromech. and Microeng. 12 (2002)
Examples of SU-8 use

• Bio compatibility: lab-on-a-chip applications

• Multiple layers of patterned SU-8 alternative to bonding

B. Xue 
(Unev. Shanghai)
Examples of SU-8 use

- SU-8 removal using a lift-off layer
- A stencil mask made in SU-8

G. Kim et al. (MESA+, UT), Sensors and Actuators A 107 (2003)

- SU-8 as plating mold → cheap, fast, UV LIGA

L. Jian et al. (Louisiana State Univ.), SPIE vol. 4979 (2003)
DS of SU-8 mesa capacitor structures

SiO$_2$: 0.8–1 kV/µm

SU-8: 443 ± 16 V/µm

Kapton-N: 270 V/µm

MCP: ≤ 100 V/µm

MPGD: ≤ 10–20 V/µm
Outgassing from SU-8

- Outgassing rate comparable to Kapton
- 20–30 min Hard-Bake $\rightarrow$ efficient pre-conditioning
- Components directly linked to resist formulation

$T = 150 \, ^\circ \text{C}$
Overview

• InGrid, integrated MPGD

→ Capabilities of InGrid
→ InGrid for photon detection
Chip bonding

- Finish post-processing
- Attach chip (w/ InGrid) to board
- Wirebonding of connections
- Mount chamber onto board

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InGrid performance

- High single e\(^{-}\) collection efficiency (> 90% at G=10\(^4\)), set by field-ratio
- Good energy resolution (11.7% FWHM for \(^{55}\)Fe in Ar/CH\(_4\))
- 2D and 3D tracking of MIPs etc
- Different device designs, Micromegas, GEM, multiple electrodes
Gain in Ar/iso-Butane mixtures

Typical threshold level, $2 - 3 \cdot 10^3$

From the thesis of Max Chefdeville (NIKHEF)
Homogeneous response

Separately mounted Micromegas as Post-processed InGrid

Microlithography $\rightarrow$ alignment tolerance (few $\mu$m)
$\rightarrow$ alignment between pixels and grid (55 $\mu$m pitch)
$\rightarrow$ no more Moiré patterns
Two $^{90}$Sr tracks in a B field
Recorded with a 3 cm Timepix TPC

Courtesy: Martin Fransen and Lucie de Nooij, NIKHEF
InGrid for photon detection

• Aim: complete integration of a UV photon sensitive detector
• Based on InGrid technology
• High resolution, high sensitivity, high rate
• Photocathode deposited after chip bonding
Set-up for photon detection

- Si-nitride spark protection of 8 μm
- Typical InGrid: 80 μm gap, 25 μm holes (OT: 19%)
- GOSSIP/NEXT chamber, USB readout
- CsI is deposited by thermal evaporation, after chip is processed and mounted on board
Operation principle of a light sensitive InGrid

Steel mesh

Al grid, 200 nm CsI pillars

TimePix chip

Low field: transfer
High field: multiplication

readout

pixel n pixel n+1
Extraction of primary electrons into He/isobutane

- He shows increased backscattering (compared to Ar)
- Addition of quencher (isobutane) restores yield (partially)
- High concentration of isobutane leads to UV absorption
Ion Back Flow (IBF) measurement

IBF:
Fraction of anode current that flows back to cathode (as ions)

Ions can damage photocathode (surface reactions)

Options for reduction

• Optimization of geometry, field ratio, gas
  Saclay (Colas et al.) reported IBF ~ 0.001

• Multistage structures (IBF not known)
UV pulses measured on grid

- UV or Fe 55 irradiation
- mesh cathode
- grid with PC
- Timepix
- Pulse readout (MCA)

- He/isobutane (80/20), Al grid with 200 nm CsI
- Distribution $G(Q) \propto C \cdot 1/G \cdot \exp(-Q/G)$
- Fit to distribution $\rightarrow$ extract $G(V)$
Gain of InGrid device with PC

- UV or Fe 55 irradiation
- mesh cathode
- grid with PC
- Timepix
- Pulse readout (MCA)

- He/isobutane (80/20), Al grid with 200 nm CsI, 80 μm gap height, 25 μm hole size
- slope ≈ 100–110 V/dec, max. gain ≈ 7 \cdot 10^4
Spectra with and without CsI

→ No increase in (photon) feedback
Determining spatial resolution using slanted edge method

Select ROI

Correct using open frame
Determining spatial resolution using slanted edge method

Select ROI

Correct using open frame

Find edge using derivation for all lines and fit a line

Shift line data accordingly
Determining spatial resolution using slanted edge method

1. Select ROI
2. Correct using open frame
3. Find edge using derivation for all lines and fit a line
4. Shift line data accordingly
5. Resample into 1 ESF
6. Calculate LSF
7. Determine resolution
Determining spatial resolution using slanted edge method

Fit to LSF:
- Gaussian with $\sigma = 0.48$ pixel = 26.4 $\mu$m
- FWHM = 1.13 pixel = 62.2 $\mu$m

Fourier transformation of LSF $\rightarrow$ MTF
MTF calculated from LSF

- MTF50 = 0.4 lp/pixel (≈ 7 lp/mm)
- Limit ≈ 0.8 lp/pixel (≈ 14 lp/mm)
- Resolution < pixel size (MTF = 0.32 @ f_{Nyquist})
Influence of cathode mesh

Mesh modulates light → non-uniform response, but also indication of resolution

Pixel pitch = 55 μm

Fine mesh (56 μm) → Moiré pattern

Coarse mesh (500 μm) → Mesh is imaged

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More images

Siemens star

Vertical stripes

Logo of the University of Twente

Fingerprint on window

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**Conclusions**

- Post processing combines CMOS strengths with MEMS flexibility
- SU-8 pillars and Al grid allow integration of MPGD on CMOS readout
- CsI deposition on InGrid successful, CsIPC works on InGrid
- Timepix fully operational with PC

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Conclusions

Successful integration of MPGD and PC on CMOS imaging chip:

- No photon feedback observed
- IBF $\approx 0.02$
- Max gain $\approx 7 \cdot 10^4$
- UV photon imaging capability demonstrated, external cathode mesh
- Spatial resolution is very good, FWHM of LSF is 62 $\mu$m, resolution limit above $f_{\text{Nyquist}}$
Outlook

• Qualitative measurement of QE
• Multistage structures for better IBF
• Other photocathodes
• Spectroscopic capabilities of Timepix TOT readout-mode
• Other grid materials (spark protection)
• Technological limits, alignment and feature size
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Questions
Dependence on drift field

- TOT count of full frame (in cps)
Gain curve based on TOT count

- Fe55: 99 V/dec; TOT: 117 V/dec
TwinGrid

multistage structure to reduce IBF, increase gain
Detector geometries

- Hole pitch variation:
  20 - 32 - 45 - 58 μm
- 20 & 32 μm pitch: pillars inside holes
- 45 & 58 μm pitch: pillars between holes
- Hole pitch/diameter variation: ratio 1.5 - 2.0 - 3.0 (hole sizes from 7 - 38 μm)
- Amplification gap set by SU-8 thickness, variable with spin speed