How to Deliver Very Large Amounts of Low Voltage Current to HEP Detectors in High Radiation & Magnetic Fields?

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When the current generations of detectors were planned, there was no consideration given to DC power distribution to the FE electronics. LHC detectors use linear regulators with power supplies located in a safe environment at distances of ATLAS 140 meters and CMS 30 meters. A 30% power delivery was acceptable. For the next generation of detector being designed with 0.13 μm lithography, the operating voltage is ~ 1 V. This results in delivery efficiency of 10%.

Plan delivering power at x10 higher voltage and propose to use DC-DC Converters on the same PCB as the FE ASIC chips. These have to operate in radiation of up to 100 Mrads, magnetic fields of 5T and produce very low noise.

We explore commercial (COTS) technology for DC-DC converter Chips suitable for use with air core inductors. The latter requirement is unique to HEP because of the high magnetic field.

For the SiD detector powering, we are exploring techniques that shall minimize the material in the active region.

Locating Converter chips next to load, power supply current reduction
Factor 10 with Silicon technology.
Factor 50 with Gallium Nitride FET switches.
Since Cable losses are $(\text{current})^2$ x Cable Resistance. Power supply delivery efficiency in typical LHC detectors can be doubled.

Summary

DC-DC Converter Plug in cards with air coils have been developed and tested. Two different commercial chips are used; one is monolithic while the other is a 3 die MCM (multi chip module). MCM can have optimized version of the FET switches for the high and low side with a separate converter chip. All three can be fabricated with different technologies and in principle have better performance. However the radiation results can be difficult to understand. One of the purposes was to see if the noise was more with the MCM monolithic converter; it does not seem to be the case.

The above converter chips are not radiation resistant. We are to study the conducted and radiated noise with the noise with the KPiX chip printed circuit boards. When tested with the ATLAS Silicon tracker and RHIC Polarimeter detector, there was no additional noise due to the close proximity of these cards while also supplying power to the readout chips. There is radiated noise to the silicon strips that can be made negligible by using 20 μm of Al shield.

Initial power pulsing tests have been done with an electronic load. A National semiconductor application engineer is looking into simulating SiD conditions to obtain faster switching with smaller output capacitors.

Our investigation has lead to technology for radiation resistant LDMOS CMOS devices at 12 -20 volts while using thin oxide of 5 -7 nm. Two foundries have been identified and verified.
Our focus is on commercial devices as there are very little power device ASIC design capability available in the US HEP community.

Gallium Nitride devices offer high frequency and very high radiation resistance as some of the transistor structures do not use oxide insulator.