R&D on Counting Pixel Chips

Yunpeng Lu

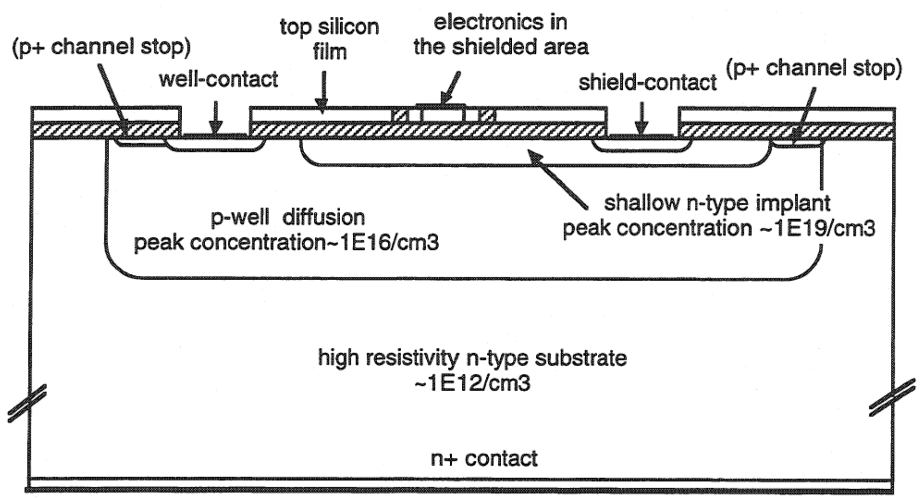
Outline

- Motivation
- Fundamental Issues
- Current Mirror & Amp-Sha-Disc
- Nested-Wells & DSOI
- Summary

Motivation(1)

- Shielding is a key issue in SOI Pixel Technology, and Counting Pixel is an effective measure to study it.
  - Necessity of shielding was recognized and understood by F. X. Pengg
  - Integrating pixel works fine with BPW suppressing back gate effect

  (Why no charge injection observed? Slow slew rate/ Cancelled by integration?)
  - But in counting pixel, charge injection messed up the counting results.



Figure(2.11a): The n+-p-n- structure of shield and well in the high resistivity substrate, cut.

Shielding-well proposed by F. X. Pengg in his dissertation "Monolithic Silicon Pixel Detectors in SOI Technology"

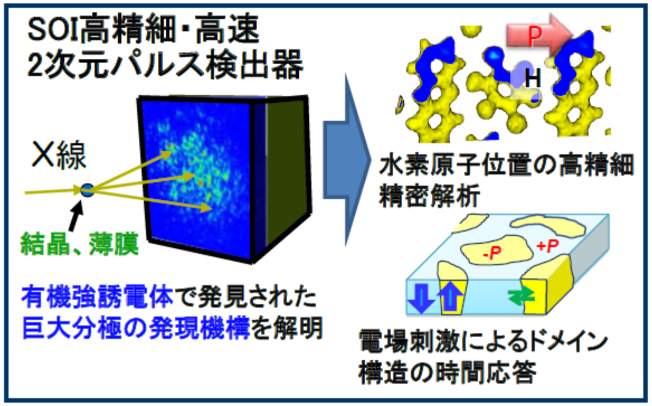
Good concept but not implemented successfully.

Motivation(2)

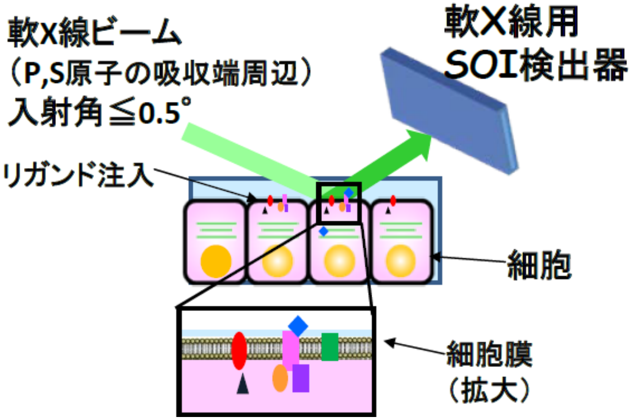
- Counting Pixel is getting more and more popular in synchrotron radiation application.
- Particularly interested in the area detector proposed by Prof. Kishimoto.
  - 30 um^2 pixel size
  - 1k frames/s
  - 14 bit counter
  - Low energy X-ray 2~4 keV

Very compact pixel circuit and good S/N required!

Ferroelectricity in a molecular crystal



Structure change of a cell membrane



Fundamental Issues

- On-chip circuit
  - Amp-Sha-Disc system
  - Counter and register in pixel
- Shielding
  - Nested-wells
  - Double SOI
- Leakage current
  - Low temperature would mitigate it
- Radiation damage
  - Should be fine if back-illuminated by low energy X-ray

Review of CPIXTEG2 results

- ✓ Amp-Sha-Disc system
- ✓ Counter and Register
- ✓ Bias and Aobuf
- • Current Source variation
- ✓ Shielding between analog and sense node
- ✓ Response of Light stimulus
- • Shielding between counter and sense node not reported

A-R-Tec Confidential
2012/3/19 大本・今村

測定実施TEG一覧

N基板用及び{N,P}基板共用TEG

TEG種別	TEG番号	チップID番号 1	2	3	4	5	コメント
pixel array	PA-1C N	○					レジスタ(CSR,DATA)読み書き確認のみ
	PA-2C N	○					レジスタ(CSR,DATA)読み書き確認のみ
cross-talk	0-1C N	○					
	0-2C N	○					
	0-3C N	○					
	0-4C N	○					
preamp+ shaper+ discri	1-1C N	○					
	1-2C N	○					
	1-3C N	○					
	1-4C N	○					
	1-5C N	○					
preamp+ shaper	2-1C N	○	○				
	2-2C N	○	○				
	2-3C N	○	○				
	2-4C N	○	○				
	2-5C N	○	○				
preamp	3-1C N	○	○	○			
	3-2C N	○	○	○			
	3-3C N	○	○	○			
shaper	4-1C	○					TEGアレイ中のshaper(TEG1X,2X)の測定でshaperの特性を評価
	4-4C	○					
discri	5-1C N	○	○	○			
aobuf		○	○	○	○	○	
bias		○	○	○	○	○	

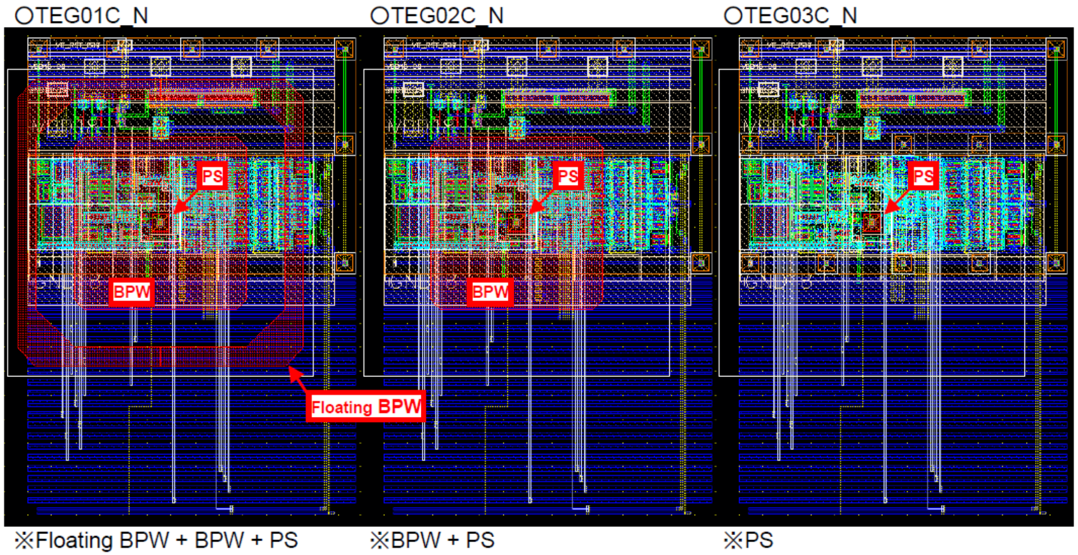
P基板用TEG

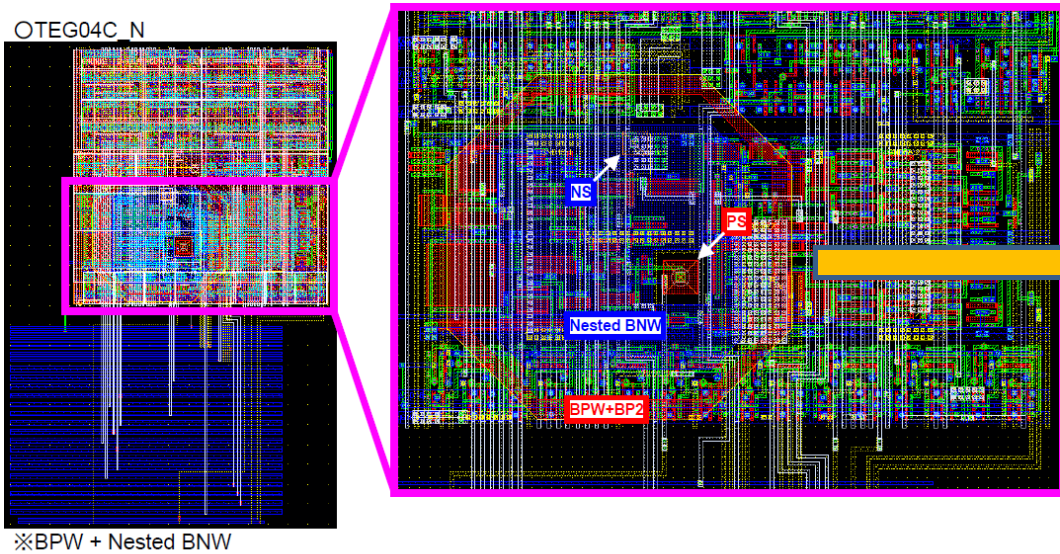
TEG種別	TEG番号	チップID番号 1	2	3	4	5	コメント
pixel array	PA-1C P	○					レジスタ(CSR,DATA)読み書き確認のみ
	PA-2C P	○					レジスタ(CSR,DATA)読み書き確認のみ
cross-talk							
preamp+ shaper+ discri	1-1C P						
	1-2C P						
	1-3C P						
	1-4C P						
	1-5C P						
preamp+ shaper	2-1C P						
	2-2C P						
	2-3C P						
	2-4C P						
	2-5C P						
preamp	3-1C P						
	3-2C P						
	3-3C P						
shaper							
discri	5-1C P	○	○	○			
aobuf							
bias							

Continuing efforts of Nested-wells on CPIXTEG3

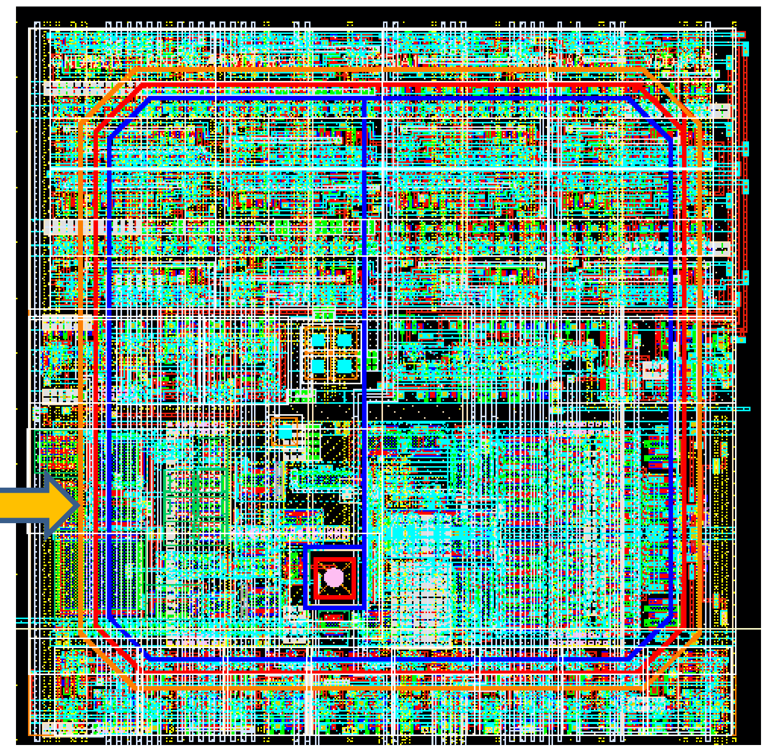
New nested-wells layout:

- Expand to full pixel
- More BNW contacts



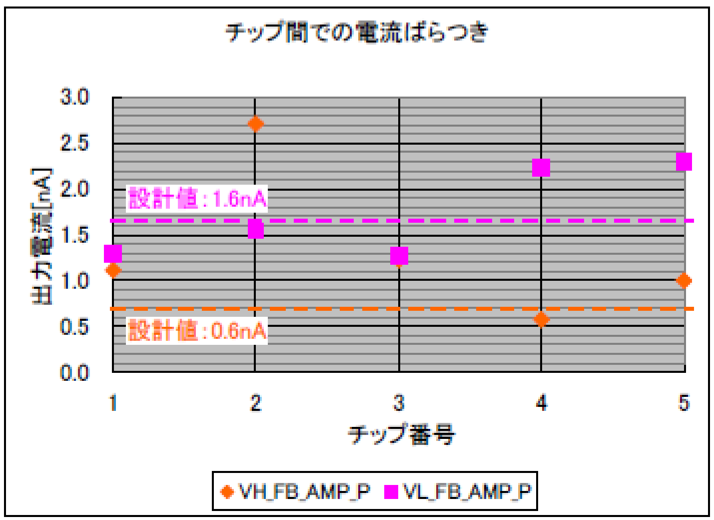


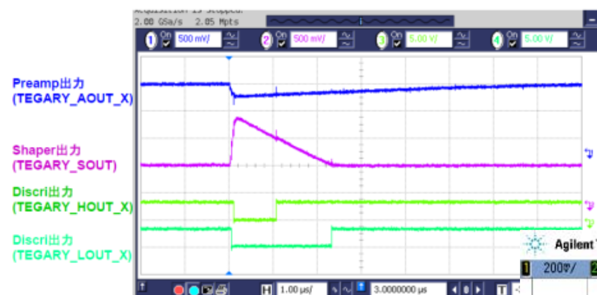
CPIXTEG3
TEG04C_N



Findings though CPIXTEG2/3

- Low current source variation (double checked)
- Insufficient shielding efficiency if the sense node overlaps with Discriminator or Counter (measured on CPIXTEG3)
  - Shielding between shaper and sense node is good (double checked)
- A new chip CPIXTEG3b designed on basis of above findings.



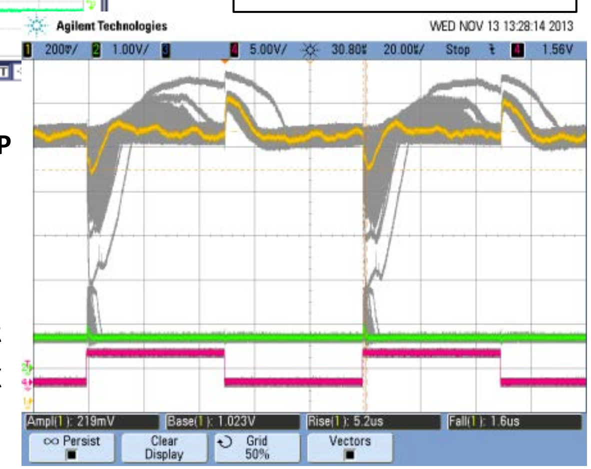


Display Mode: Persist

PREAMP

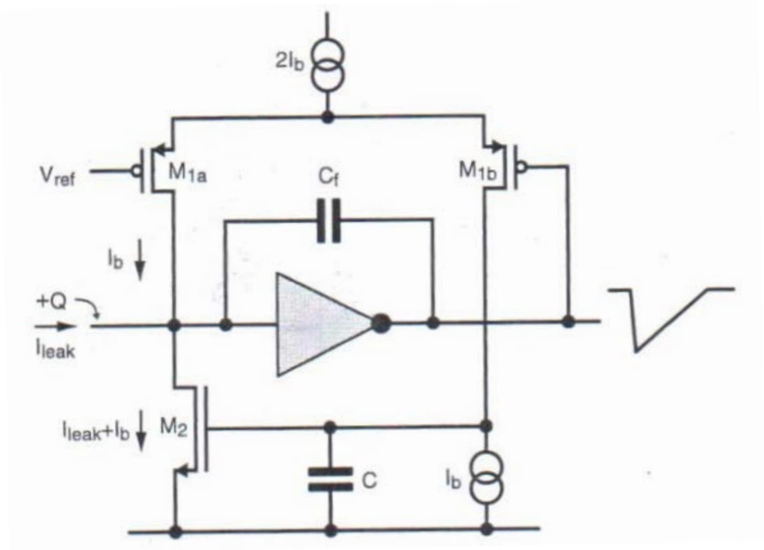
SHAPER

Counter_CLK

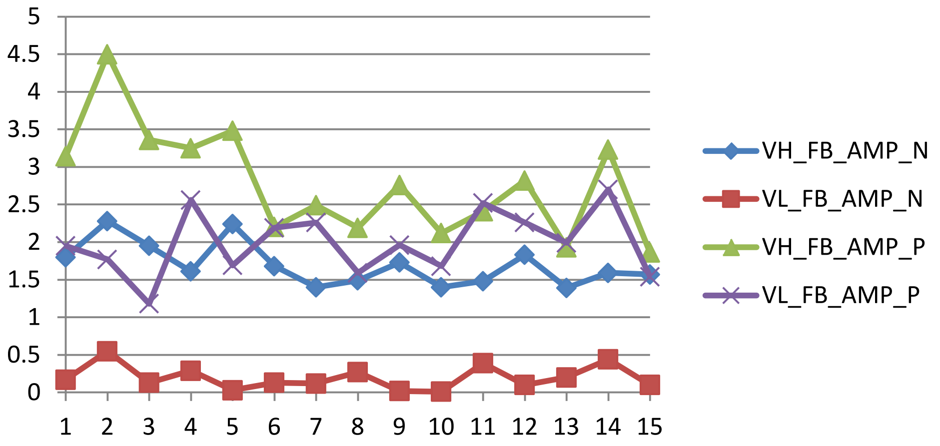


The Krummenacher Scheme and current source

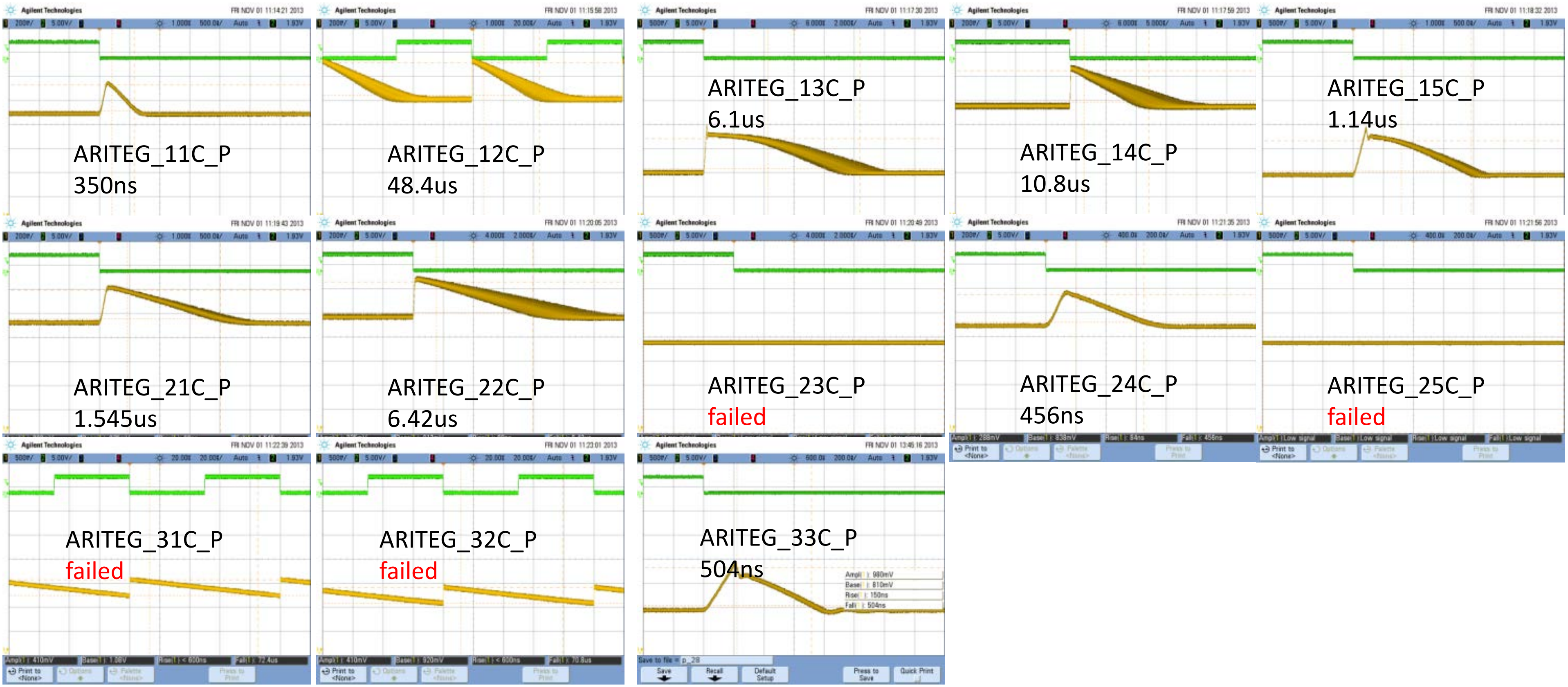
- The kummenacher scheme was adopted for Preamp and Shaper in cpixteg2/3 design.
  - Baseline of output can be set by Vref, which is good for DC coupling to the next discrimination stage.
  - However, its operation relies on the exact ratio of Isource_h and Isource_l.



- CPIXTEG3 Measurement
- PMOS current increased dramatically!
  - VH_FB_AMP_N/VL_FB_AMP_N=1.0nA/0.55nA (SPICE)
  - VH_FB_AMP_P/VL_FB_AMP_P=0.53nA/1.1nA (SPICE)



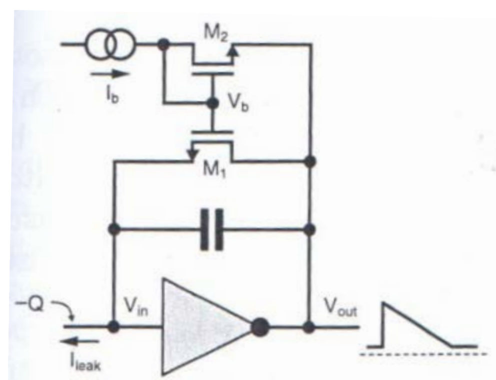
- PREAMP is not supposed to work with VH_FB_AMP_P/VL_FB_AMP_P=3.14nA/1.95nA (0.53nA/1.1nA by SPICE).
  - Feedback current ~ (VL_FB_AMP_P - VH_FB_AMP_P)
- Some PREAMPs among the 13 TEG elements did fail to operate.
  - Others showed quite different falling edge, which implies different feedback current



350ns falling edge ~ 4.6nA feedback current
48.4us falling edge ~ 0.033nA feedback current
6.1us falling edge ~ 0.26nA feedback current

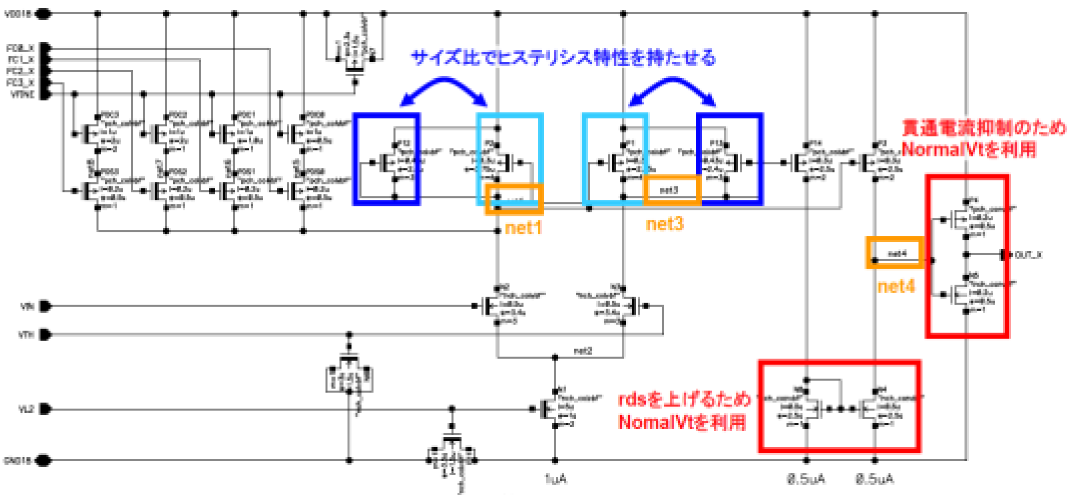
Constant Current Feedback

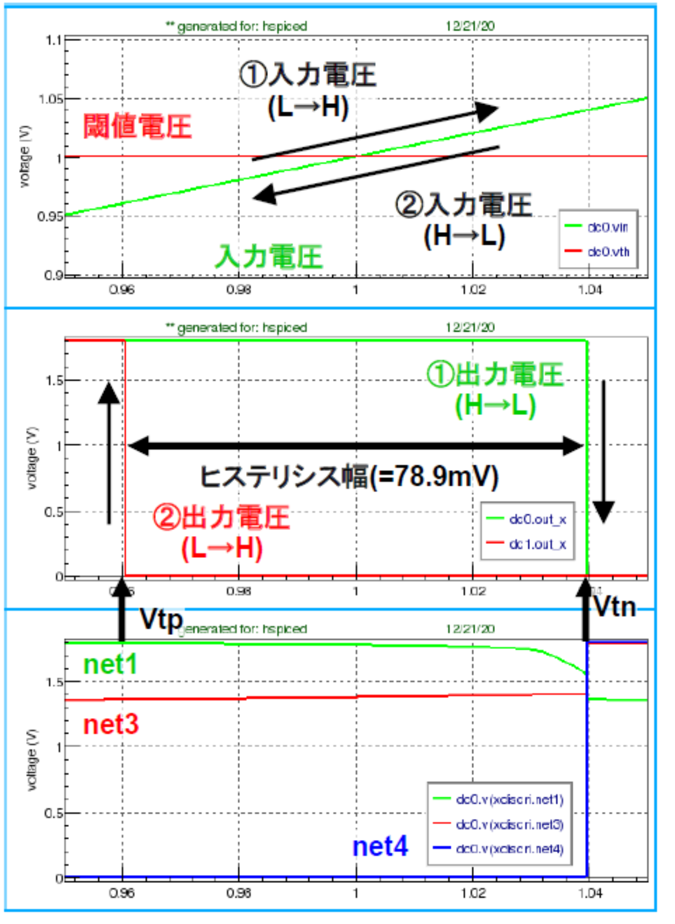
- Constant current feedback structure is less dependent on the precision of low current source.
  - Variation of current source only changes falling edge but the amplifier would still operate.
  - Vout depends on the Vth of input transistor, leakage current and DC operating point of feedback transisitor.
  - DC coupling to discriminator is not a good choice any more.



Differential-pair discriminator

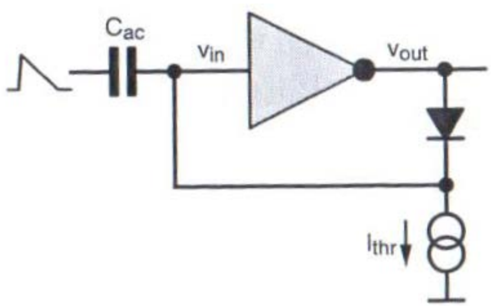
- DC coupled discriminator used in CPIXTEG2/3.
  - Differential pair with composite load(a diode-connected transistor and another one operated in linear region)
  - Hysteresis
  - DAC coded current to adjust the local threshold

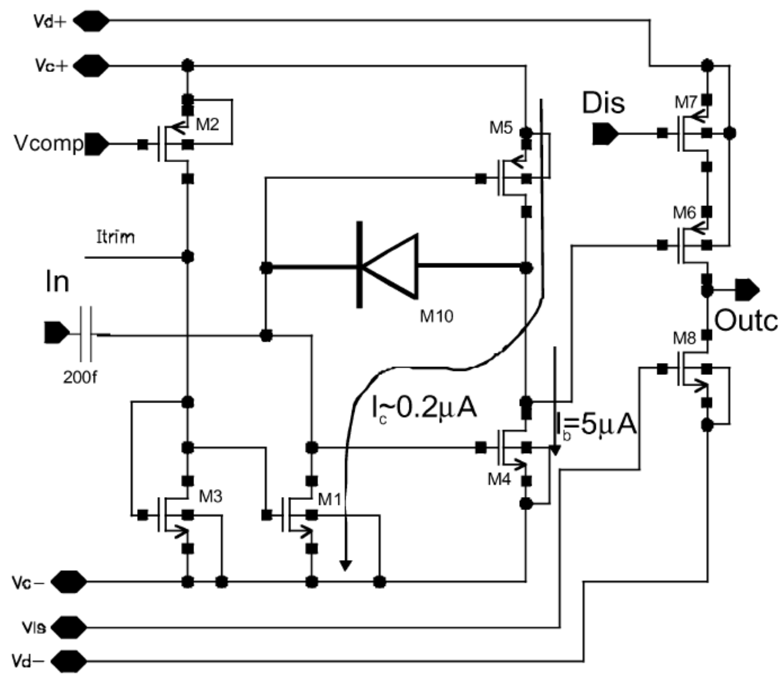




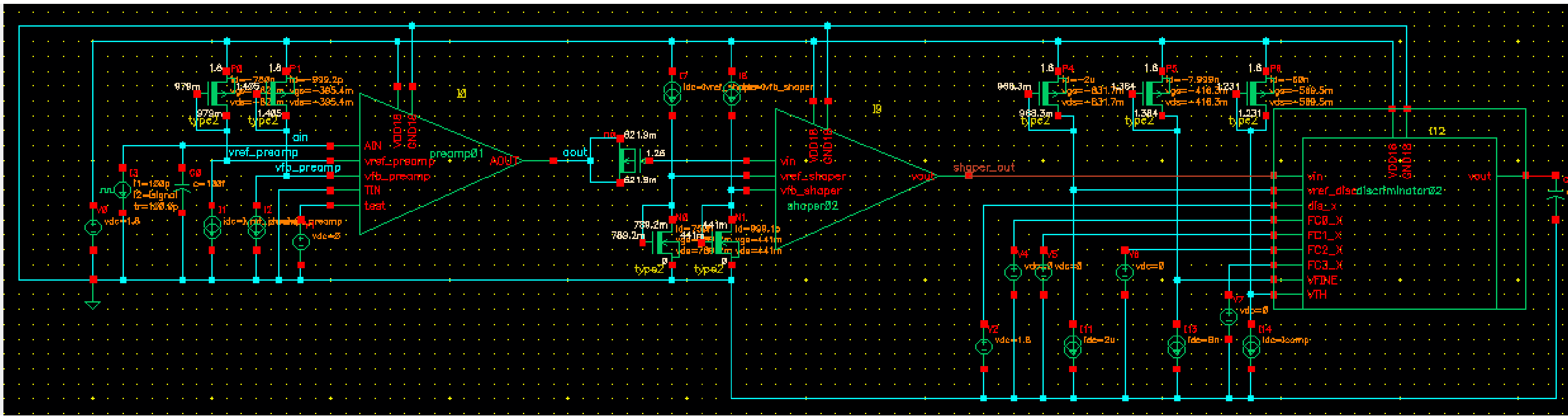
Diode-biased-inverter discriminator

- Used in the PILATUS chip.
- AC coupling is compatible with Amp-Sha that adopted the constant current feedback.
- 120e- threshold dispersion without threshold trim reported, very attractive.
- Threshold voltages set by Vdiode according to $I_{thr} = I_s(e^{V_D/V_T} - 1)$



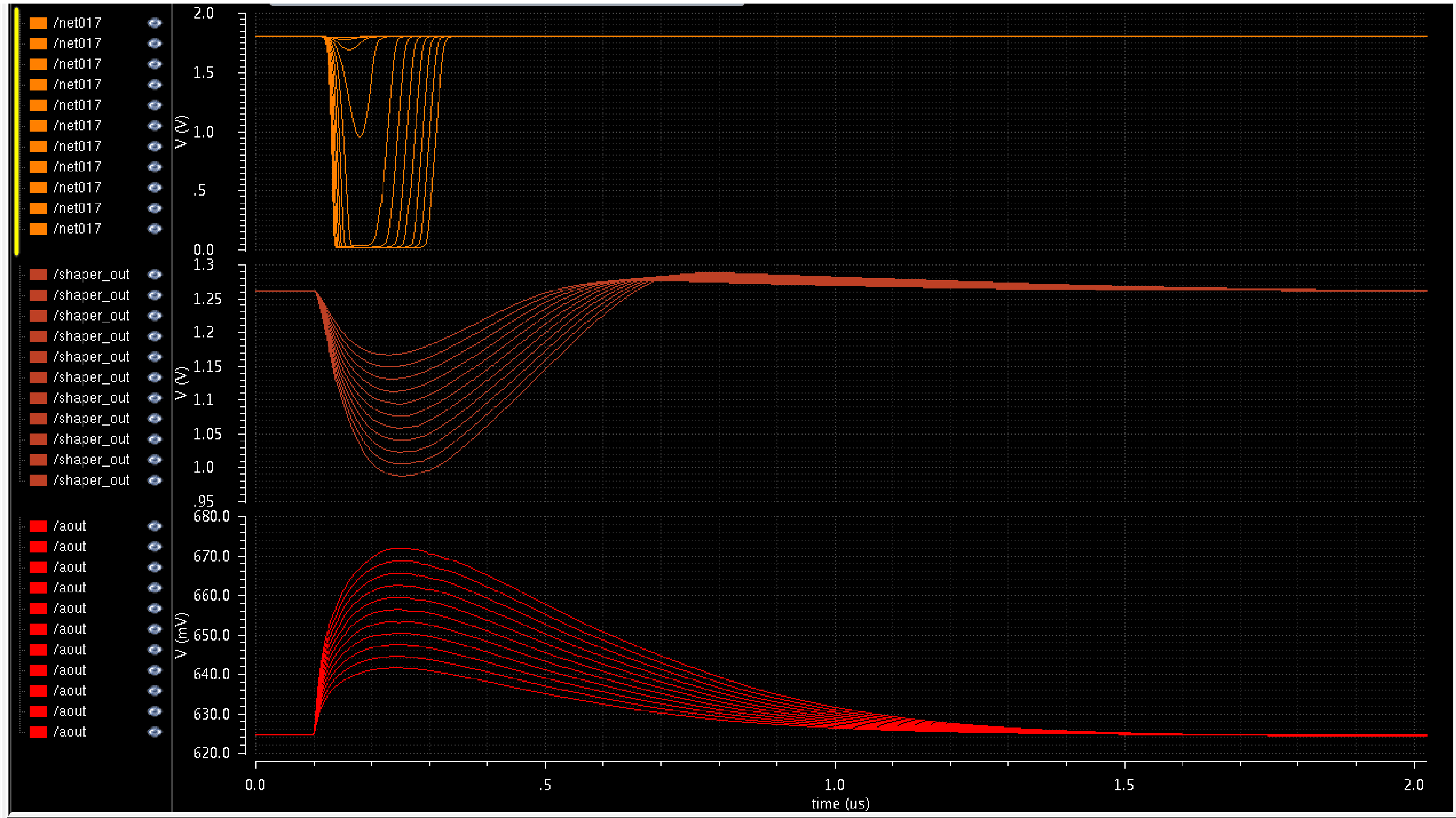


Amp-Sha-Disc System designed for CPIXTEG3b

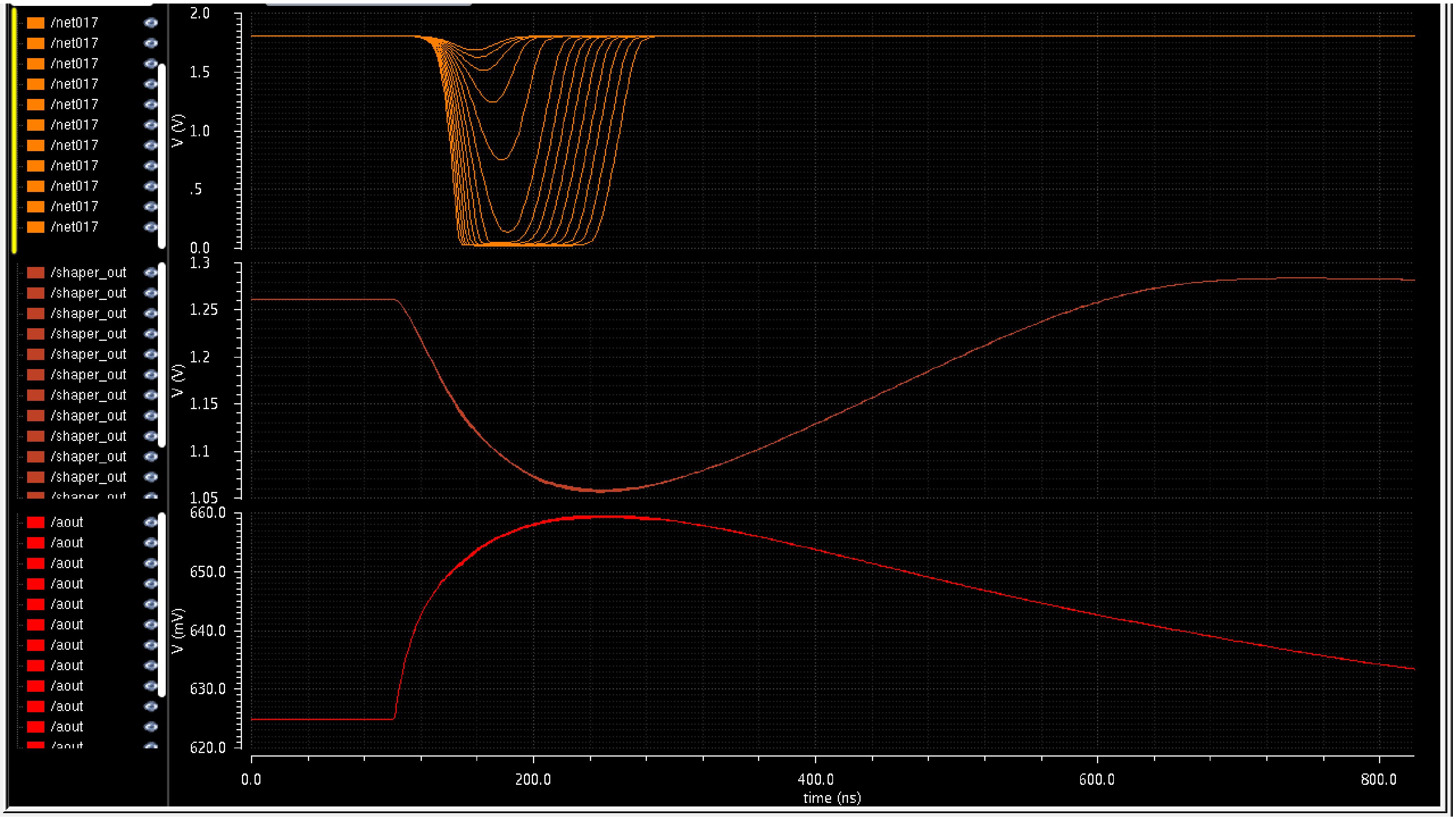


- Constant current feedback Preamp, 5fF feedback capacitor
- AC coupled to shaper, voltage gain of 6
- AC coupled diode-biased inverter discriminator, 4-bit local tunning

$I_{threshold}$ (I_0) =40nA, input charge = 750e$^-$ to 2000e$^-$



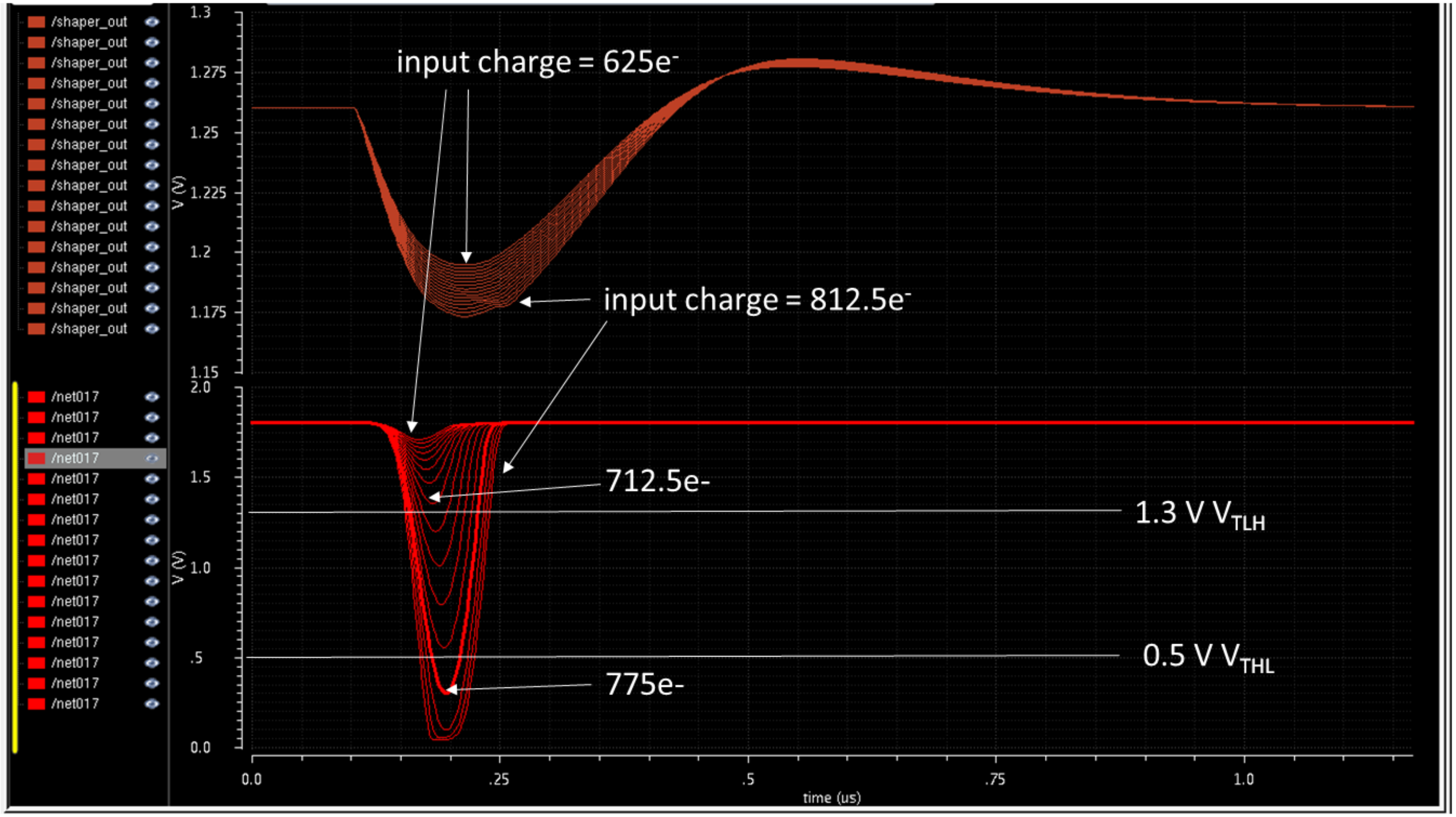
input charge = 1500e$^-$, $I_{threshold}$ (I_0) = 40nA to 66nA



threshold scan

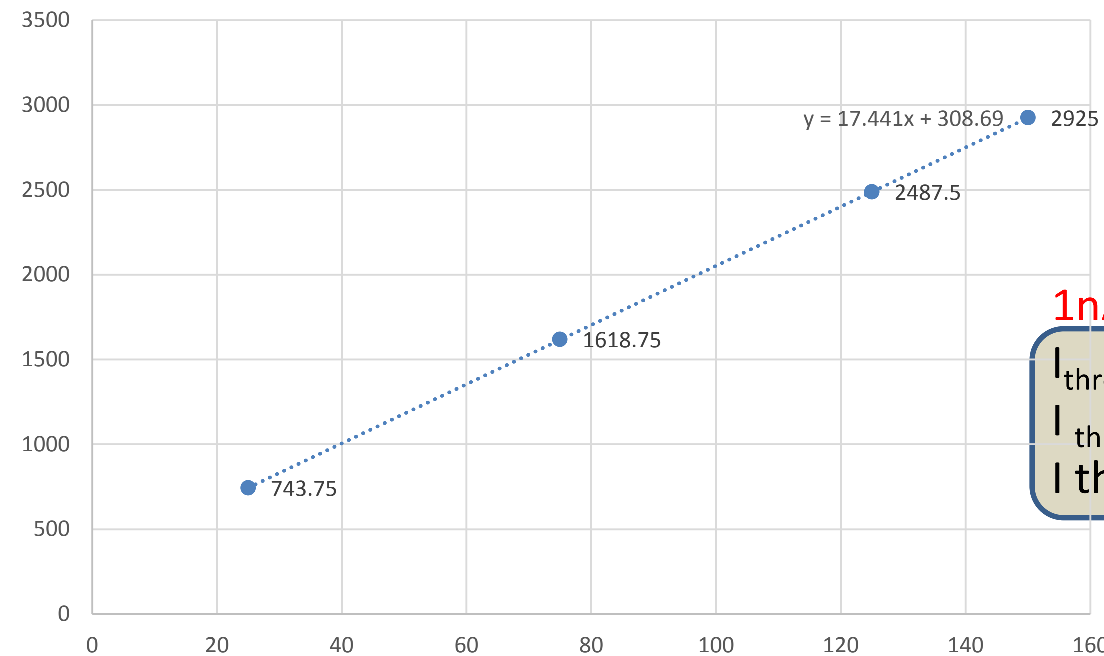
Ithreshold = 25nA, Assuming V_{TLH} = 1.3V and V_{THL} = 0.5V for the following digital inverter;

Transition btw. 712.5e⁻ and 775e⁻



$I_{threshold}$	input charge (e^-)	Transition charge (e^-)	Average input charge (e^-)
25nA	625-812.5	712.5-775 (62.5)	743.75
75nA	1500-1687.5	1575-1662.5 (87.5)	1618.75
125nA	2375-2562.5	2437.5-2537.5 (100)	2487.5
150nA	2812.5-3000	2875-2975 (100)	2925

Average input charge (e^-)



Ithreshold (nA)

1nA ~ 17.4e^-

$I_{threshold}$ Adjustment Range: 25-150nA
$I_{threshold}$ tuning step: 2-5nA
I threshold tuning DAC: 4 bits or 3 bits

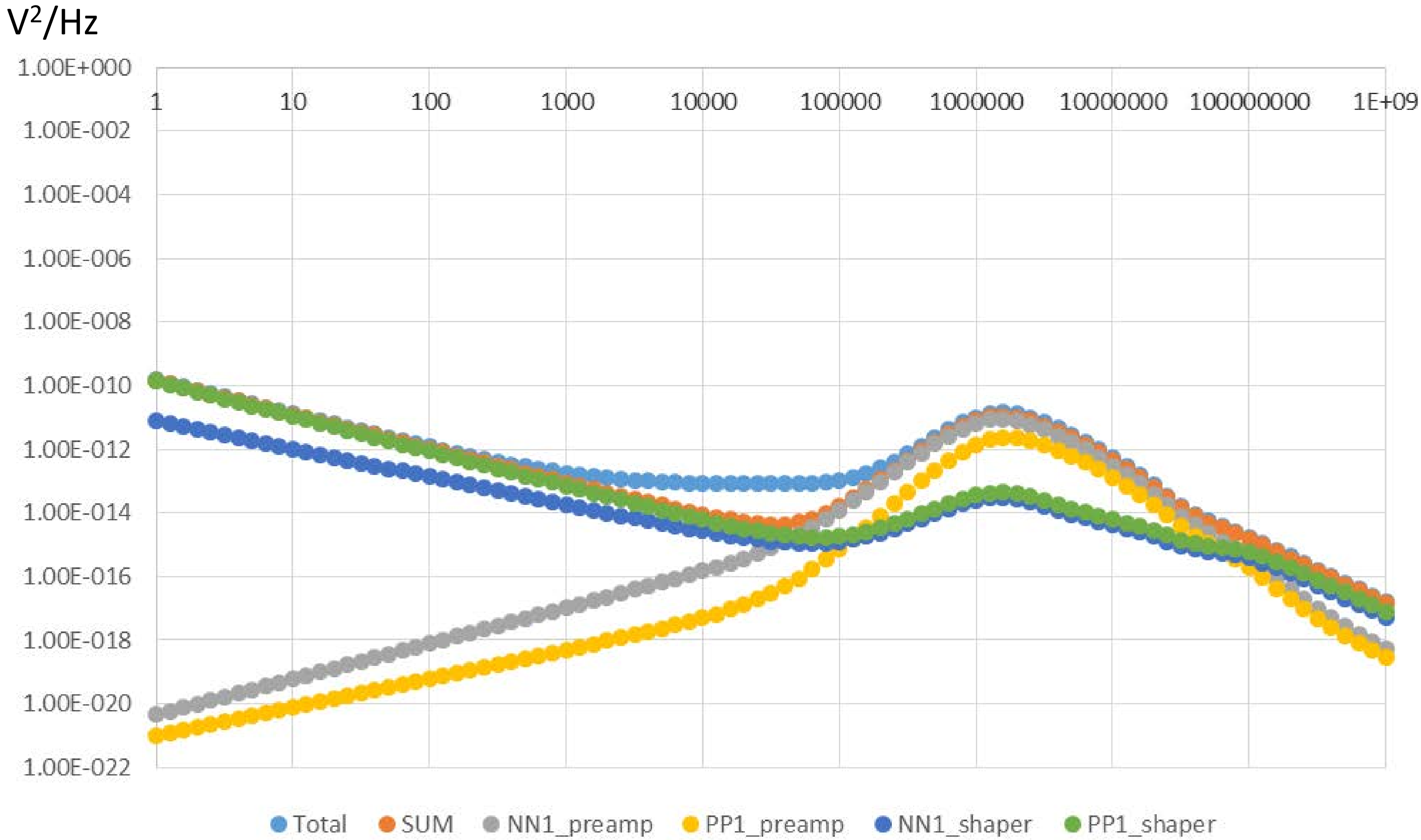
Total Noise Spectrum @ shaper output

Primary noise source: NN1&PP1 of preamp around 2 MHz;

NN1&PP1 of shaper at low frequency;

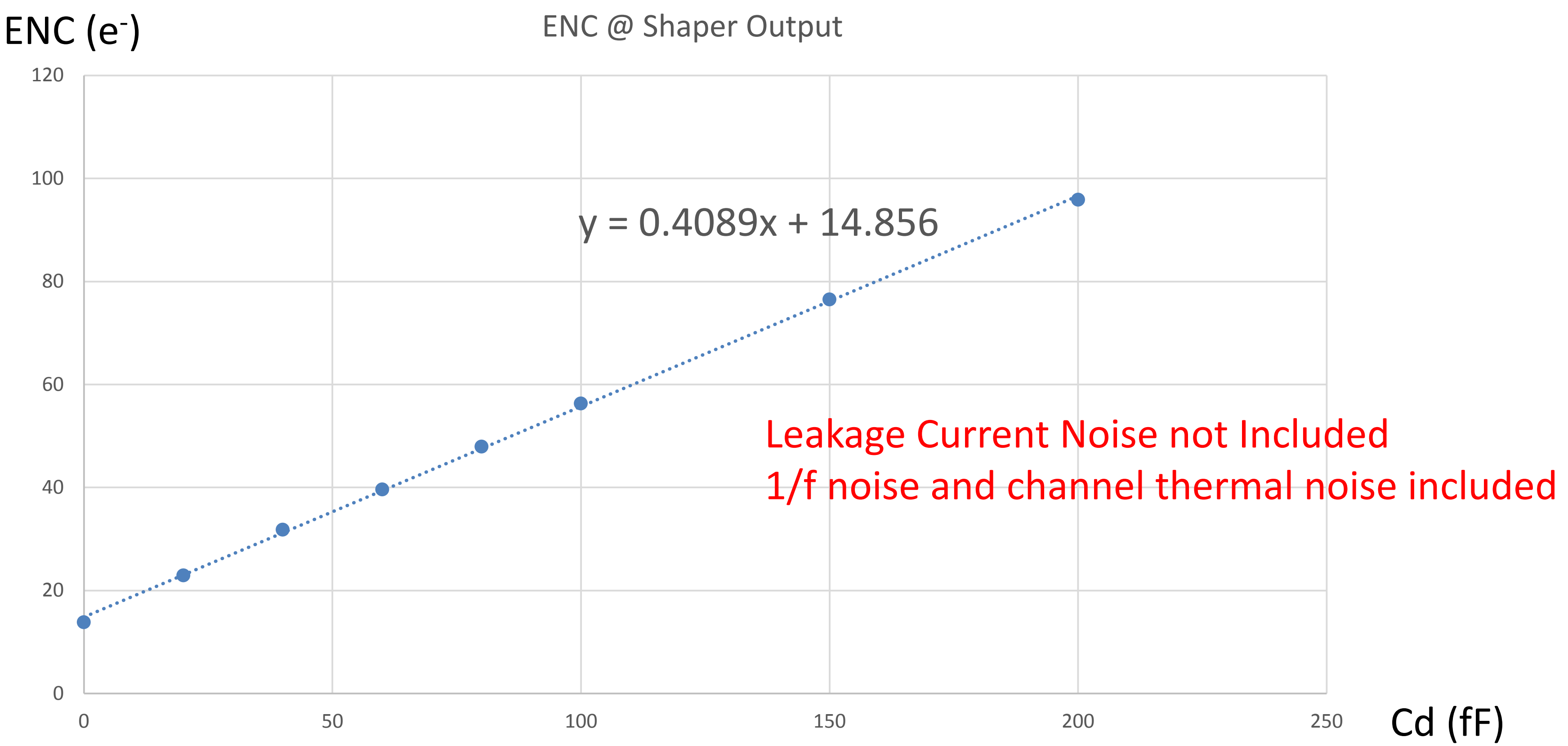
SUM = NN1_preamp + PP1_preamp + NN1_shaper + PP1_shaper

(Total – SUM) is mainly contributed by the Feed-back Tr. (P1) in shaper



- Noise @ PREAMP Output
  - n_o = 1.4mV
  - equivalent to 70 e^-
- Noise @ SHAPER Output
  - n_o = 6.8mV
  - equivalent to 57 e^-

Cd=100fF;
Cf=5fF;
Ccouple = 30fF
Ifb_preamp = Ifb_shaper = 1nA;



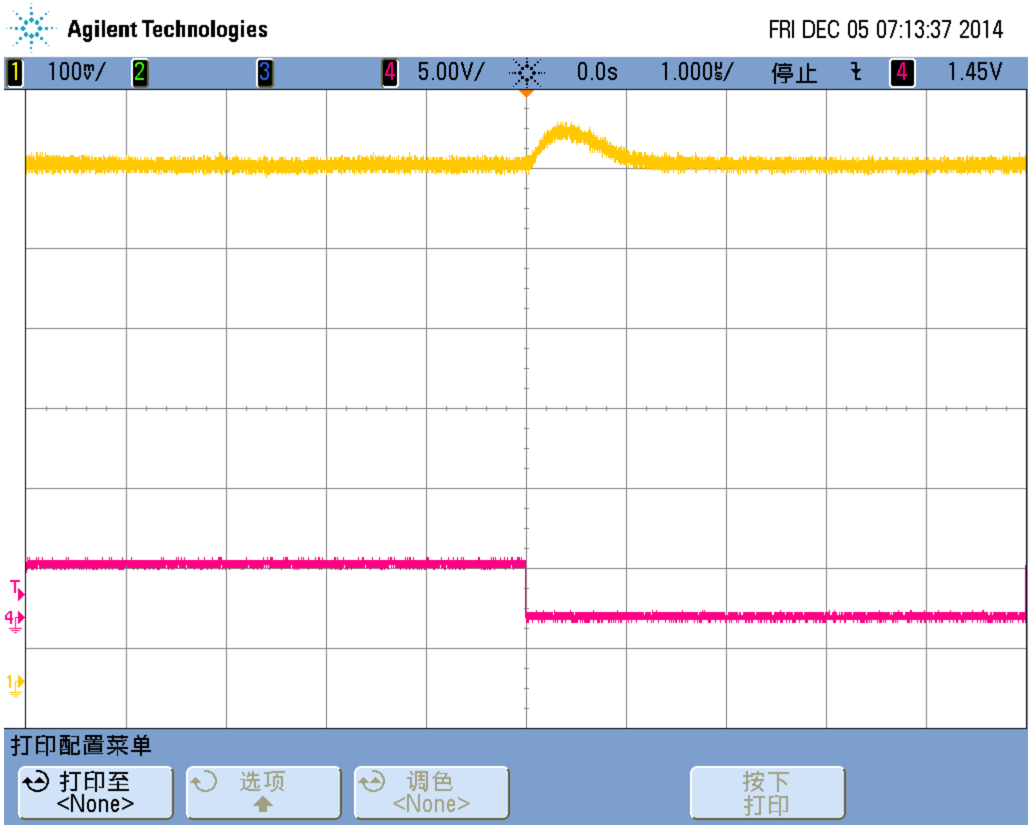
First Test Results of CPIXTEG3b (1)

- Bias current measurement (VIO_BPW = 0.85V)
  - Discrepancy between Iout and Iout_pixel1,2,3 affected by VIO_BPW, but required different VIO_BPW to compensate NMOS and PMOS respectively.
  - Error on Ifb_shaper not understood.
  - Should be OK to operate the chip on the basis of measurement results.

Current Source	Iin (nA)	Current Ratio	Iout (nA)	Iout_pixel1 (nA)	Iout_pixel2 (nA)	Iout_pixel3 (nA)
Ifb_preamp	-10.5	10:1	-1	-0.49	-0.5	-0.47
Ifb_shaper	1.6	10:1	1.4	1.3	1.4	1.4
Iref_preamp	-3000	4:1	-791	-726	-709	-696
Iref_shaper	3000	4:1	1180	1140	1200	1170
Ithr	-1500	8:1	-223	-172	-167	-172
Ithr_tunning	-40	8:1	-4			

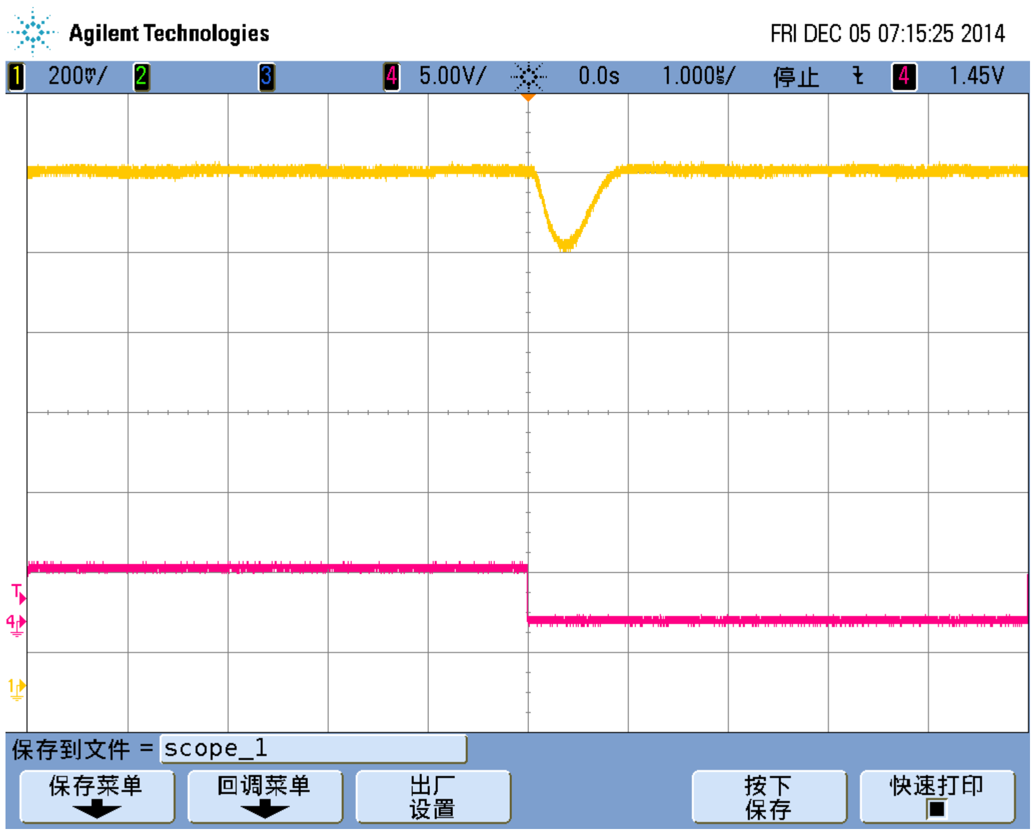
First Test Results of CPIXTEG3b (2)

- Analog out of Preamp
  - Vtest = 80mV, equivalent to 1900 e^-



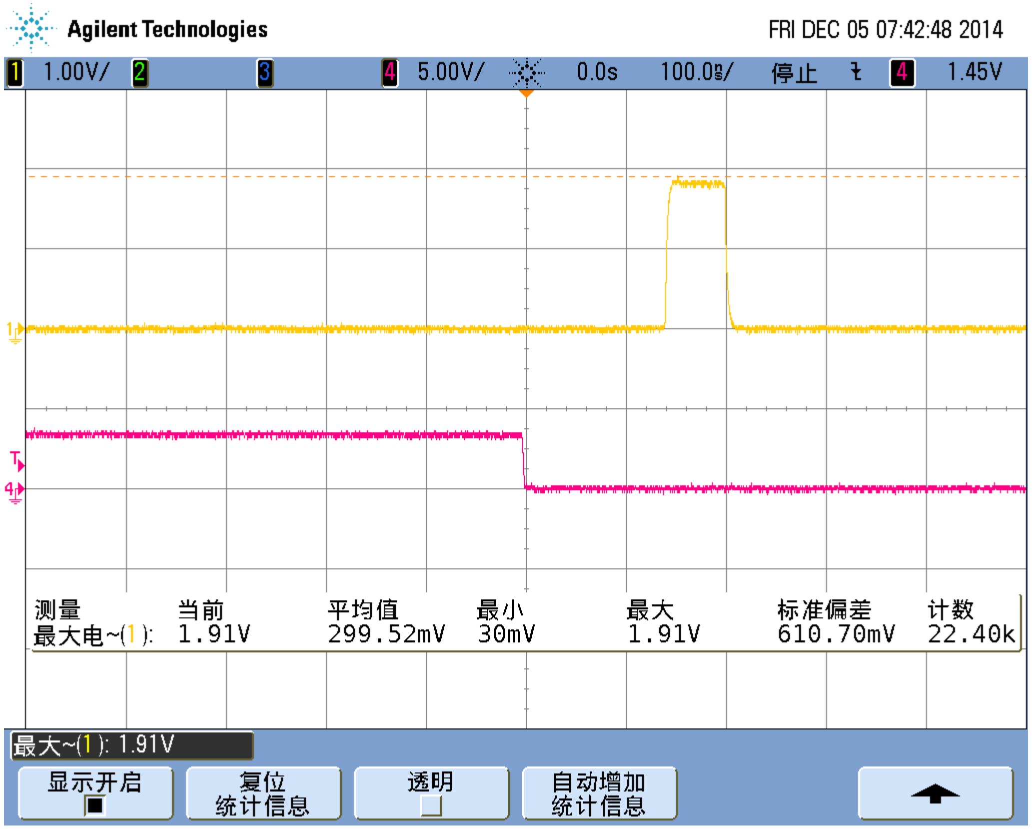
First Test Results of CPIXTEG3b (3)

- Analog out of Shaper
  - Vtest = 80mV, equivalent to 1900 e^-



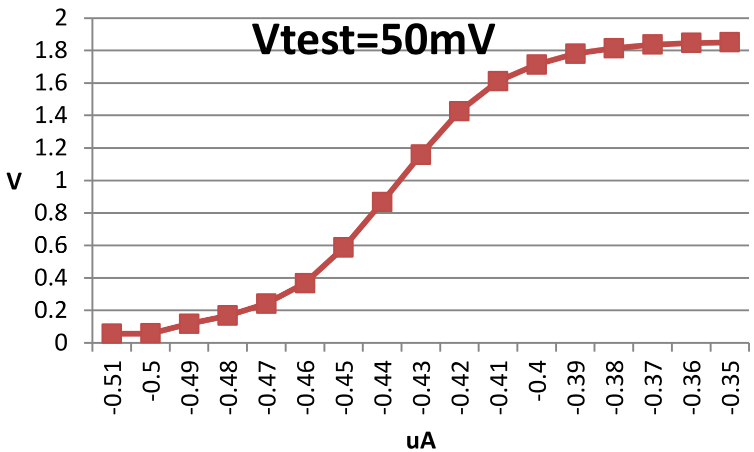
First Test Results of CPIXTEG3b (4)

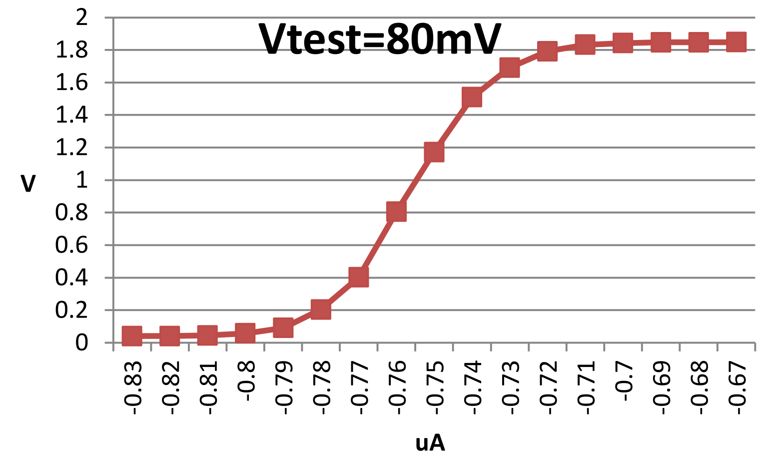
- Analog out of Discriminator
  - Vtest = 80mV, equivalent to 1900 e^-

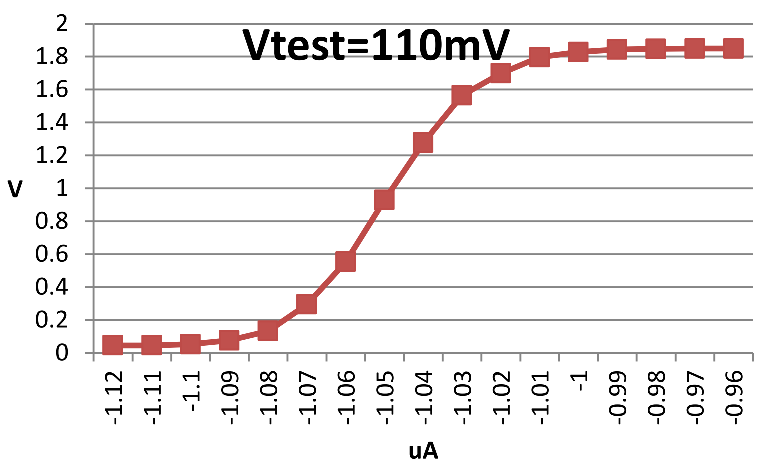


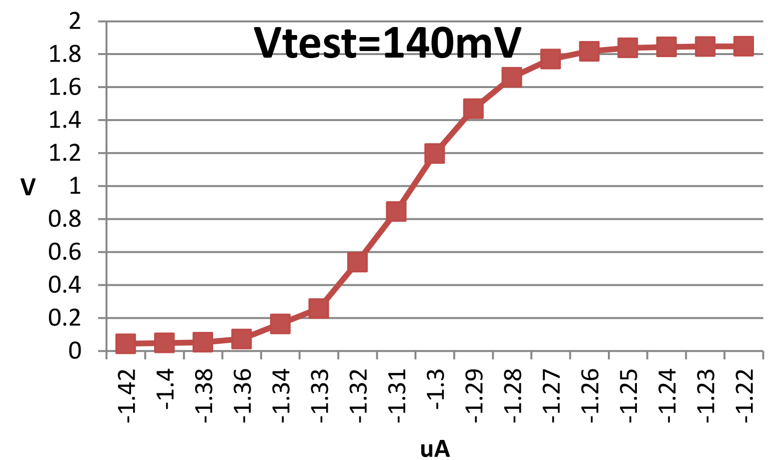
First Test Results of CPIXTEG3b (5)

- S curve measurement
  - ENC ~ 27e$^-$





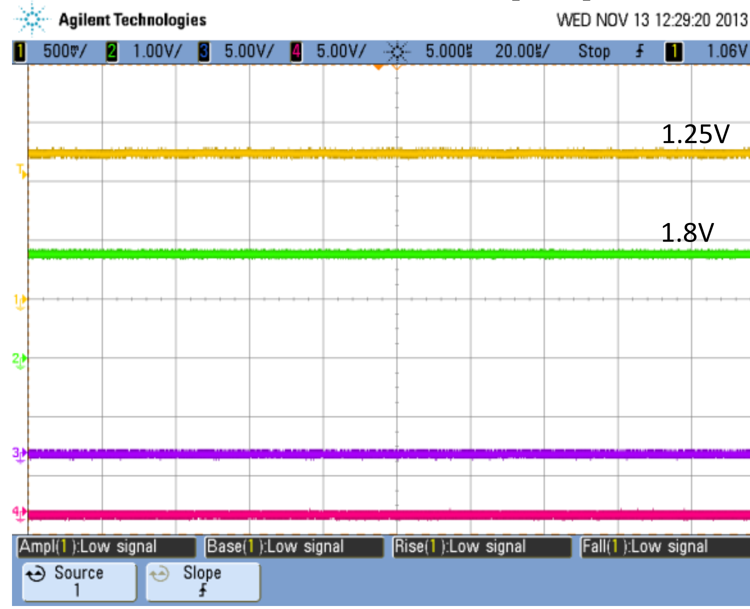




Shielding Measurement on CPIXTEG3 (1)

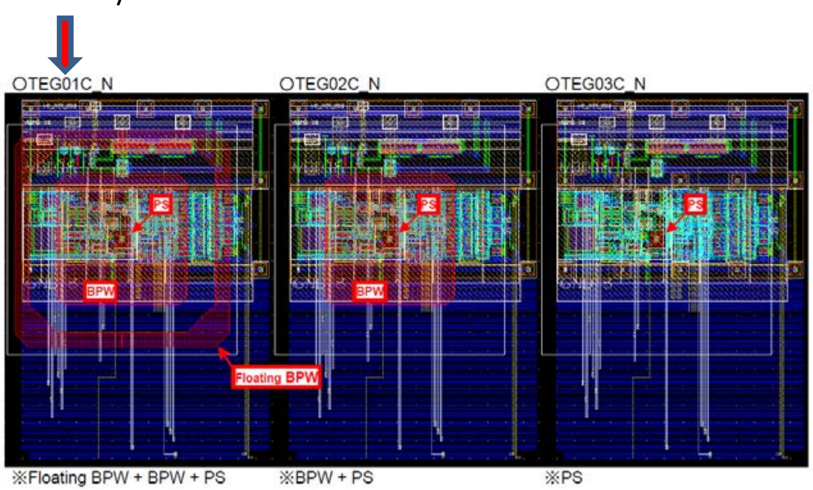
1. Oscillation

Disable SHAPER via VH2



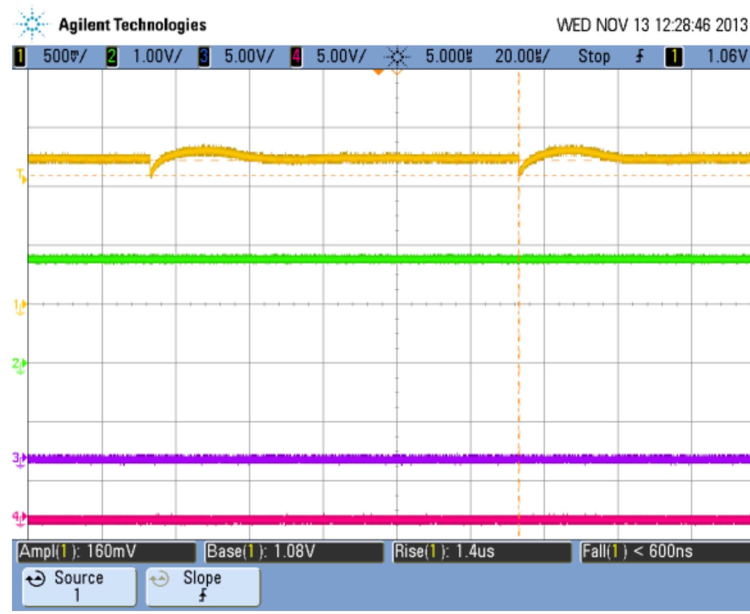
2. Oscillation stopped after shaper disabled

Pixel Layout



Vtest = 300mV;
VL_AMP_N = 300mV;
Vdet = +5V

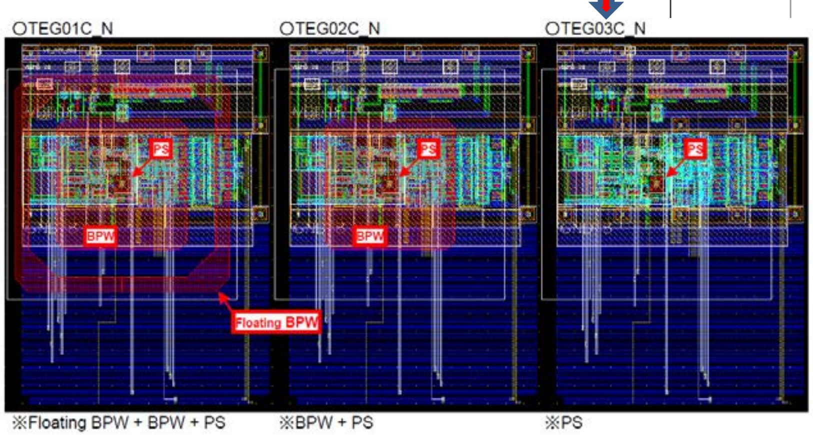
3. Response to Charge Injection 300mV



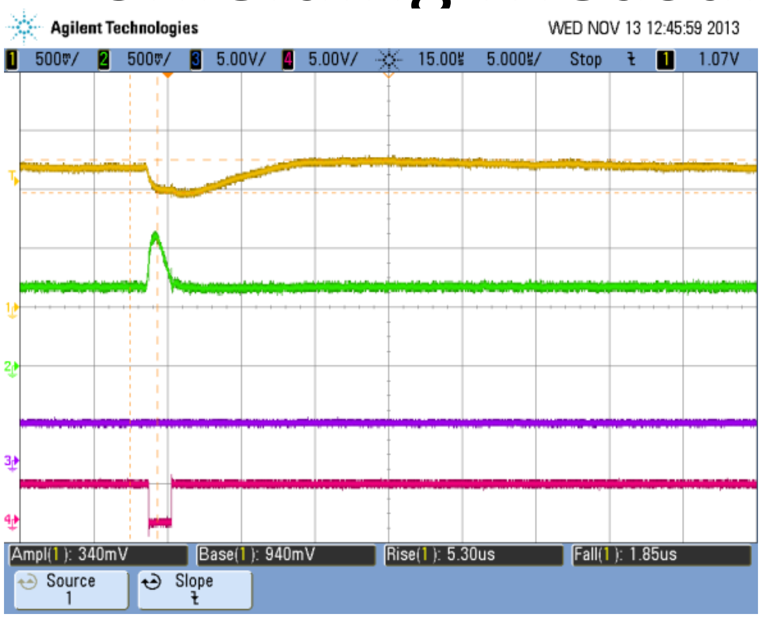
Shielding Measurement on CPIXTEG3 (2)

Vdet = +5V;
Adjust VL_AMP_N = 0.2V;
Vtest = 300mV;
Vthh = 1250mV;
Vthl = 800mV;
Glitches can be removed by disabling Disc. via DO_EN.

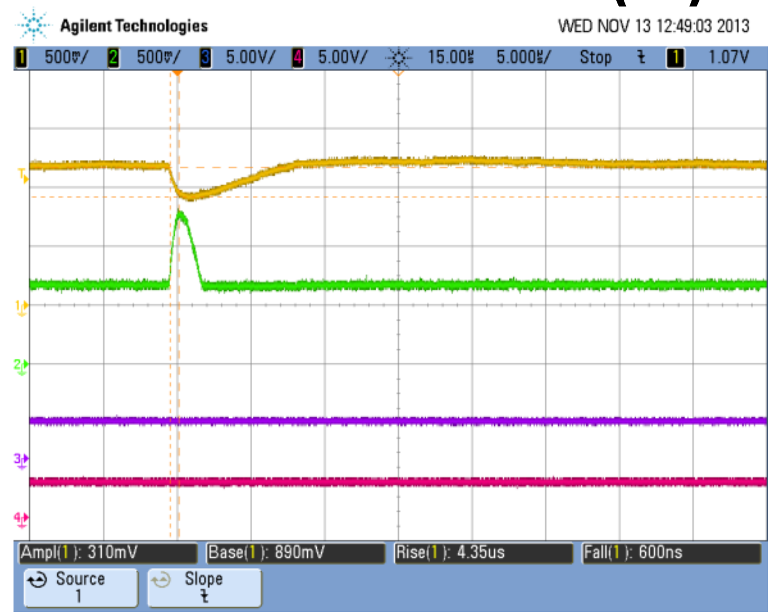
Pixel Layout



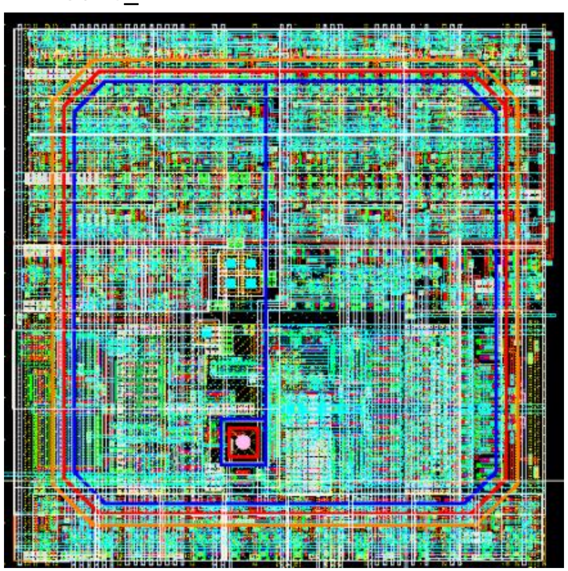
Shielding Measurement on CPIXTEG3 (3)



Disable Disc.
via VH2



TEG04C_N

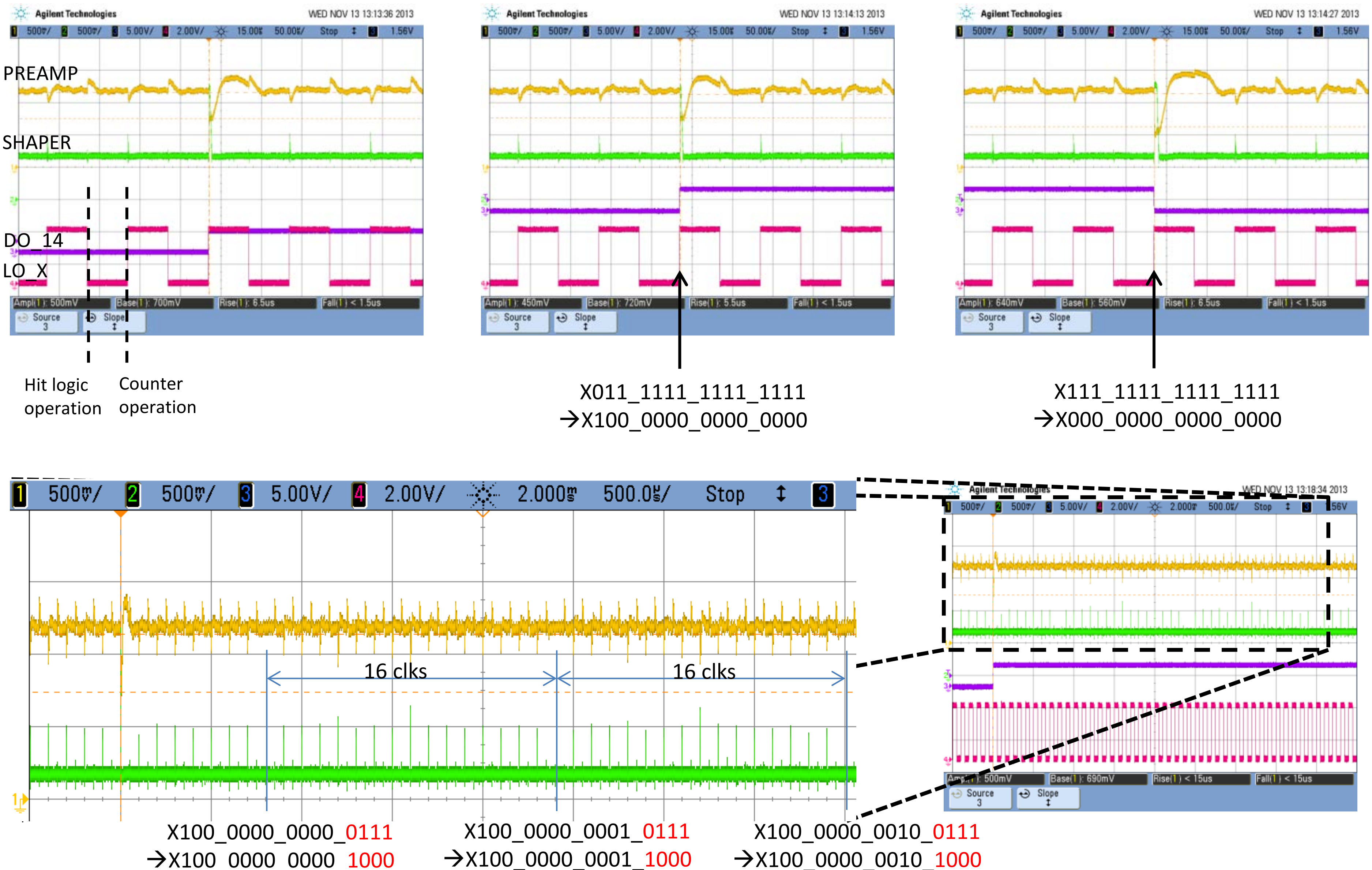


1. Charge Injection with Discr. working

Vtest = 600mV;
VL_AMP_N = 280mV;
Vdet = +5V

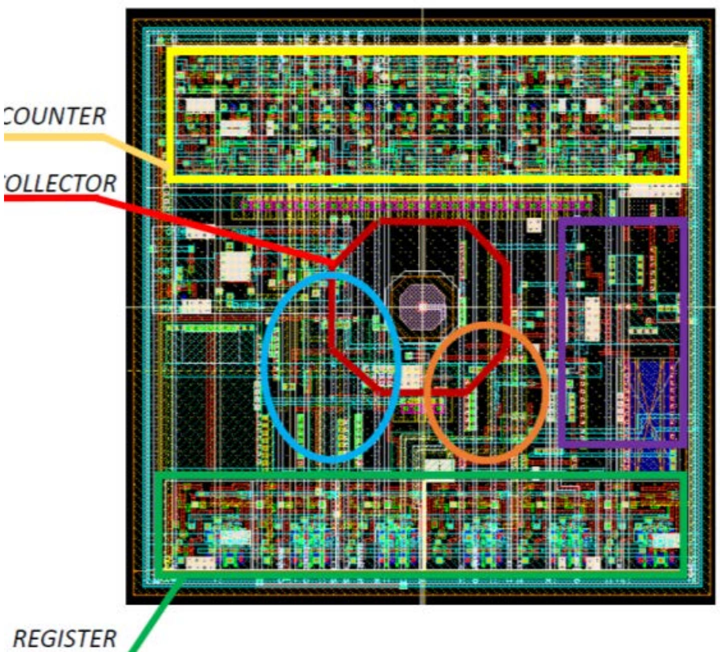
2. Charge injection with Discr. stopped

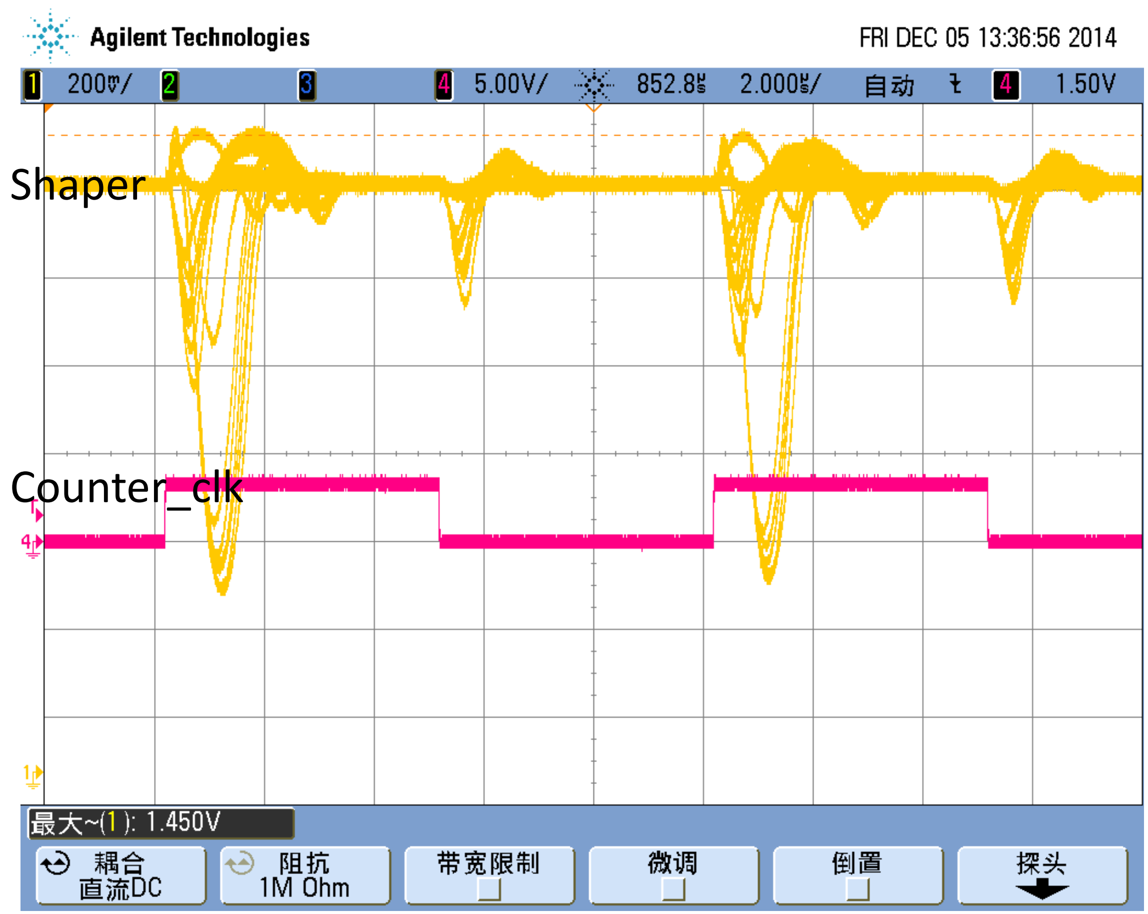
Shielding Measurement on CPIXTEG3 (4)



Preliminary resutls on CPIXTEG3b

First CPIXTEG3b dilivered was fabricated on normal SOI wafer. No DSOI at all. Clear crosstalk seen.





Summary

- Shielding is a critical issue in counting pixel chips.
- A new Amp-Sha-Disc system works, which is less dependent on the precision of very low current source.
- Nested-Wells provided shielding between analog and sense node, but no sufficient for shielding digital part in the pixel.
- Small sense node and small pixel is being pursued.