Advanced technology for ILC Calorimeters

Readout and DAQ parts

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KEK seminar
2017, December 12
Electronics challenges for ILC ECAL

DAQ introduction

Electronics development

Beam tests results

Next steps

Feeding others projects
Preview of prototypes

1st prototype
30 layers ~ 10k channels

Proof of concept
- Linearity
- Resolution
- Sensors
- Very front-end

Feasibility of design options
- Compactness
- Granularity
- Front-end
- Power pulsing
- Long SLAB

Construction
- Integration
- Environment
- Services
- Industrialization
- Tooling
- Project org.

Time

2nd prototype
6 layers ~ 6k channels

NEW ELECTRONICS DESIGN

Last prototype
10 layers ~ 10k channels

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Introducing the DAQ
Calicoes

- Highly modular and distributed
- Control the Ecal electronics but also the peripheral devices (Power supply, pulse generator,...)
- Provides a high level state machine for final user
- Scripting language (Python)
- Good stability

Global control-command architecture
Calicoes

GDCC (Gigabyte Data Concentrator Card) vs CCC (Clock and Control Card)

- Able to connect 7 DIF
- Base on Xilinx Spartan XC6SLX75
- Marvell component for Ethernet

- Until 8 HDMI connections
- Synchronize all sub-systems
- Distribute asynchronous trigger/busy signals
- Capable to distribute clock 50MHz

GDCC

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<th>FPGA</th>
<th>GEMAC</th>
<th>Main Interface (based on several FSM)</th>
<th>DIFs Links (Protocol fsm ser-des 8b/10b)</th>
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CCC Board

MARVELL

MCLK

TRIG

ETHERNET

TO DIF

DIFs Links (Protocol fsm ser-des 8b/10b)
Goal: connect the detector to control and DAQ system by serial link synchronous to 40MHz.
- Condition signals to VFE chips
  - Configuration
  - Readout
- Generate clock 2.5MHz for ReadOut
- Get information like board status, firmware version ...

Able to read several thousands of detector channels up to 13000.
Able to read different chips for many experiments in our laboratory.
SMB (Sweat Main Board)

Goal: condition signals for VFE chips, power supply and clock integrity.

Regulator for Analogue and Digital power supply

Big capacitance (300mF) to absorb the dynamic power supply current, design for 1 ms acquisition in the barrel.

Buffer to drive the clocks 40MHz and 2.5MHz
FEV board (Front End Board)

- Read energy of 1024 pixels
- Slow Control for 16 Skiroc2
- Readout for 2 partitions of 8 chips
- 2 power supply (analogue & digital)
- 16 layers

16 Skiroc2 chip

1024 pixels

Glued wafers

Pedestal

MIP
Skiroc chip

- SILICON SENSORS (325µm thick): 26000e-/MIP
- C detector
- Estimated 9pF + 10pF for PCB pad's
- PIN diode leakage up to 10nA / channel
- Ultra low power consumption (to minimize cooling)
  → 25 µW/ch with Full Power Pulsing
- 1 MIP = 4fC
- 64 channels
- 250 pads
- Technology: AMS SiGe 0.35µm
- Size: 65mm²
- Very low noise: 2500e- (0.4fC)
- Dynamic range: 0.4fC → 10pC

SKIROC: Silicon Kalorimeter Integrated Read Out Chip

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Skiroc chip

Scurves vs threshold

Preamplifier DC level uniformity

Fast shaper noise studies

rms noise= 5.3 mV ie 1/9 MIP → S/N>9

DC PreAmplifier SKIROC2

<=1.969 V
rms=1.5 mV
First tests of ASU bench

There is a specific bench to test FEV board before gluing.
Possibility to place a wafer, a mechanic interface and the FEV board.

Goal: verify all chip answered, pcb as no shortcut.
Also, it’s interesting to estimate noise on each chip.
Scurves, noisy channels

Instead activated all channel, run 8 by 8.
→ Reduce effect of crosstalk.

Uniform noise around 220-240uDAC.

Reproducible measure in time.
Introduce short SLAB

Goal: first studies to improve design.
- Be able to detect a MIP (Minimum Ionization Particle)
- Configure all chip compare to noise
- Have adapted signals for clock and control
- Get a S/N > 10
- Read raw data in few ms.
Short SLAB

Get a final layer design include chips, PCB, wafer ...
Thickness of electronics < 4mm (half alveolar size)
Compact detector
Include up to 10 layers
Possibility to place Tungsten between each layer
Connect each power supply by a front panel.

Auto-masking of noisy channels:
Every layers are adjusted in laboratory with optimize scripts.
10 layers adjusted in 3h !!!
Excellent results, S/N~20 better than 2015.

Concept is validate $\rightarrow$ next step LONG SLAB

Test beam performance presentation: [https://indico.cern.ch/event/629521/contributions/2703010/](https://indico.cern.ch/event/629521/contributions/2703010/)
Event Display

ECAL -> Acquisition server -> Multiple ECAL converters -> Event builder -> Track reconstruction

Real time domain

Online Monitor

Energy Histogram

Event display

Angle Histogram

Calicoes Event Display

Shower (event layer/layer)

Compact shower + “cosmic”
ILD Slab (for final detector)

For ILD 8 to 12 ASU / layer ➔ Layer length = 2.2 meters

Many challenges:

- Interconnection solution
  - Kapton
  - Connector

- Propagate signal on 3 meters
  - Clock (delay, load, attenuation, ...)
  - Control signals
  - ReadOut (data integrity, amount of data)

- Power distribution?
  - Power tree
  - Cross board

- Mechanical structure
  - Design with minimize distortion
  - Weigh
  - Transportation
12 ASU full equipped of wafer 120k€
→ Need to make physics with less cost
→ Use mini wafer (4x4 pixels instead of 16x16)

Alpha source put under the long slab for physics

S-curves analysis for baby wafer glue on long slab
ILD Slab (for final detector)

New mechanical structure, able to receive 12 ASU

→ Total length 3m

System to place ASU on structure with 3d printed
Location: J-PARK neutrino beam, JAPAN
Physics goal: Cross section ratio measurement between H2O/CH for charged-current interaction with different Neutrino energy ranges.
Base on Calice design:
2 pcb layers
- read out: 4 chip SKIROC2cms, 4x32 channels
- FPGA: ALTERA MAX10
- sensor (200µm, 6” silicon wafer)
→ Electronics and instrumentation department of LLR develop many prototypes (conception, production and tests), with high technology and good performances. The results of ILD Slab in the next test beam will shows the ability to instrument 2.2 meters active layer (readout, clock, power, data integrity, …).

→ LLR DAQ is generic and adapt for many experiments, local, international (HGCAL CMS) and with Japan (T2K WAGASCI) on innovative and complex projects of detector.

→ LLR able to solve Electronics, DAQ, instrumentation Challenges, in a context of international project with R&D phase, tests definition, proposal solutions. …