SEABAS 用 INTPIX4 サブボード

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このボードは、SEABAS (GN-0836-1) ボード用のサブボードで、INTPIX4 チップの試験用のものです。

従来のものと違いベアチップを直接基板上にのせ、ワイヤーボンディングします。チップの外形はおよそ 10.3mm x 15.5mm (添付の図参照) で、センサー部の下には X 線照射用に長方形の穴をあけ、周辺部の裏面は導電性接着剤で基板上で電極(VBACK)に接続します。

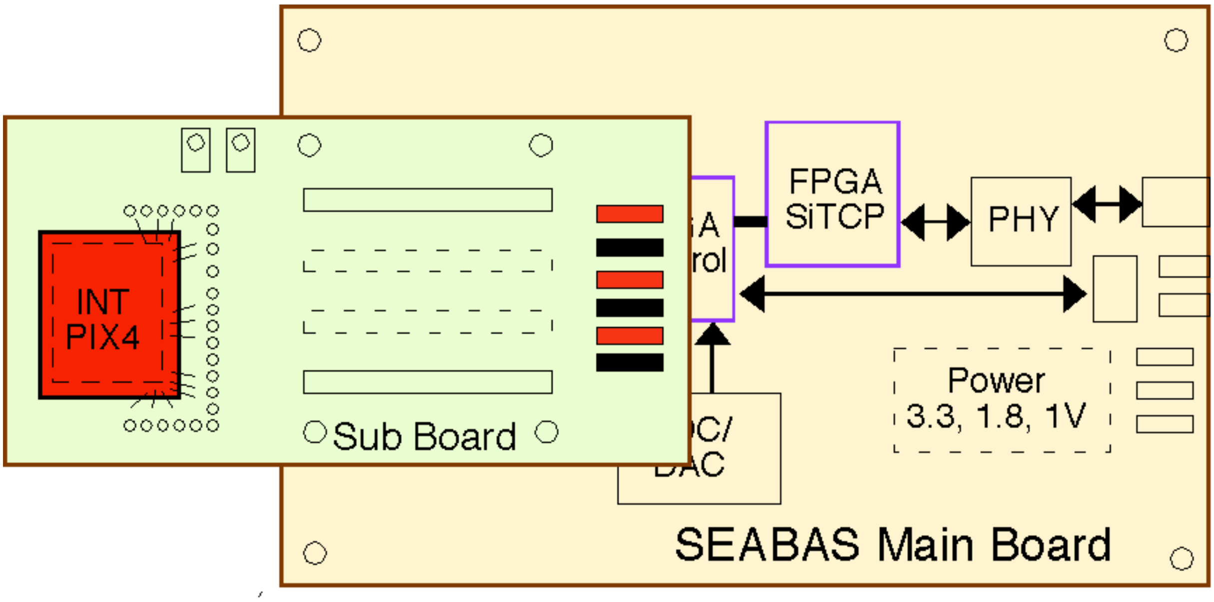
全体のレイアウトイメージを下に示します。いつもと同様に以下の点に注意して下さい。

＊やや多めに適当な数のパスコンを入れて下さい。

＊基板にまんべんなく 4 個くらいのグラウンドピンを立てて下さい。

＊空いているエリアは IC 等の追加の為の穴を開けておいて下さい。

＊Jumper, 測定 Pin 等のそばに出来るだけ信号名のシルクを書いて下さい。



MX1350 INTPIX4 Pad & Pin Assignment (15.4 mm x 10.2mm chip) 2009.11.20 Y. Arai (KEK)

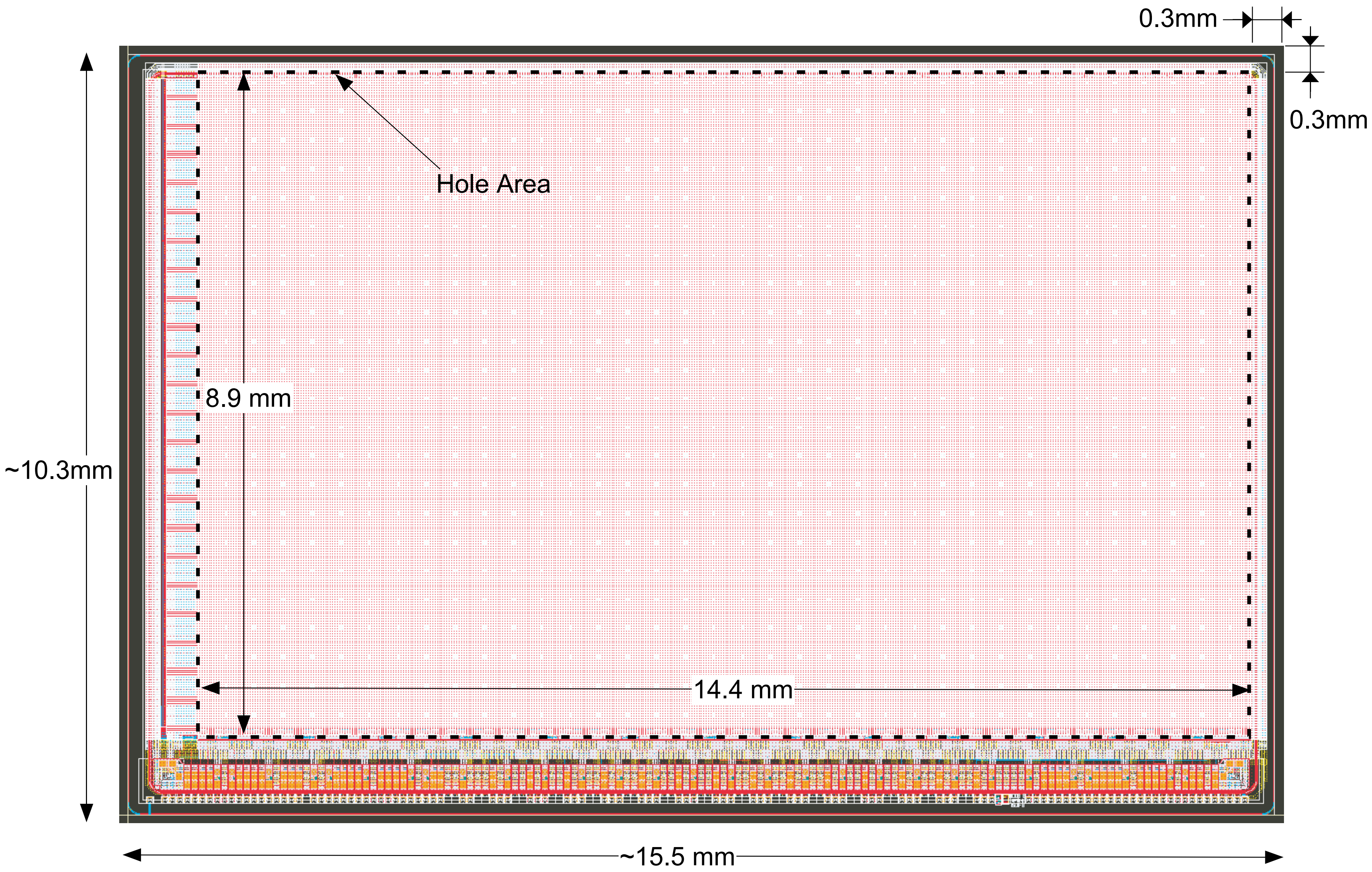
PAD pitch = 100 um

Location	PAD No.	I/O Buffer	Pad Name	Internal Signal	Comment
Left	1	pad90_4M_noM123	VDET	VDET	HV ring voltage
		–	–	–	
	2	S02_CORNER_VER2_L1P	VDD18	VDD18	1.8V VDD core
	3	S02_CORNER_VER2_L1P	VDD33	VDD33	3.3V VDD I/O
	4	S02_CORNER_VER2_L1P	VSS	VSS	Ground
Bottom	5	iod_L1P	IIN1	IIN1	Ref Current for VH2(VH), LOAD
	6	iod_L1P	IIN2	IIN2	Ref. Current for RBUF(VL), RBUF_SW
	7	S02_IT4N_L1P	ENBIAS1_x	IENBIAS1_x	enable LOAD
	8	S02_IT4N_L1P	ENBIAS2_x	IENBIAS2_x	enable RBUF_SW(AOUT0-12)
	9	S02_VDD18_L1P	VDD18	VDD18	1.8V VDD core
	10	S02_VSS_L1P	VSS	VSS	Ground
	11	S02_VDD33_L1P	VDD33	VDD33	3.3V VDD I/O
	12	iod_L1P	VH	VH	VH monitor
	13	iod_L1P	VL	VL	VL monitor
	14	iod_L1P	BPWCIR	BPWCIR	BPW for peripheral circuit
	15	iod_L1P	PIXRING	PIXRING	PSUB ring around pixel array
	16	S02_VDD18_L1P	VDD18	VDD18	1.8V VDD core
	17	S02_VSS_L1P	VSS	VSS	Ground
	18	S02_IT4N_L1P	RST	irst	Reset Signal
	19	S02_IT4N_L1P	RST_CDS	irst_cds	CDS Reset Signal
	20	S02_IT4N_L1P	STORE	istore	STORE signal
		iofill_L1P	–		
	21	S02_VDD18_L1P	VDD18	VDD18	1.8V VDD core
	22	S02_VSS_L1P	VSS	VSS	Ground
	23	S02_VDD33_L1P	VDD33	VDD33	3.3V VDD I/O
	24	S02_IT4N_L1P	RA0	IRA0	Row Address 0
	25	S02_IT4N_L1P	RA1	IRA1	Row Address 1
	26	S02_IT4N_L1P	RA2	IRA2	Row Address 2
	27	S02_IT4N_L1P	RA3	RIA3	Row Address 3
	28	S02_VDD18_L1P	VDD18	VDD18	1.8V VDD core
	29	S02_VSS_L1P	VSS	VSS	Ground
	30	S02_IT4N_L1P	RA4	IRA4	Row Address 4
	31	S02_IT4N_L1P	RA5	IRA5	Row Address 5
	32	S02_IT4N_L1P	RA6	IRA6	Row Address 6
	33	S02_IT4N_L1P	RA7	IRA7	Row Address 7
	34	S02_VDD18_L1P	VDD18	VDD18	1.8V VDD core
	35	S02_VSS_L1P	VSS	VSS	Ground
	36	S02_VDD33_L1P	VDD33	VDD33	3.3V VDD I/O
	37	S02_IT4N_L1P	RA8	IRA8	Row Address 8
	38	S02_IT4N_L1P	RAEN_x	IRAEN_x	Row Address Enable
		iofill_L1P	–	–	
		iofill_L1P	–	–	
	39	S02_VDD18_L1P	VDD18	VDD18	1.8V VDD core
	40	S02_VSS_L1P	VSS	VSS	Ground
		iofill_L1P	–	–	
		iofill_L1P	–	–	
	41	iod_L1P	AOUTA	AOUTA	All Analog Output
	42	S02_VSS_L1P	VSS	VSS	Ground
	43	S02_VDD18_L1P	VDD18	VDD18	1.8V VDD core

	iofill_L1P	–	–	
	iofill_L1P	–	–	
44	iod_L1P	AOUT0	AOUT0	Bank 0 Analog Output
45	S02_VSS_L1P	VSS	VSS	Ground
46	S02_VDD18_L1P	VDD18	VDD18	1.8V VDD core
	iofill_L1P	–	–	
	iofill_L1P	–	–	
47	iod_L1P	AOUT1	AOUT1	Bank 1 Analog Output
48	S02_VSS_L1P	VSS	VSS	Ground
49	S02_VDD18_L1P	VDD18	VDD18	1.8V VDD core
	iofill_L1P	–	–	
	iofill_L1P	–	–	
50	iod_L1P	AOUT2	AOUT2	Bank 2 Analog Output
51	S02_VSS_L1P	VSS	VSS	Ground
52	S02_VDD18_L1P	VDD18	VDD18	1.8V VDD core
	iofill_L1P	–	–	
	iofill_L1P	–	–	
53	iod_L1P	AOUT3	AOUT3	Bank 3 Analog Output
54	S02_VSS_L1P	VSS	VSS	Ground
55	S02_VDD18_L1P	VDD18	VDD18	1.8V VDD core
	iofill_L1P	–	–	
	iofill_L1P	–	–	
56	iod_L1P	AOUT4	AOUT4	Bank 4 Analog Output
57	S02_VSS_L1P	VSS	VSS	Ground
58	S02_VDD18_L1P	VDD18	VDD18	1.8V VDD core
	iofill_L1P	–	–	
	iofill_L1P	–	–	
59	iod_L1P	AOUT5	AOUT5	Bank 5 Analog Output
60	S02_VSS_L1P	VSS	VSS	Ground
61	S02_VDD18_L1P	VDD18	VDD18	1.8V VDD core
	iofill_L1P	–	–	
	iofill_L1P	–	–	
62	iod_L1P	AOUT6	AOUT6	Bank 6 Analog Output
62	S02_VSS_L1P	VSS	VSS	Ground
64	S02_VDD18_L1P	VDD18	VDD18	1.8V VDD core
	iofill_L1P	–	–	
	iofill_L1P	–	–	
65	iod_L1P	AOUT7	AOUT7	Bank 7 Analog Output
66	S02_VSS_L1P	VSS	VSS	Ground
67	S02_VDD18_L1P	VDD18	VDD18	1.8V VDD core
	iofill_L1P	–	–	
	iofill_L1P	–	–	
68	iod_L1P	AOUT8	AOUT8	Bank 8 Analog Output
69	S02_VSS_L1P	VSS	VSS	Ground
70	S02_VDD18_L1P	VDD18	VDD18	1.8V VDD core
	iofill_L1P	–	–	
	iofill_L1P	–	–	
71	iod_L1P	AOUT9	AOUT9	Bank 9 Analog Output
72	S02_VSS_L1P	VSS	VSS	Ground
73	S02_VDD18_L1P	VDD18	VDD18	1.8V VDD core
	iofill_L1P	–	–	
	iofill_L1P	–	–	

	74	iod_L1P	AOUT10	AOUT10	Bank 10 Analog Output
	75	S02_VSS_L1P	VSS	VSS	Ground
	76	S02_VDD18_L1P	VDD18	VDD18	1.8V VDD core
		iofill_L1P	–	–	
		iofill_L1P	–	–	
	77	iod_L1P	AOUT11	AOUT11	Bank 11 Analog Output
	78	S02_VSS_L1P	VSS	VSS	Ground
	79	S02_VDD18_L1P	VDD18	VDD18	1.8V VDD core
		iofill_L1P	–	–	
		iofill_L1P	–	–	
	80	iod_L1P	AOUT12	AOUT12	Bank 12 Analog Output
	81	S02_VSS_L1P	VSS	VSS	Ground
	82	S02_VDD18_L1P	VDD18	VDD18	1.8V VDD core
		iofil2l_L1P	–	–	
		iofil2l_L1P	–	–	
		iofil2l_L1P	–	–	
		iofil2l_L1P	–	–	
	83	S02_VDD18_L1P	VDD18	VDD18	1.8V VDD core
	84	S02_VSS_L1P	VSS	VSS	Ground
	85	S02_IT4N_L1P	CA0	ICA0	Column Address 0
	86	S02_IT4N_L1P	CA1	ICA1	Column Address 1
	87	S02_IT4N_L1P	CA2	ICA2	Column Address 2
	88	S02_IT4N_L1P	CA3	ICA3	Column Address 3
	89	S02_VDD18_L1P	VDD18	VDD18	1.8V VDD core
	90	S02_VSS_L1P	VSS	VSS	Ground
	91	S02_VDD33_L1P	VDD33	VDD33	3.3V VDD I/O
	92	S02_IT4N_L1P	CA4	ICA4	Column Address 4
	93	S02_IT4N_L1P	CA5	ICA5	Column Address 5
	94	S02_IT4N_L1P	CA6	ICA6	Column Address 6
	95	S02_IT4N_L1P	CA7	ICA7	Column Address 7
	96	S02_VDD18_L1P	VDD18	VDD18	1.8V VDD core
	97	S02_VSS_L1P	VSS	VSS	Ground
	98	S02_IT4N_L1P	CA8	ICA8	Column Address 8
	99	S02_IT4N_L1P	CA9	ICA9	Column Address 9
	100	S02_IT4N_L1P	CAEN	ICAEN	Column Address Enable
	101	S02_OT4A_L1P	CAENO	ICAEN	Column Address Enable Output
	102	S02_VDD18_L1P	VDD18	VDD18	1.8V VDD core
	103	S02_VSS_L1P	VSS	VSS	Ground
	104	S02_VDD33_L1P	VDD33	VDD33	3.3V VDD I/O
	105	iod_L1P	V_RST_CDS	V_RST_CDS	RST_CDS voltage
	106	iod_L1P	V_RST	V_RST	RST voltage
	107	S02_VSS_L1P	VSS	VSS	Ground
	108	S02_OT4A_L1P	RA0OUT_x	IRA0x	Row Address 0 output
Right	109	S02_CORNER_VER2_L1	VSS	VSS	Ground
	110	S02_CORNER_VER2_L1	VDD33	VDD33	3.3V VDD I/O
	111	S02_CORNER_VER2_L1	VDD18	VDD18	1.8V VDD core
		–	–	–	
	112	pad90_4M_noM123	VBIAS	VBIAS	Bias ring voltage

Location	PAD No.	I/O Buffer	Pad Name	Input Signal	Comment
Back	–	–	VBACK	VBACK	Chip backside connection



INTPIX4 Chip size and PC hole size