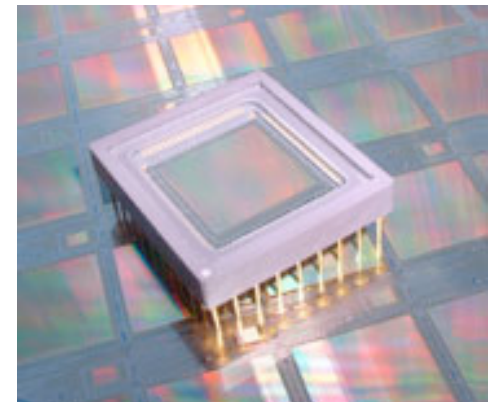


測定器開発:シリコン検出器

Monolithic Pixel Detector 開発 (まとめと提案)

2005.4.25 測定器W.S.
新井康夫(KEK)

- Silicon検出器R & D:何を狙うか？
- SOI(Silicon On Insulator) 技術
- Pixel Electronics
- まとめと提案



a "dream" of detector physicist

1. (high Z) semiconductor sensor

with

2. fully integrated ampl. circuitry and R/O logic

using

3. commercially available CMOS technologies

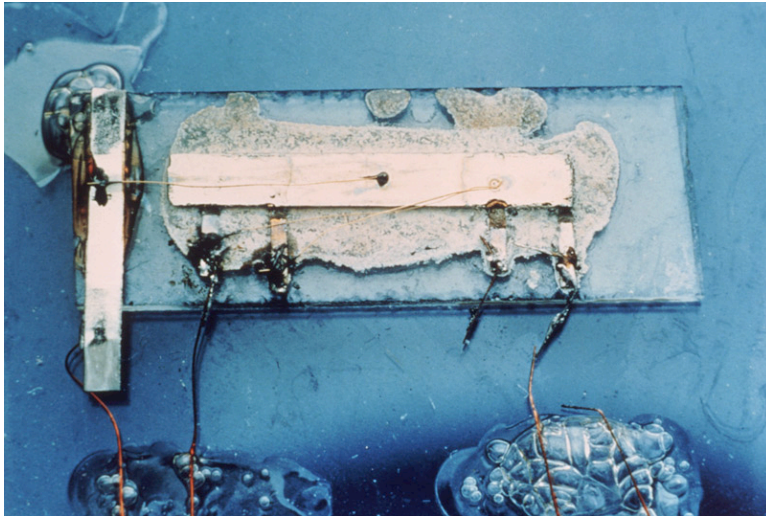
海野さんの夢を
実現させるには。。。

- KEK有志で議論(ATLAS: 海野、池上、寺田、新井、 BELL: 坪山、杉本、川崎、田島、 LC: 杉本)
- 高精度、高分解能、高速、薄型、耐放射線性
--> Strip から Pixelへ, Hybrid から Monolithicへ
==> Monolithic Pixel Detector を SOI技術をベースに開発する。
- X線検出器等、応用分野も広い。

主な Monolithic Pixel Detector 技術

	Resolution	Speed	Radiation tolerance	Process (Cost)	S/N	プロセス の利用し やすさ
CCD	◎	△	△	やや特殊	○	2
CMOS APS	◎	○	○	汎用	△	1
SOI (Silicon On Insulator)	◎	◎	◎	一部特殊	◎	3
DEPFET	◎	○	○	非常に特殊	◎	4
TFA (Thin-Film on ASIC)	○	△	○	非常に特殊	△	5

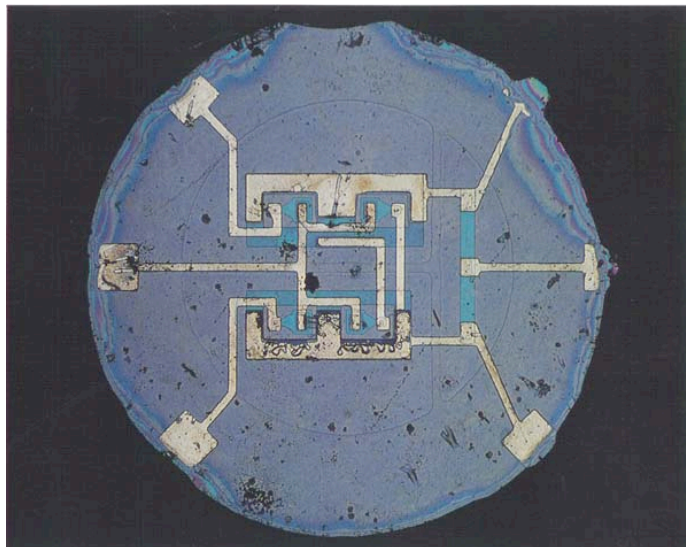
LSI開発者の夢。。。



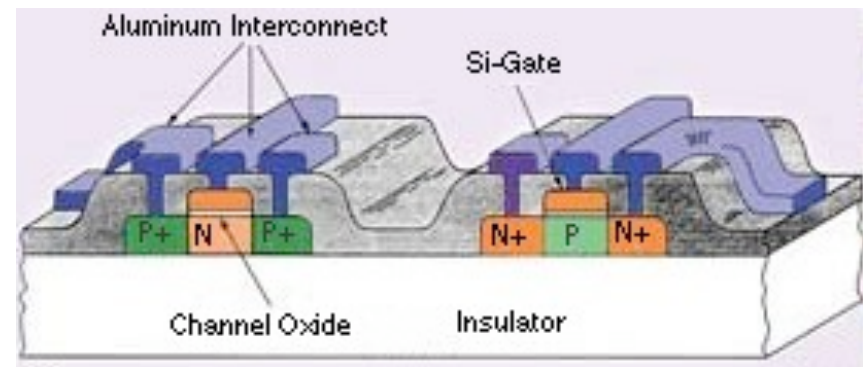
First MOSFET(~SOI)
(1926 Lilienfield)

First Integrated Circuit
(1958 J. Kirby)

First Planar IC
(1959 R. Noyce)



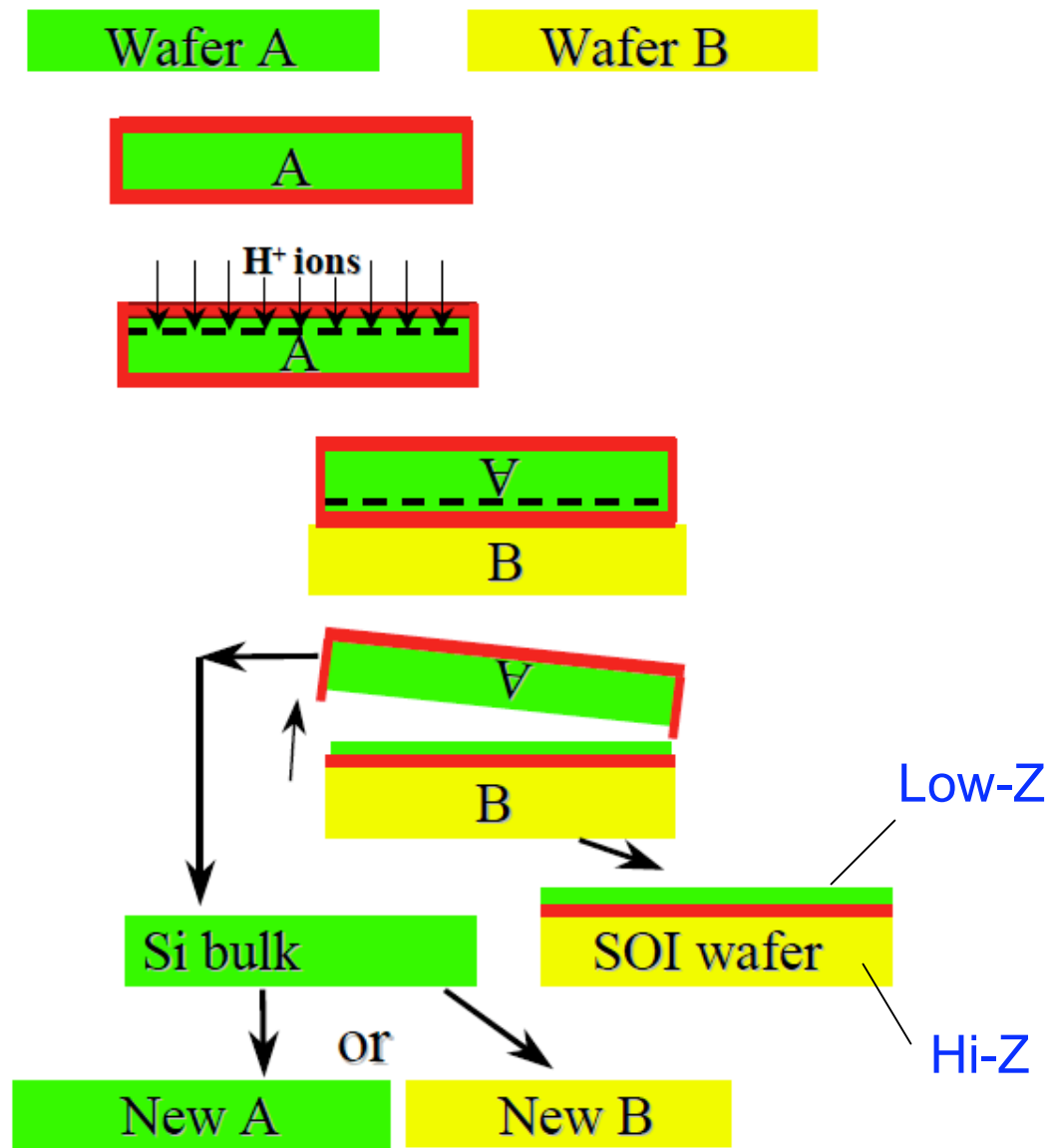
Ideal IC Structure:SOI
(1998~ IBM...)



トランジスタが完全に分離。余計なpn-junctionがない。

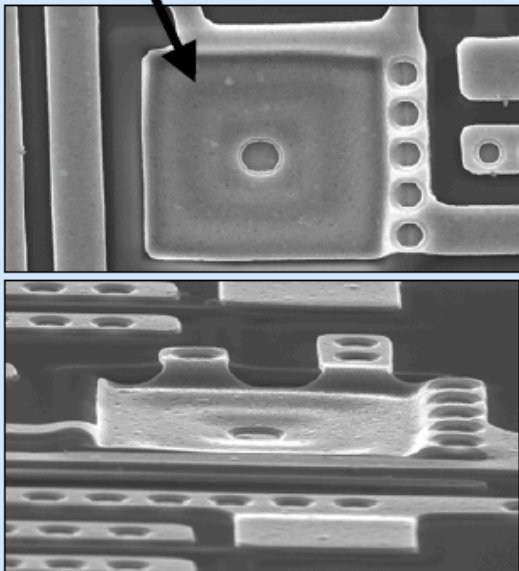
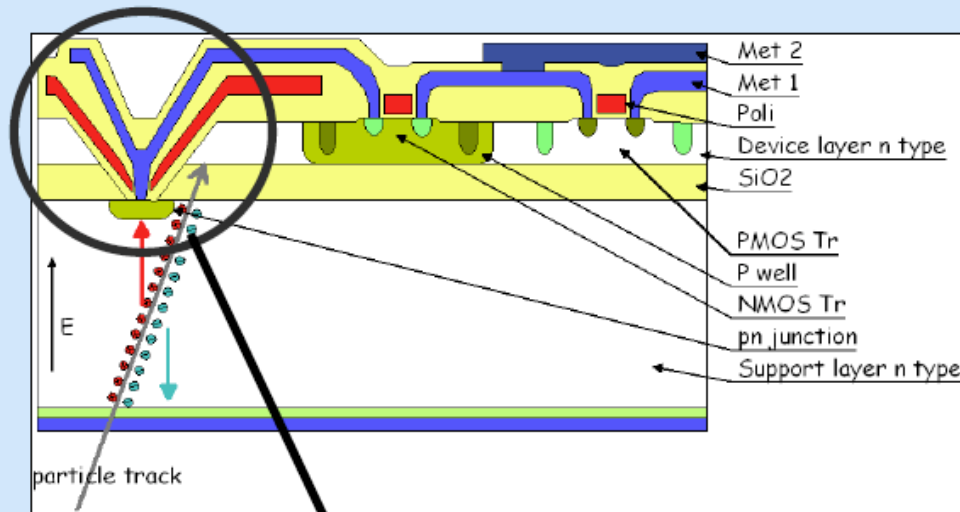
SOIウェハーの作り方: Smart Cut (UNIBOND)

- ① Initial silicon wafers A & B
- ② Oxidation of wafer A to create insulating layer
- ③ Smart Cut ion implantation induces formation of an in-depth weakened layer
- ④ Cleaning & bonding wafer A to the handle substrate, wafer B
- ⑤ Smart Cut - cleavage at the mean ion penetration depth splits off wafer A
- ⑥ Wafer B undergoes annealing, CMP and touch polish => SOI wafer complete
- ⑧ Split-off wafer A is recycled, becoming the new wafer A or B





Principle of SOI monolithic detector



The idea:

Integration of the pixel detector and readout electronics in the wafer-bonded SOI substrate

Electronics → Device layer

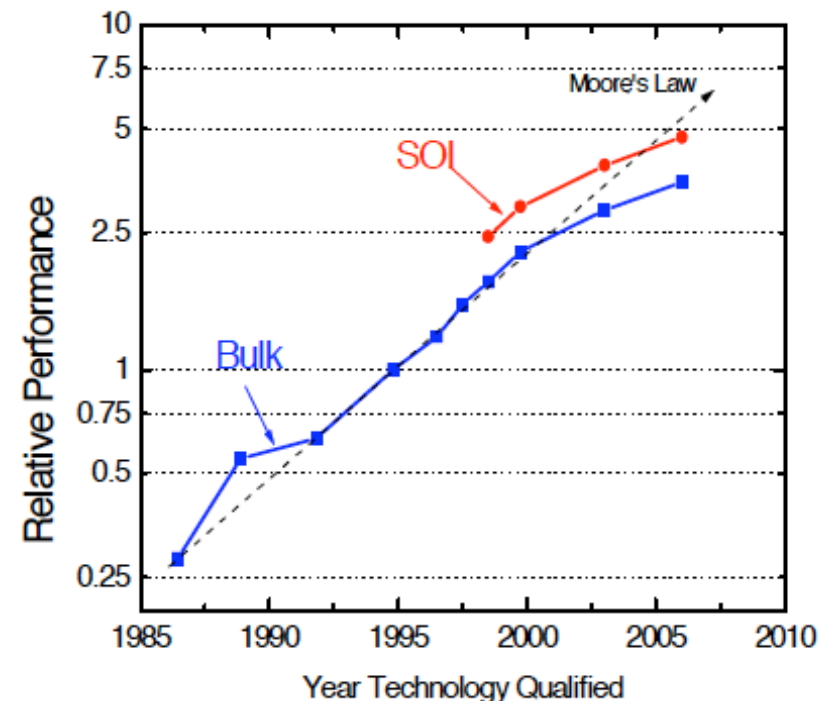
- Low resistive
(9-13 Ωcm , CZ)
- 1.5 μm thick
- Standard CMOS technology

Detector → Support layer

- High resistive
($> 4 \text{ k}\Omega\text{cm}$, FZ)
- 300 μm thick
- Conventional p⁺-n
- DC-coupled

SOI Pixel開発の利点

- SOIはセンサー部とエレクトロニクス部で抵抗値の違うSiウエハーを選択できるのでMonolithic Pixelとして理想的である。
- 高速、低消費電力、No latchup, Low Leak Current。
- 放射線に強い、薄くできる、高温(>300C)でも動作。
- SOI Pixelの開発を行っているグループはまだ少ない(Poland/Italy)。
- NTT, OKI等昔から日本技術者の多くがSOIの開発に寄与している。
- 今後LSIの主流はSOIデバイスになる(IBM PowerPC, CELL,AMD...)。



Pixel Electronics

ATLAS Pixel

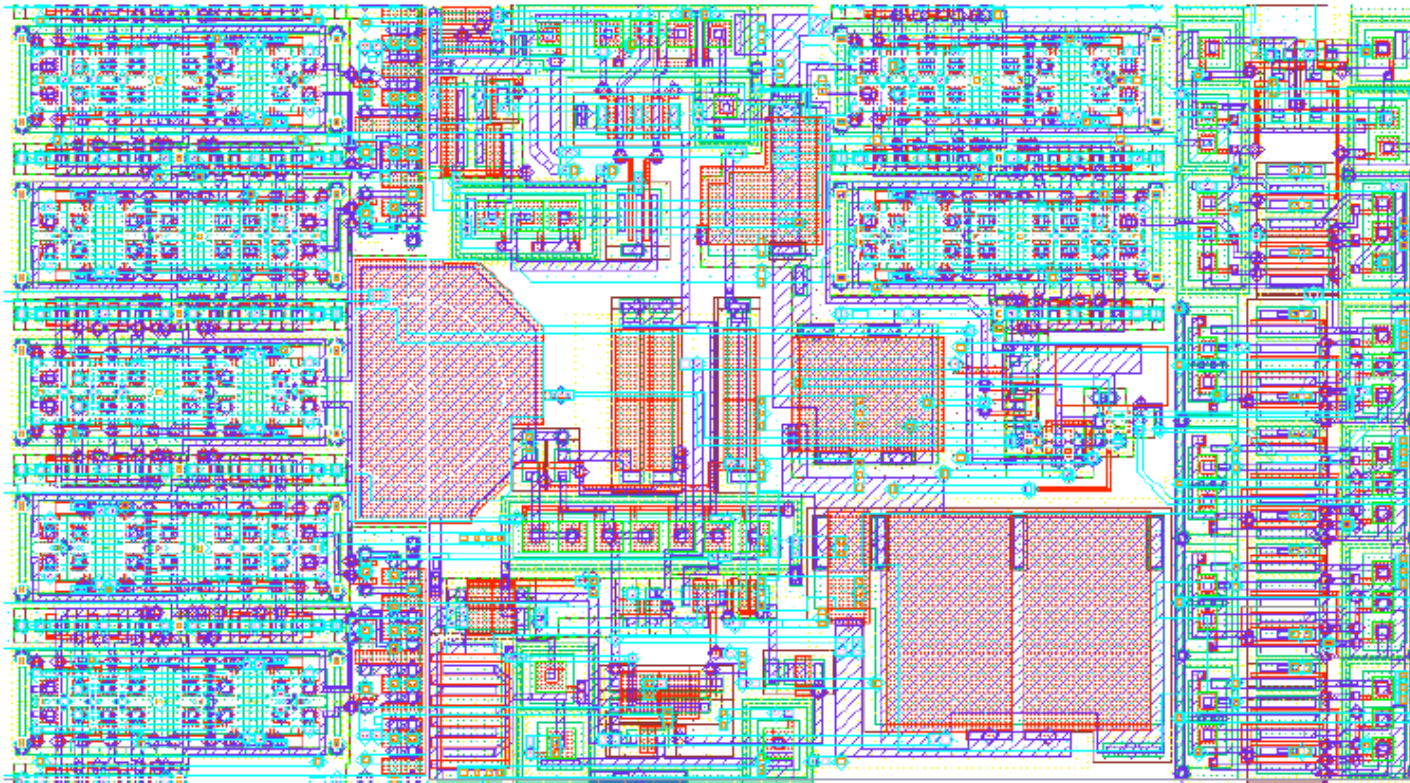
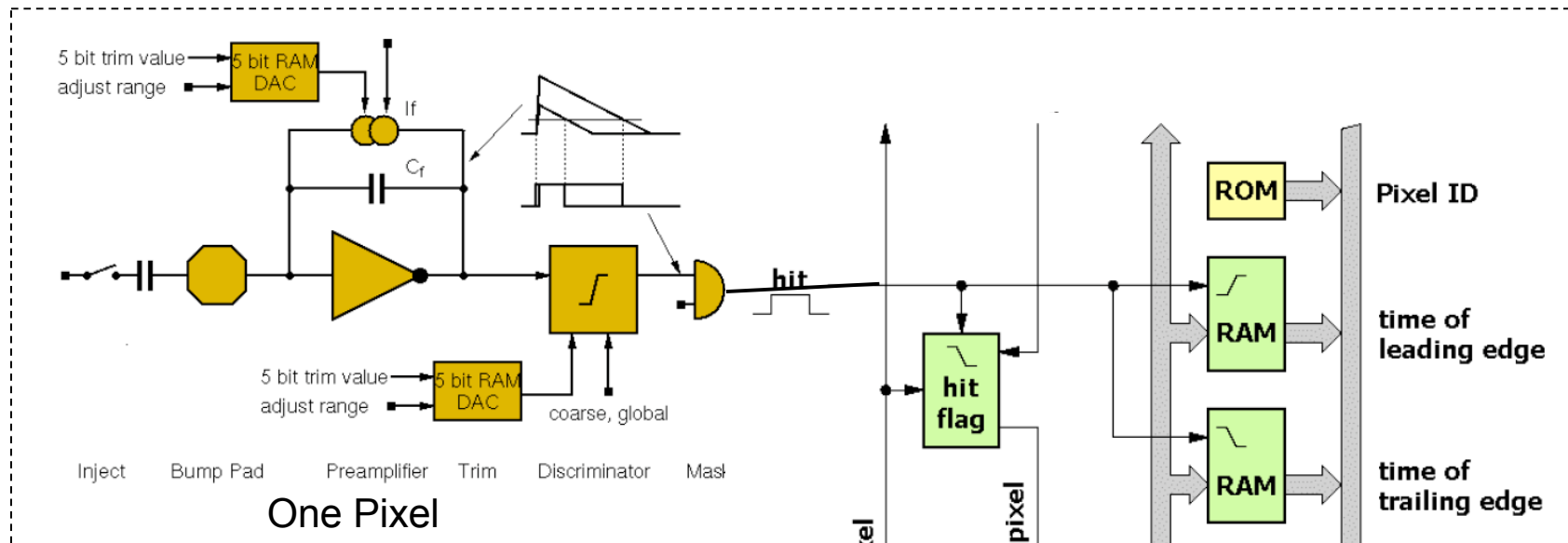
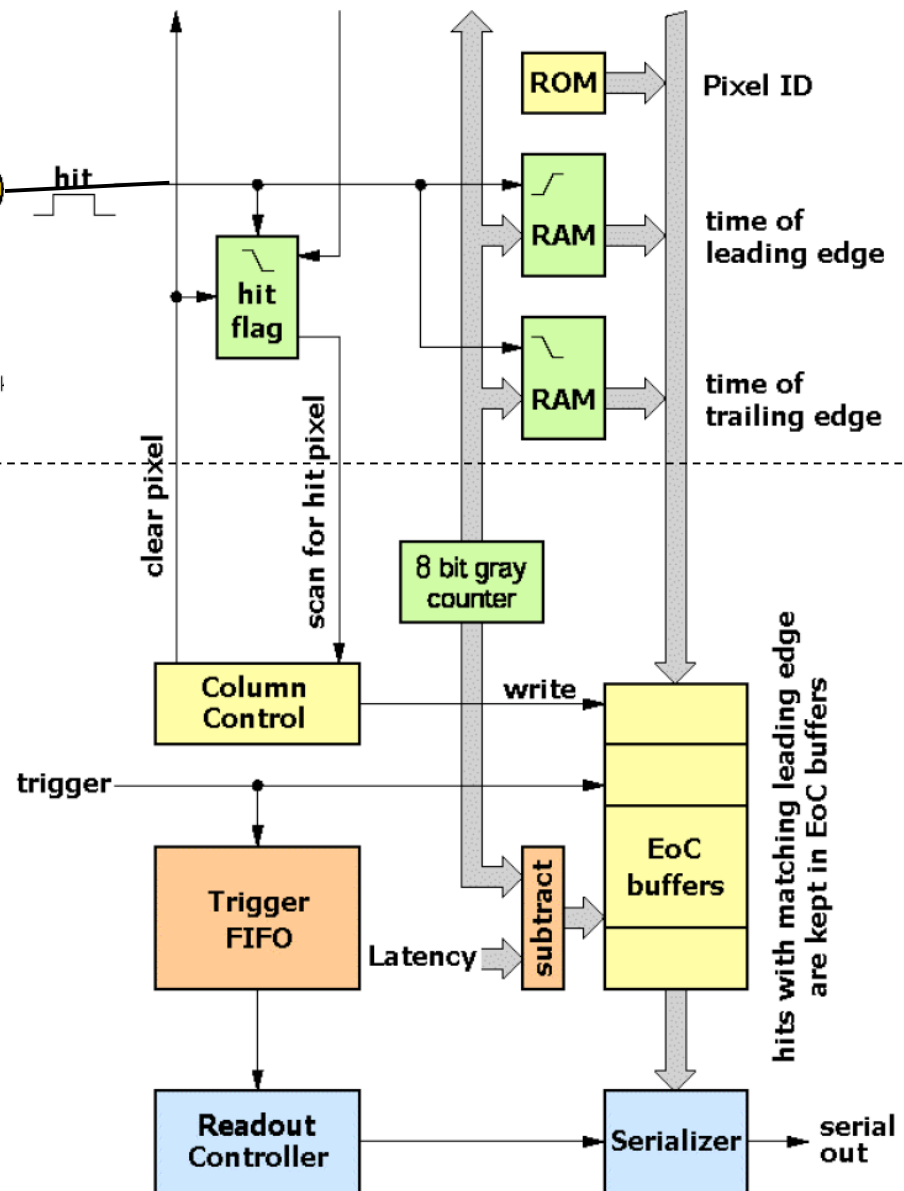


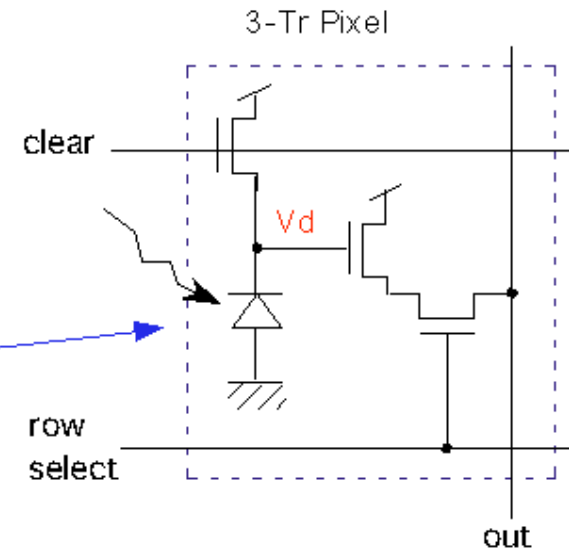
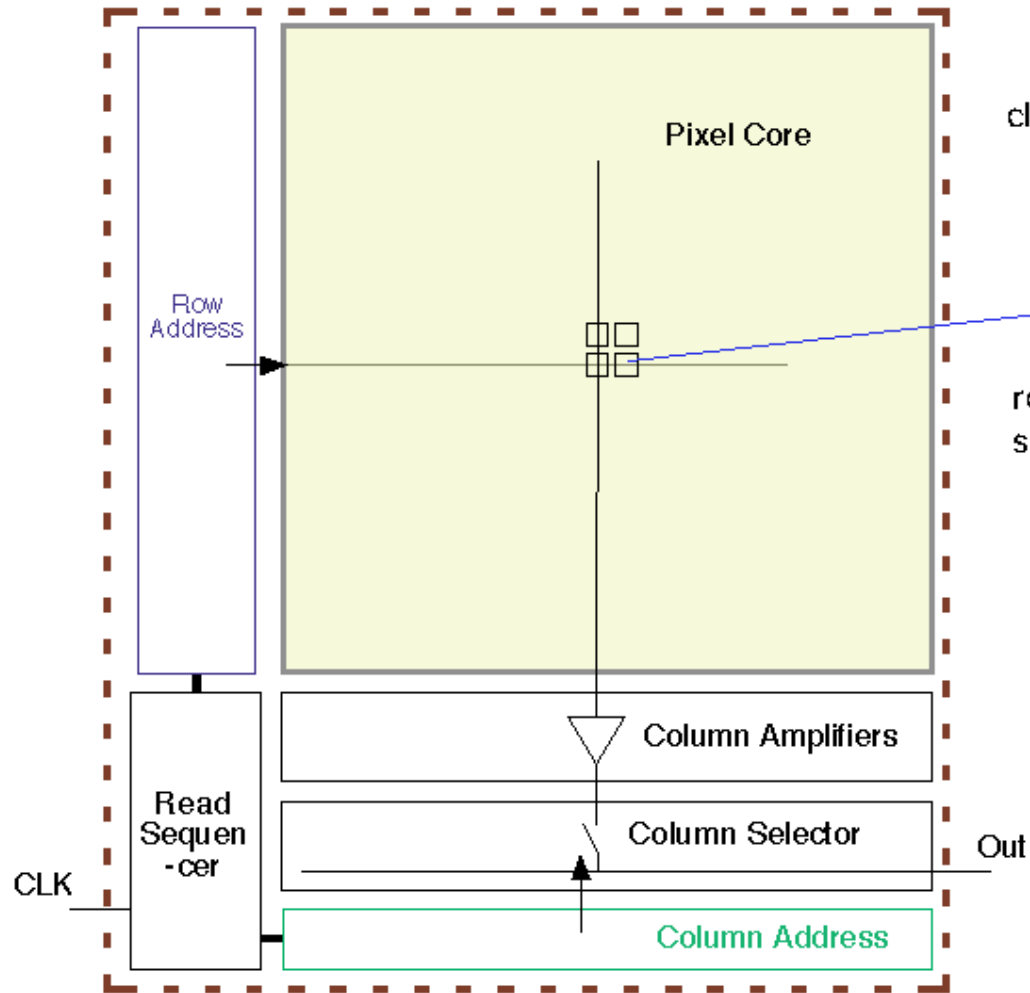
Figure 6: Layout of the analogue part + slow control of the pixel cell in FEI. This part is $50\mu\text{m}$ high and $90\mu\text{m}$ wide.



ATLAS Pixel Front End Electronics



CMOS Image Sensor

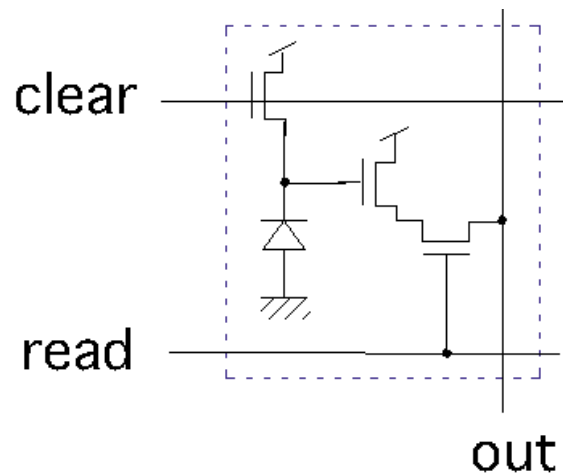
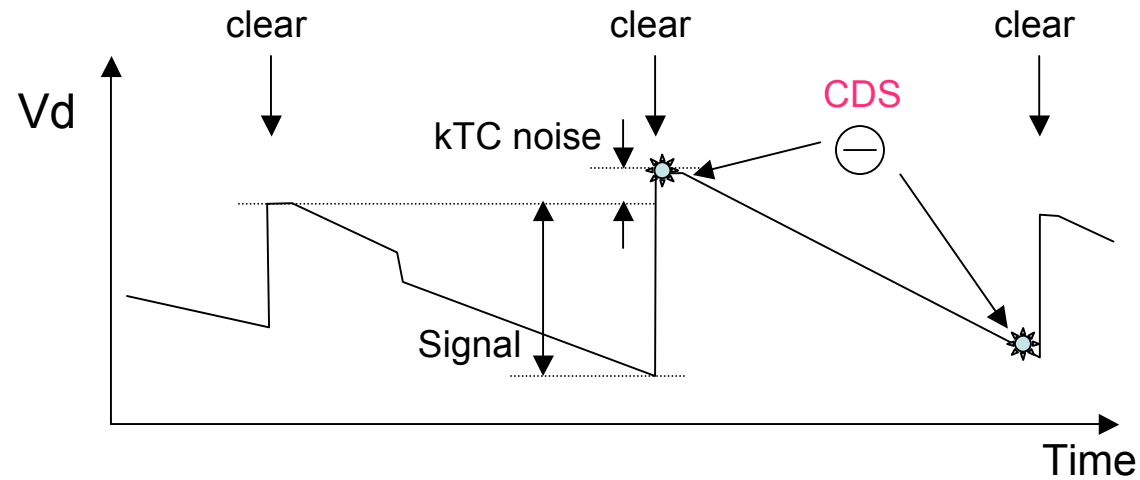


$$Signal = \frac{Q}{C} = \frac{1000e}{10fF} = 16mV$$

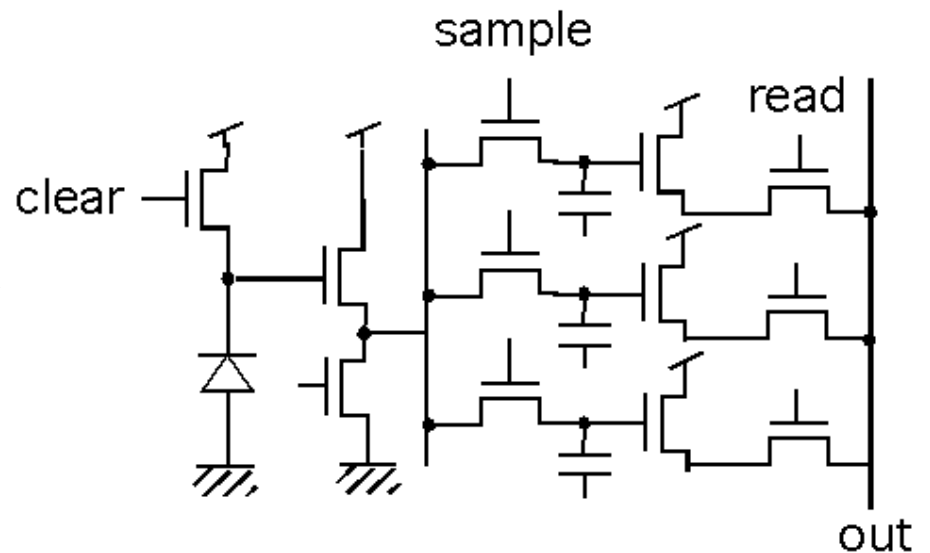
$$Noise = \sqrt{\frac{kT}{C}} = \sqrt{\frac{300k}{10fF}} = 0.64mV(40e)$$

$$S/N = \frac{1000}{40} = 25$$

Correlated Double Sampling & Pipelining



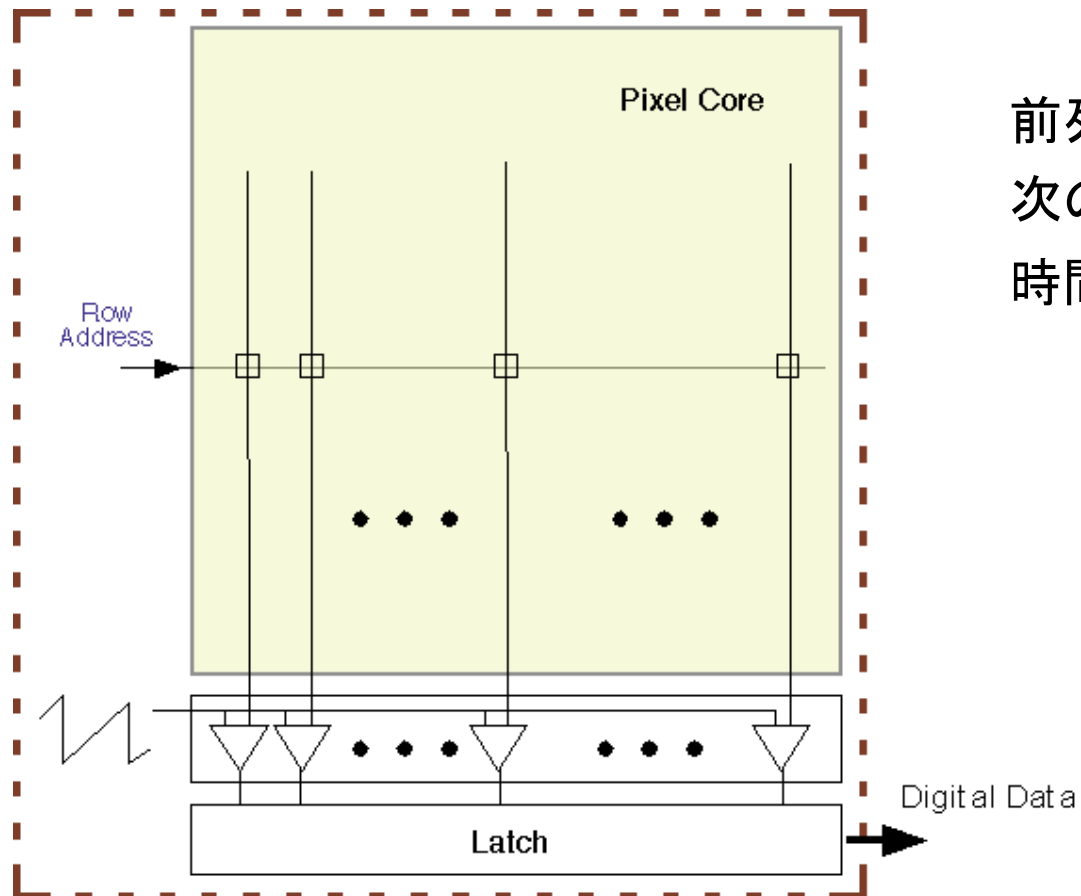
Pipeline



(CMOS APSではPMOSが使えない!)

高速化(1)

全ての列にADCを設ける (Parallel, Wilkinson ADC)。

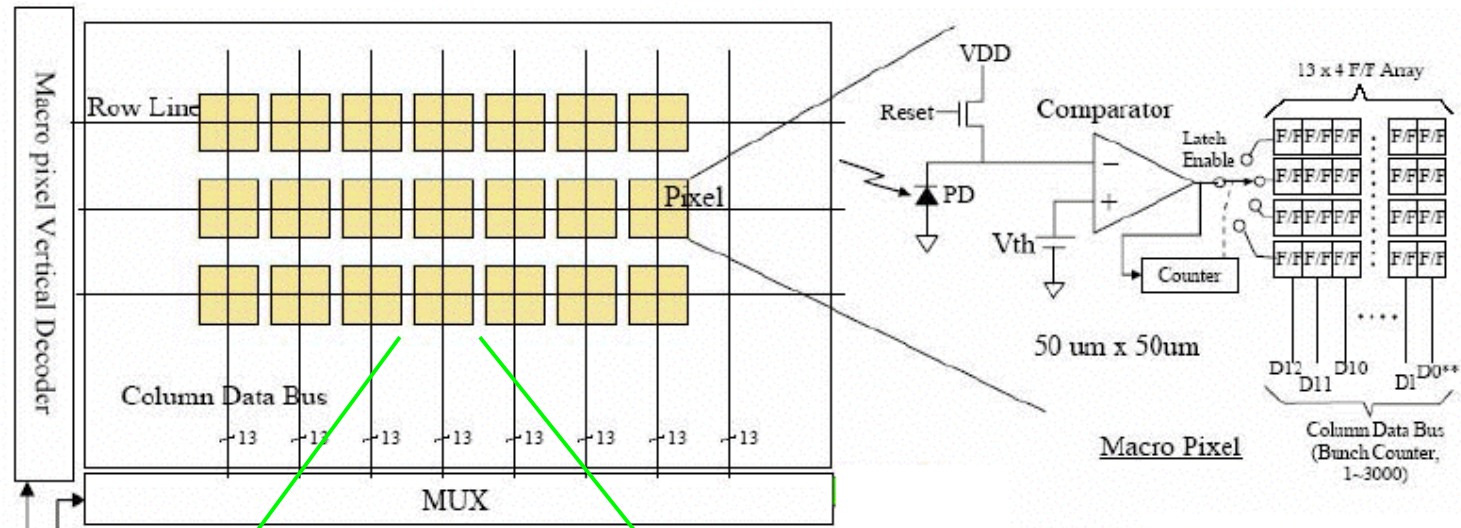


前列のデータを出力中に
次の列をAD変換する。
時間＝列数 x 1 Cycle

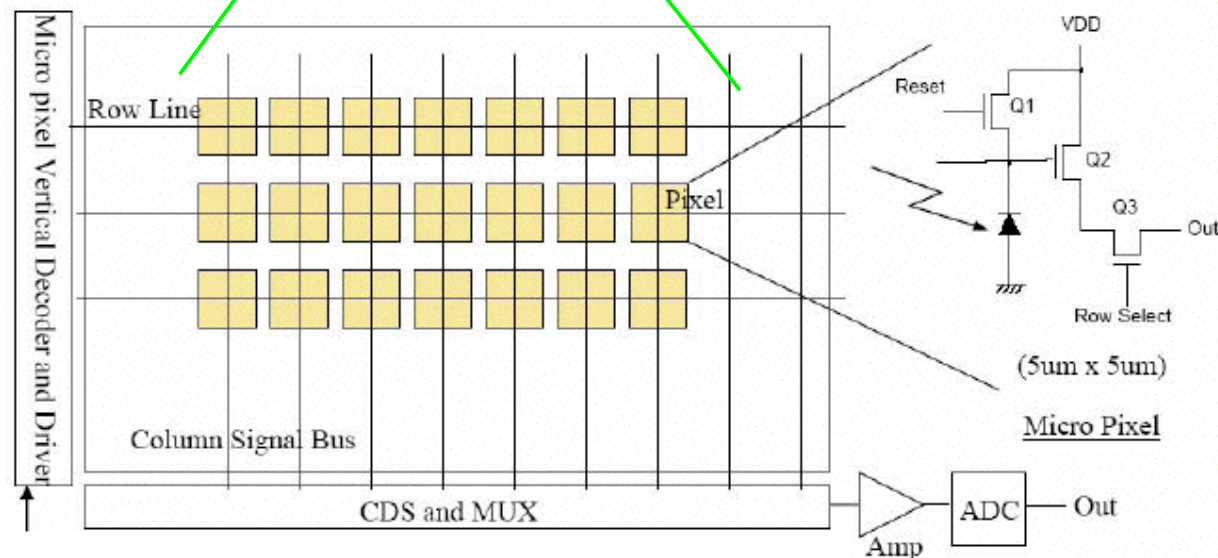
高速化(2):US Pixel R&D(Oregon, Yale...)

HitしたPixelのみ読み出す(Sparse Data Scan)。

Macro
Pixel

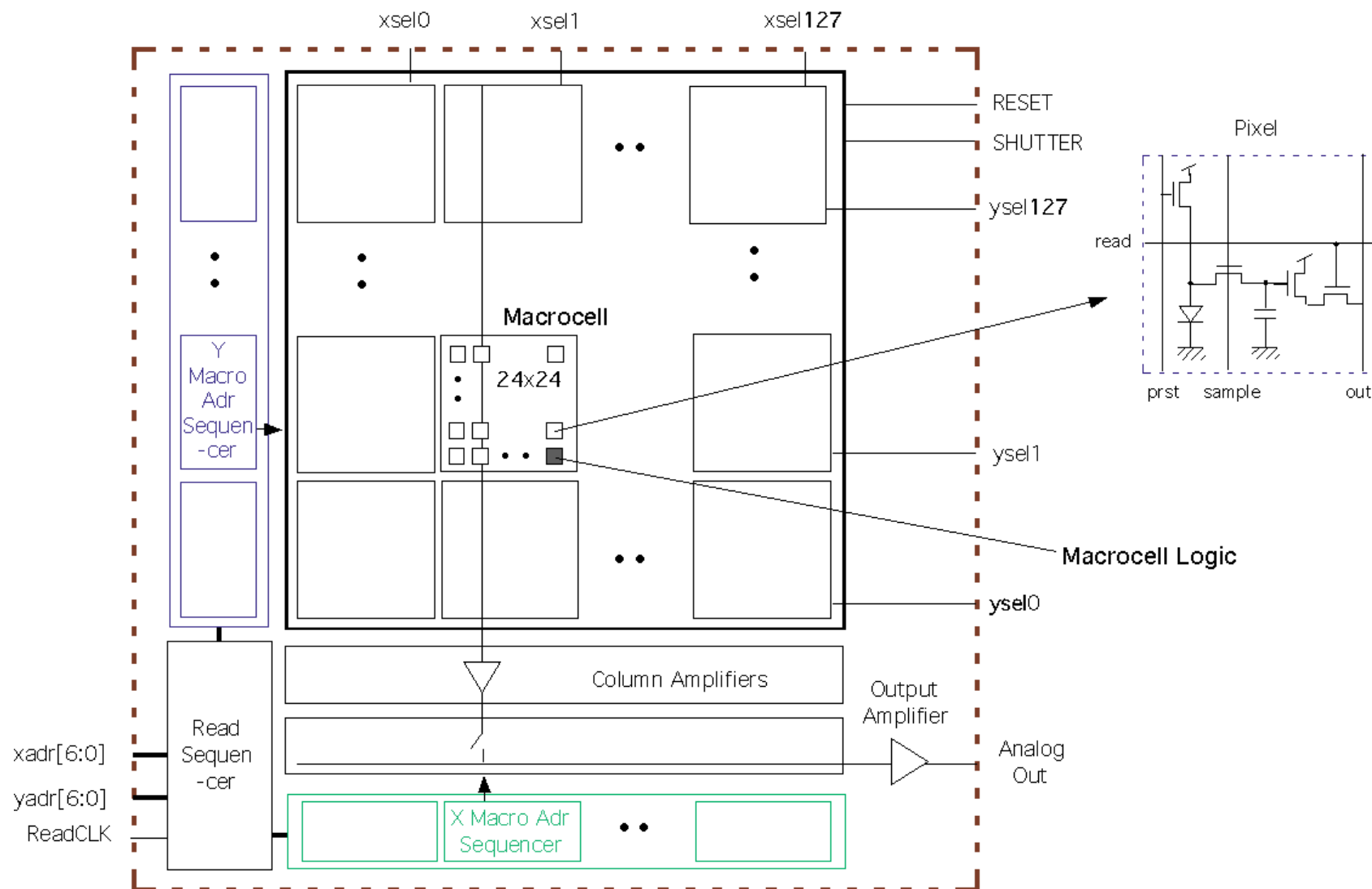


Micro
Pixel



2次元Macrocell

特開2005-51352
佐々木、青木(ICRR),新井(KEK)



まとめと提案

R&D方針

- **Monolithic Pixel**検出器の開発を行う。
- デバイス構造は **SOI**を第一候補とするが、他のデバイス構造も調査する。
- 3年でビームテストが行える所までを目標に。
- 既存資産(ATLAS, BELL,...)を有効活用。
- **他大学・研究所とも協力(参加歓迎！)**

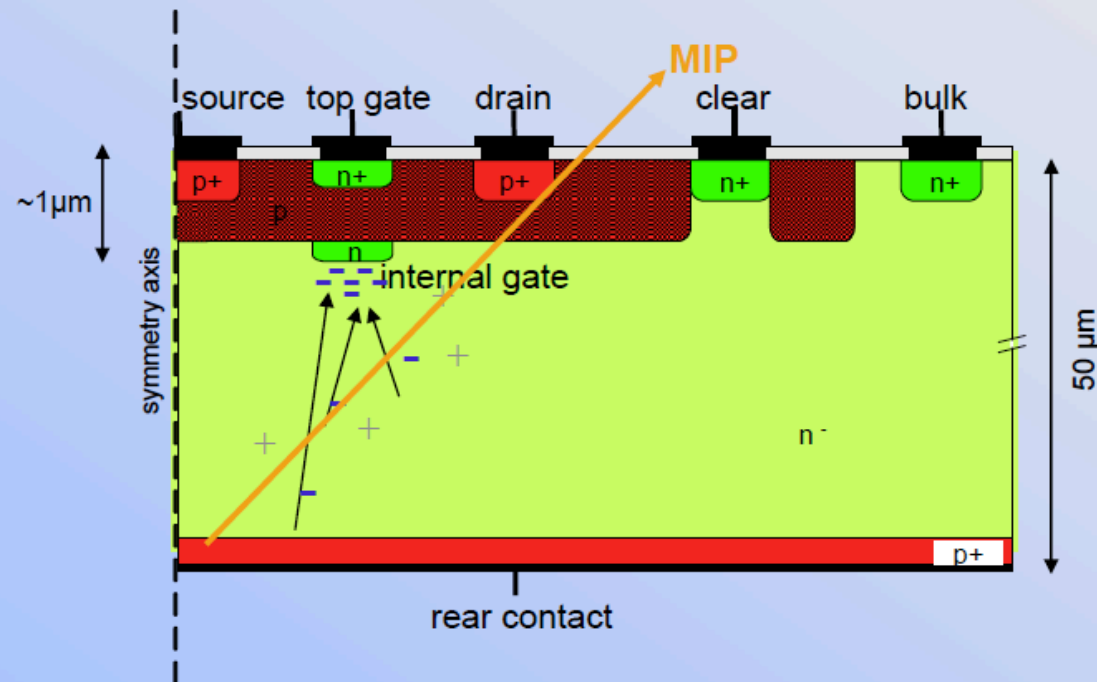
当面の計画案

- SOI Pixel開発に協力してくれる会社を探し、試作。
- TCADによるデバイスシミュレーション。
- 標準プロセスCMOS APSでの、エレクトロニクス技術開発。
- SOIの技術による薄型CCDの検討。
- 施設整備、Pixel Workshop出席等。

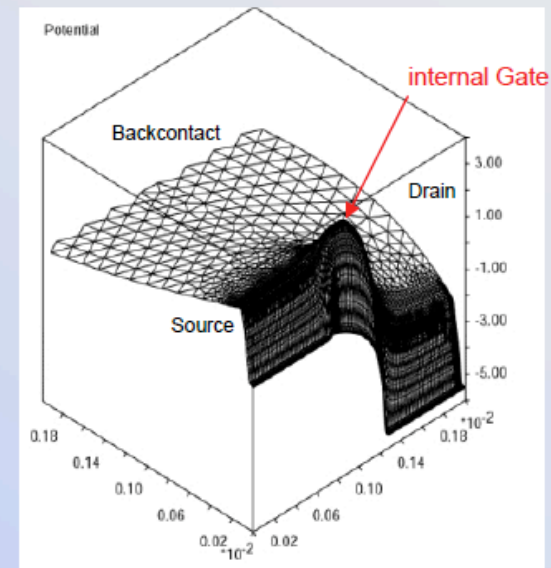
終わり

補足資料

DEPFET-Principle of Operation



Potential distribution:



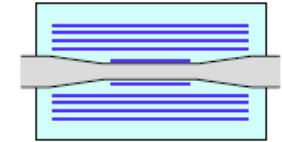
[TeSCA-Simulation]

- **FET-Transistor integrated in every pixel** (first amplification)
- **Electrons** are collected in „internal gate“ and modulate the transistor-current
- **Fully depleted substrate!**

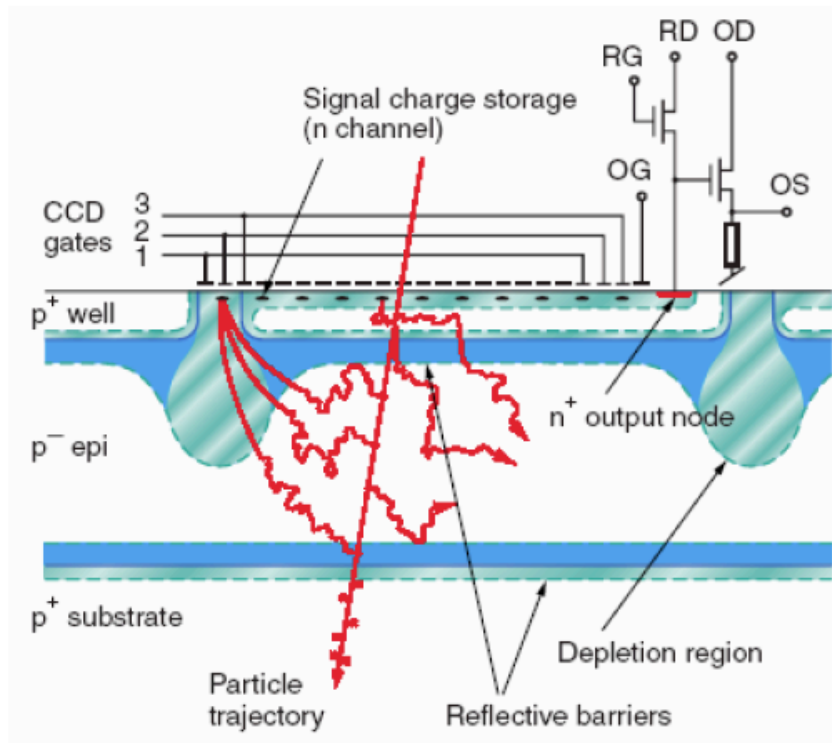


CCD

ISIS-based detector



for details cf. Chris Damerell's contribution to LCWS 2004
(session on "Tracking and Vertexing: Simulation Studies")



- **TESLA**: signals of 1000 e^- to be amplified & read;
so far envisaged 20 readouts / bunch train
- **SLC experience**:
may be impossible due to beam-related RF pickup

→ started to investigate alternative architecture:
variant of **In-situ Storage Image Sensor (ISIS)**

Idea:

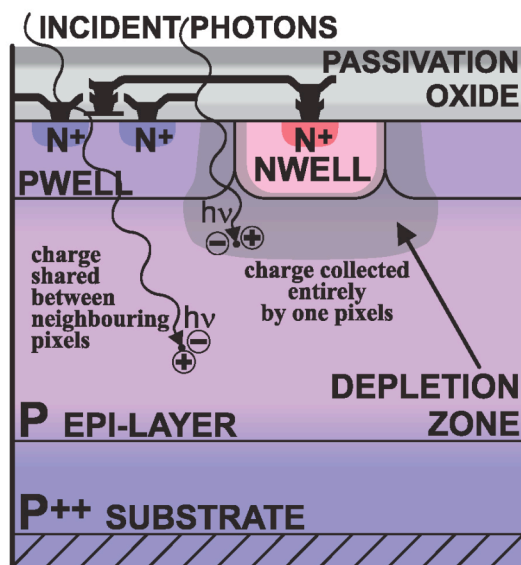
- charge collection on photogate
- in each pixel: linear CCD with 20 elements,
each storing charge collected during 1 time slice,
shifted on at 50 μs intervals

- during 200 ms between bunch trains: transfer of stored signals to local
charge sensing circuits in pixel, column-parallel readout at moderate rate, e.g. 1MHz

CMOS APS

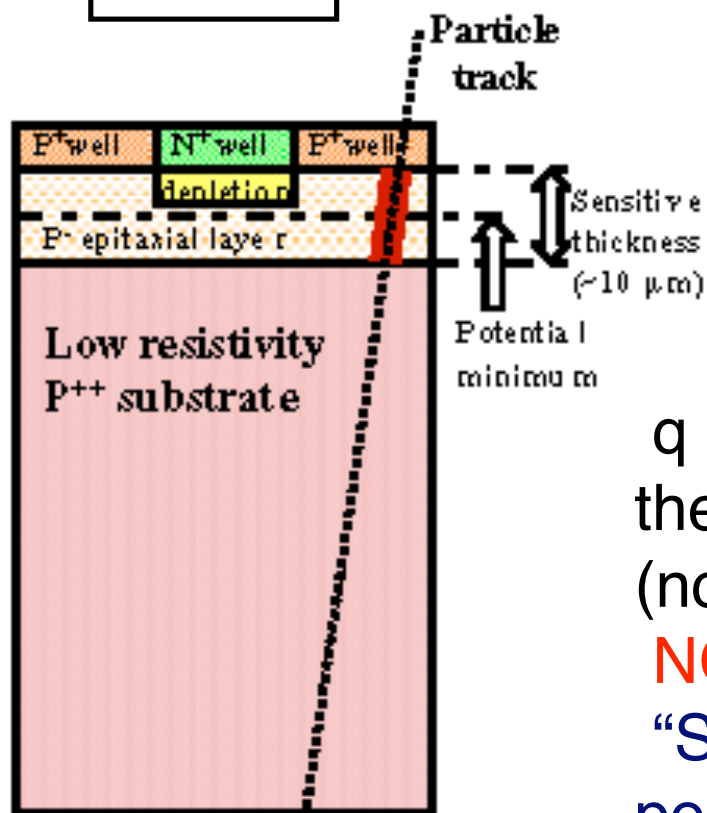
(from G. Varner, U of Hawaii)

CMOS Camera



Because of large Capacitance, need Thick DSSDs
-- APS can be VERY Thin

Particle Detector



Standard CMOS:

Low Power
Excellent Transistors
Tight Process Control
Excellent Uniformity
High volume, low cost
Large ADC, DSP base

Key Features:

q collection via thermal diffusion
(no HV)

NO bump bonding
“System on Chip” possible