SOI Pixel Development at KEK

Sep. 26, 2008 @Pixel 2008

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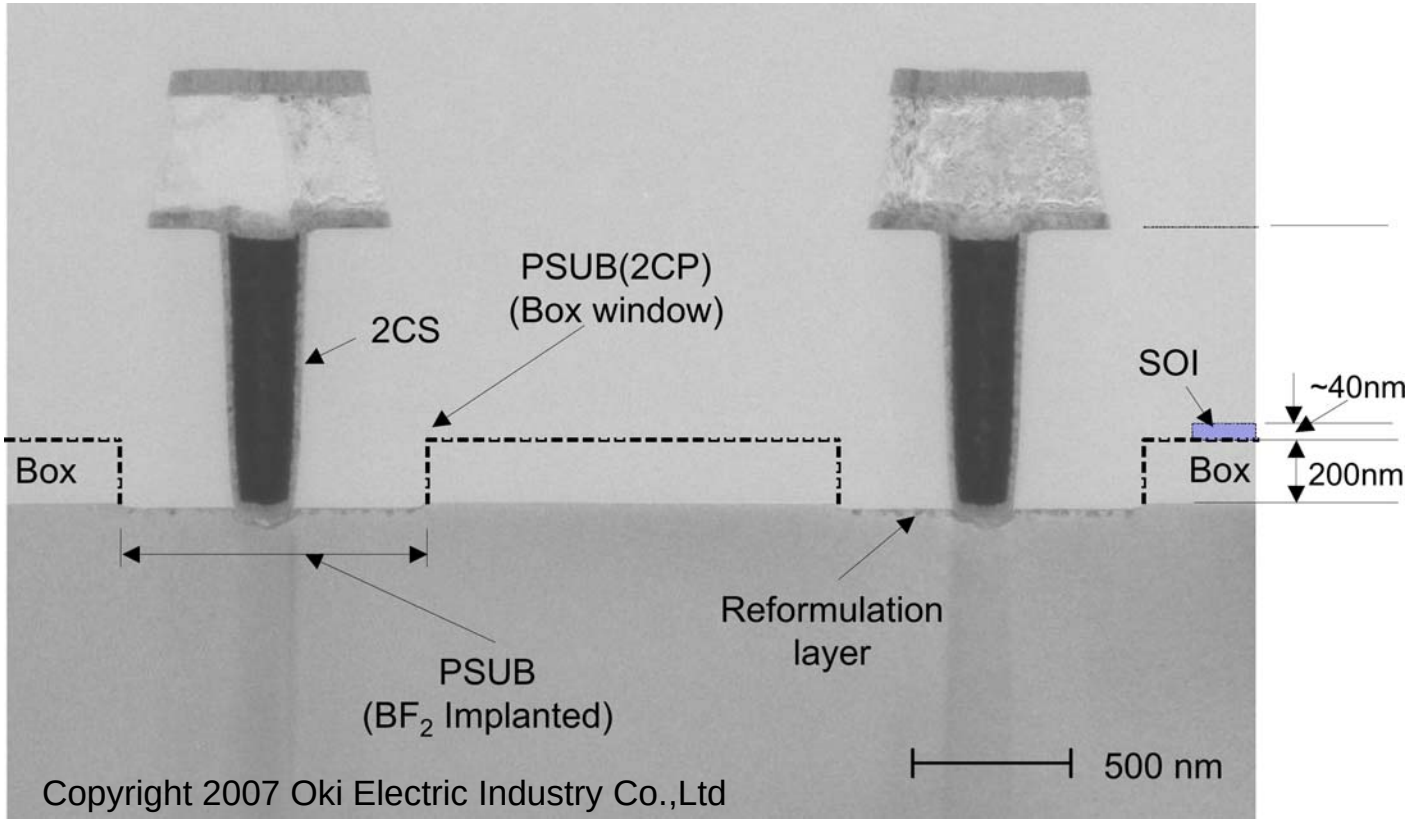
[SOI Pixel Collaboration]

- **KEK** : Y. Unno, S. Terada, Y. Ikegami, T. Tsuboyama, T. Kohriki, K. Tauchi, Y. Ikemoto, T. Miyoshi, Y. Arai
- **U. of Tsukuba** : K. Hara, H. Miyake, M. Kouchiyama, T. Sega
- **Osaka U.** : K. Hanagaki, M. Hirose
- **JAXA/ISAS** : H, Ikeda, D. Kobayashi, T. Wada, H. Nagata
- **Tohoku U.** : H. Yamamoto, Y. Horii
- **Kyoto U.** : T. Tsuru
- **Riken/JASRI** : T. Hatsui, T. Kudo, R. Ichimiya, A. Taketani
- **U. of Hawaii** : G. Varner, J. Kennedy, M. Cooney, H. Hoedlmoser, E. Martin
- **LBNL** : P. Denes, M. Battaglia, C. Vu, D. Contarato, P. Giubilato, L. Glesener
- **FNAL** : R. Yarema, R. Lipton, G. Deptuch, M. Trimpl
- **OKI Elec. Ind. Co. Ltd.** : M. Ohno, K. Fukuda, J. Ida, H. Hayashi, Y. Kawai, M. Okihara, H. Komatsubara

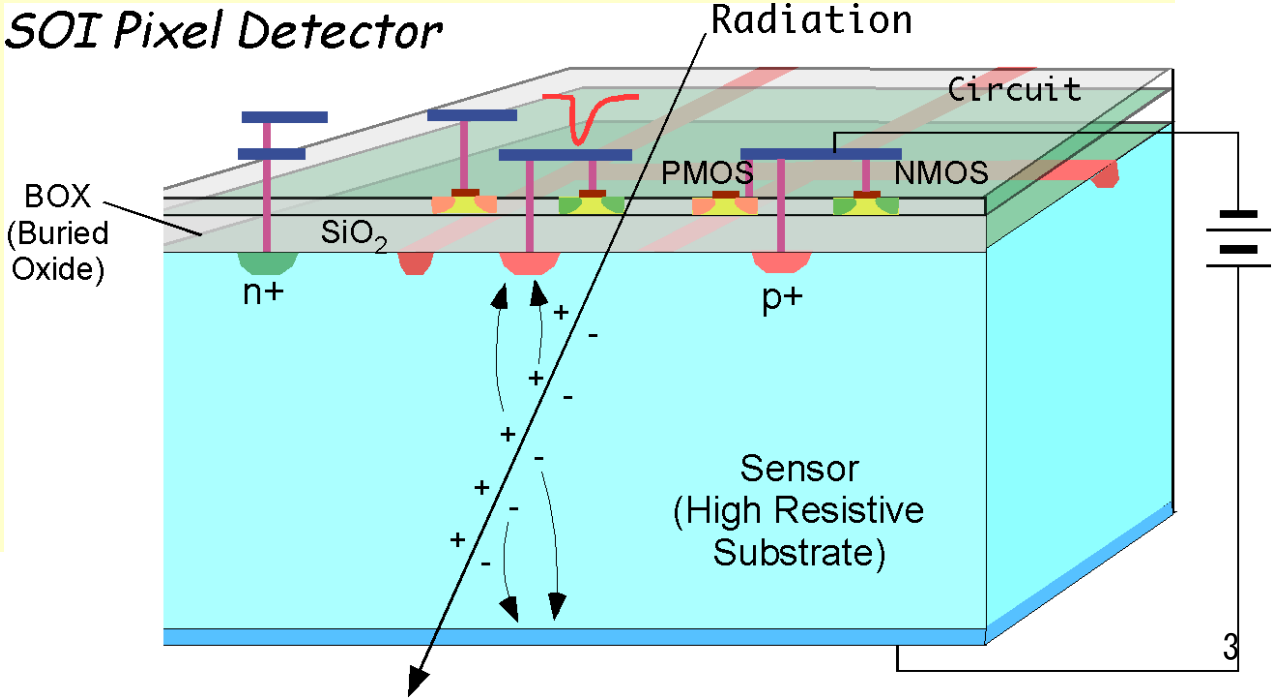
OUTLINE

- Introduction of SOI (Silicon-On-Insulator) Pixel Technology
- Status of SOI process/Detector Development
- Preliminary Pixel Test Results
- Summary



Features of SOI Pixel Detector

- Bonded wafer : High Resistivity (Sensor) + Low Resistivity (CMOS) .
- Truly Monolithic Detector (-> High Density, Low material, Thin Device).
- Standard CMOS can be used (-> Complex functions in a pixel).
- No mechanical bonding (-> High yield, Low cost).
- Fully depleted sensor with small capacitance of the sense node (~10fF, High conversion gain, Low noise)
- Based on Industrial standard technology (-> Cost benefit and Scalability)
- No Latch Up, Rad Hard.
- Low Power
- Low to High Temp (4K-300C) operation
- ...



KEK SOIPIX Target & Brief History

Starting as a generic R&D program.
Establish a SOI Pixel process and provide it to many users.
Develop detectors for XFEL, SuperBelle, ILC, sLHC, Space applications ...

'05. 7: Start Collaboration with OKI Elec. Co. Ltd. .

'05.10: TEG submission to OKI MPW run of 0.15 μm technology.

'06.12: 1st MPW run hosted by KEK with 17 designs including submissions from LBNL, FNAL, U of Hawaii.

'07.6: Process (and Fab.) is changed from 0.15 μm to 0.2 μm.

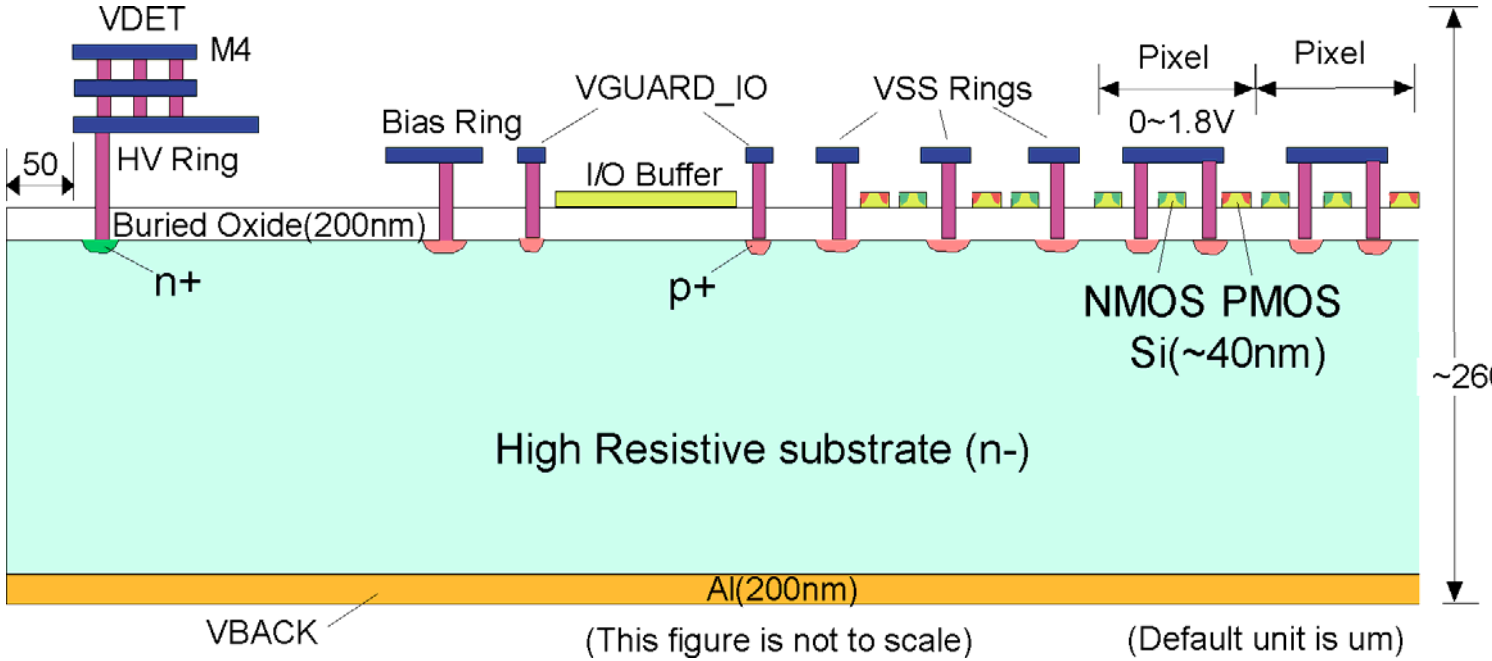
'08.1: 2nd KEK MPW run is submitted. *(Several troubles ...)*

'08.8: Chips having Implant errors are delivered.

'08.11: Final chips will be delivered.

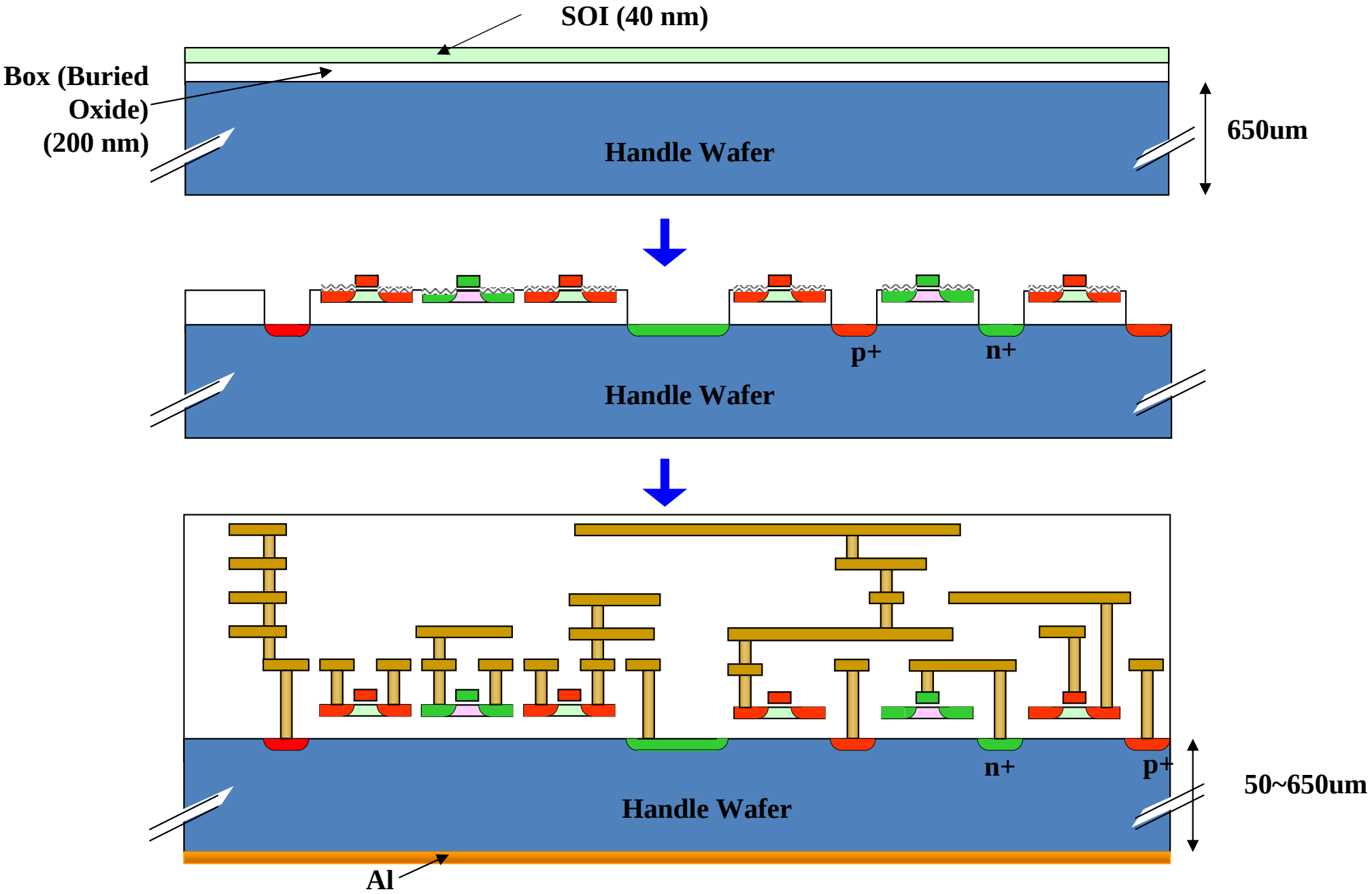
OKI 0.2 μm FD-SOI Pixel Process

Process	0.2μm Low-Leakage Fully-Depleted SOI CMOS (OKI) 1 Poly, 4 Metal layers, MIM Capacitor, DMOS option Core (I/O) Voltage = 1.8 (3.3) V
SOI wafer	Diameter: 200 mmϕ, Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz、700 Ω-cm (*n-type*), 650 μm thick
Backside	Thinned to 260 μm, and sputtered with Al (200 nm).



An example of a SOI Pixel cross section

SOI Pixel Process Flow



Process Change

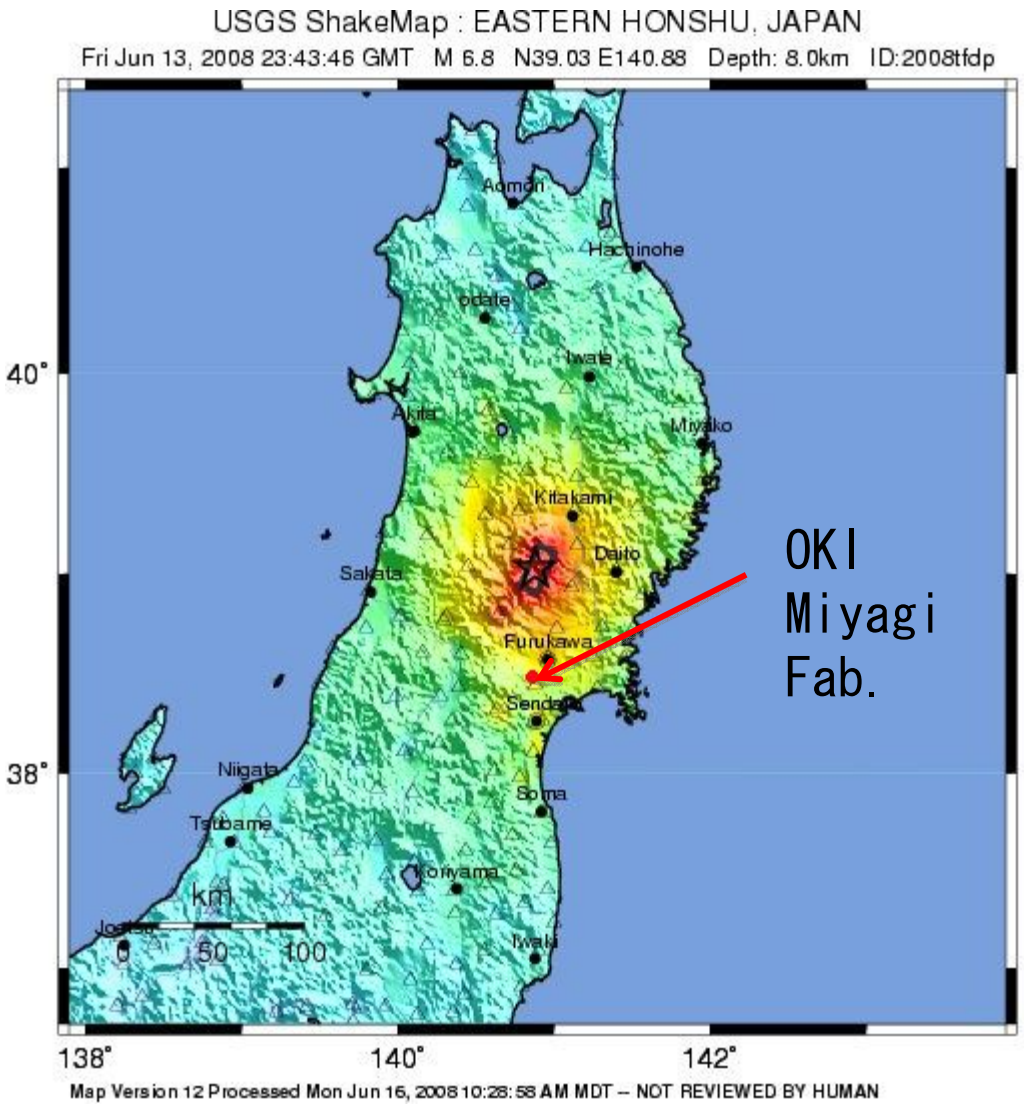
Since the 0.15 μm SOI process at OKI Hachioji Lab. was closed last spring, we moved to the 0.2 μm SOI process at OKI Miyagi Fab.

	0.15 μm →	0.2 μm
Wafer Diameter	6 inches	8 inches
Core (I/O) Voltage	1.0V (1.8V)	**1.8V (3.3V)**
Gate Length	0.14 μm	0.2 μm
Gate Oxide Thickness	2.5/5 nm	4.5/7 nm
BOX Thickness	200 nm	200 nm
Off State Current	<100 pA/μm	**<0.1 pA/μm**

Process quality is expected better for 0.2 μm, but we suffered from many trouble in this run...

Miyagi-Iwate Earth Quakes

June 14(M7.2) & July 24(M6.8)



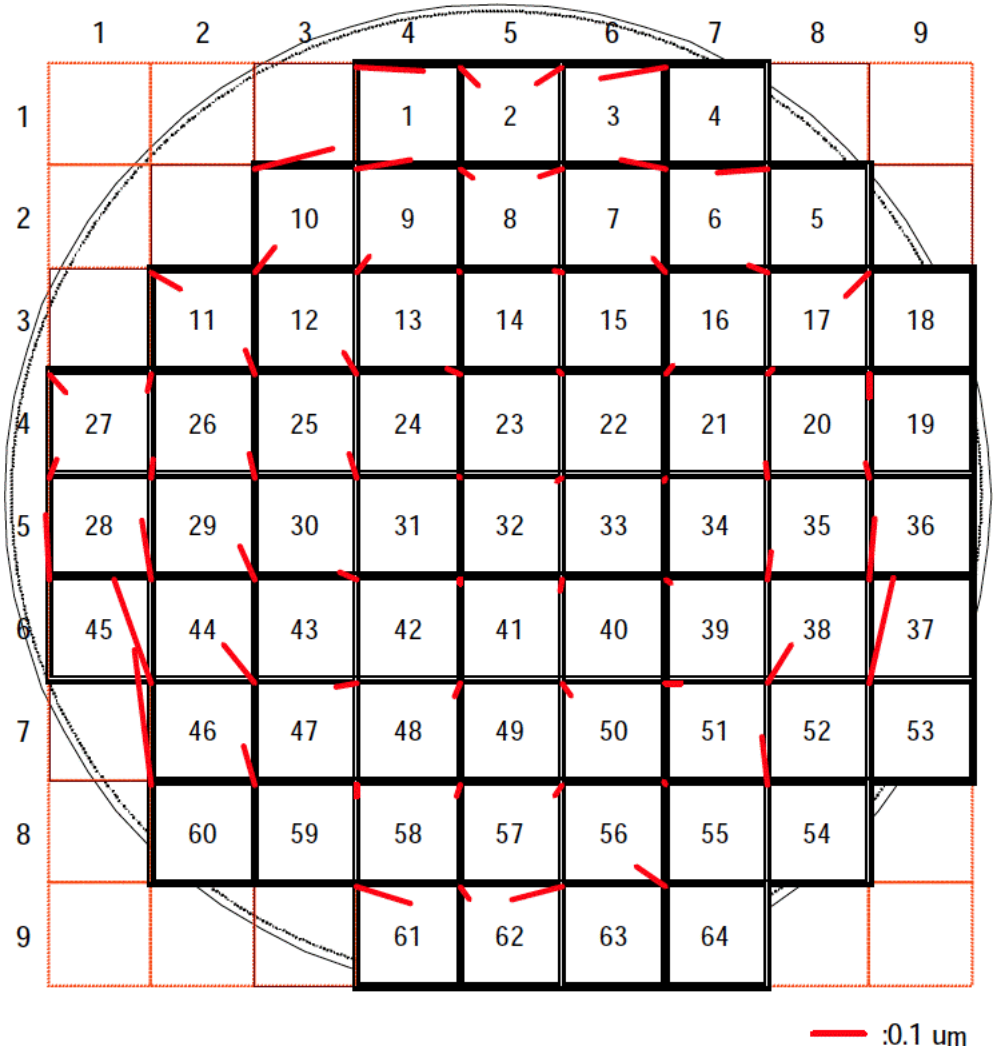
OKI Miyagi Fab.

No serious damage to fab but the line was stopped for a few weeks.

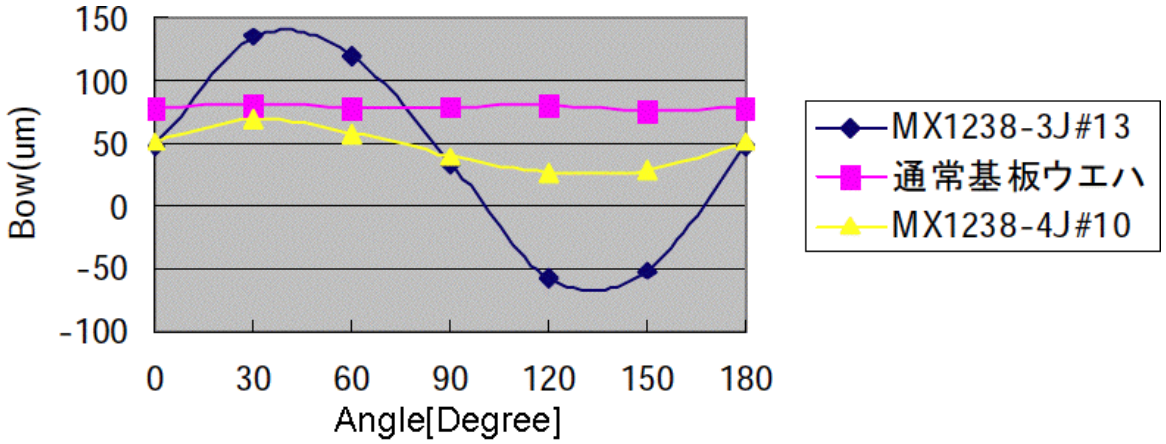
Many wafers processed in machines were damaged.
Fortunately our wafers were 30 min before the back thinning step!

Wafer Bend

- After thermal process, we observed wafer bend in some wafer.
- This cause alignment error during process.
- This looks like related to wafer lot and temperature control.
- High Resistivity (Low Oxygen) wafer is weak in general.
- Changing the thermal process and investigating the wafer lot.



Alignment mismatch after thermal process



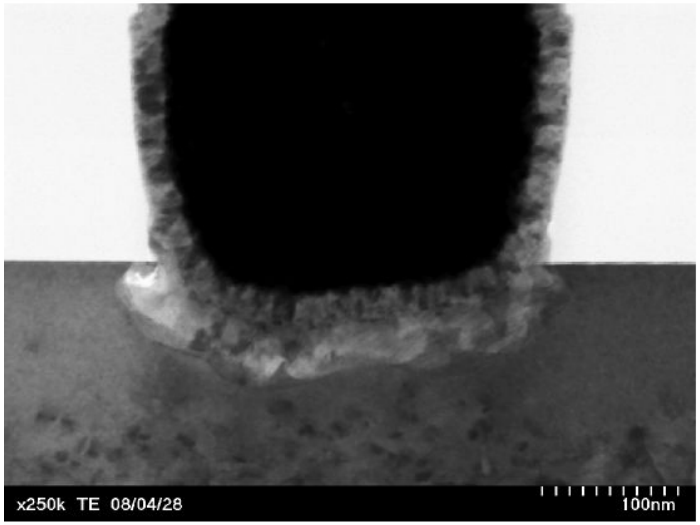
Contact Creation Error

At first, we didn't notice the wafer bend, and this leaded to redo of contact process 3 times.

Finally this caused thin oxide layer under the contact.

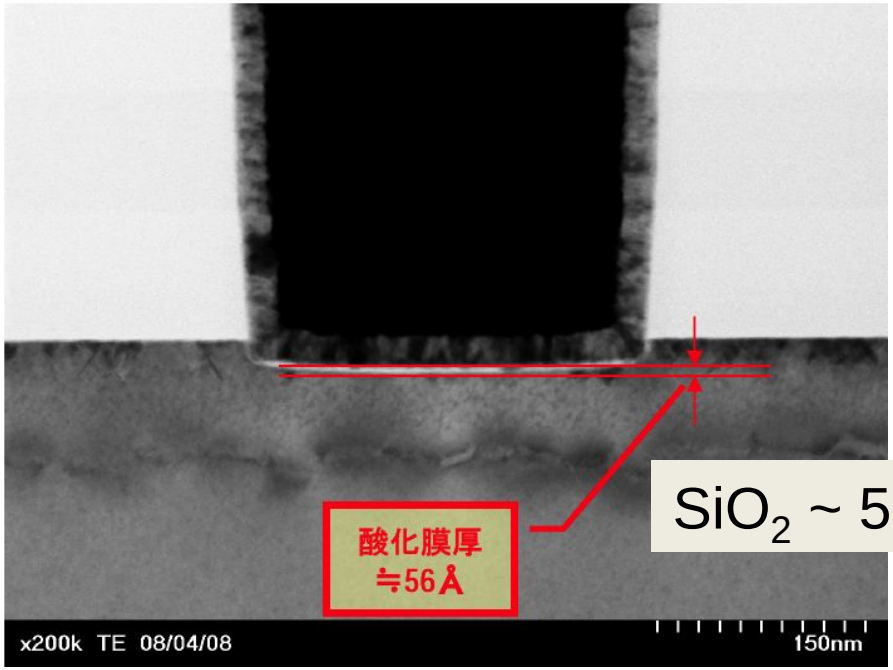
Process step was changed to avoid this even the redo is done.

PSUB上2CS(002J)



Good

PSUB上2CS(001J)

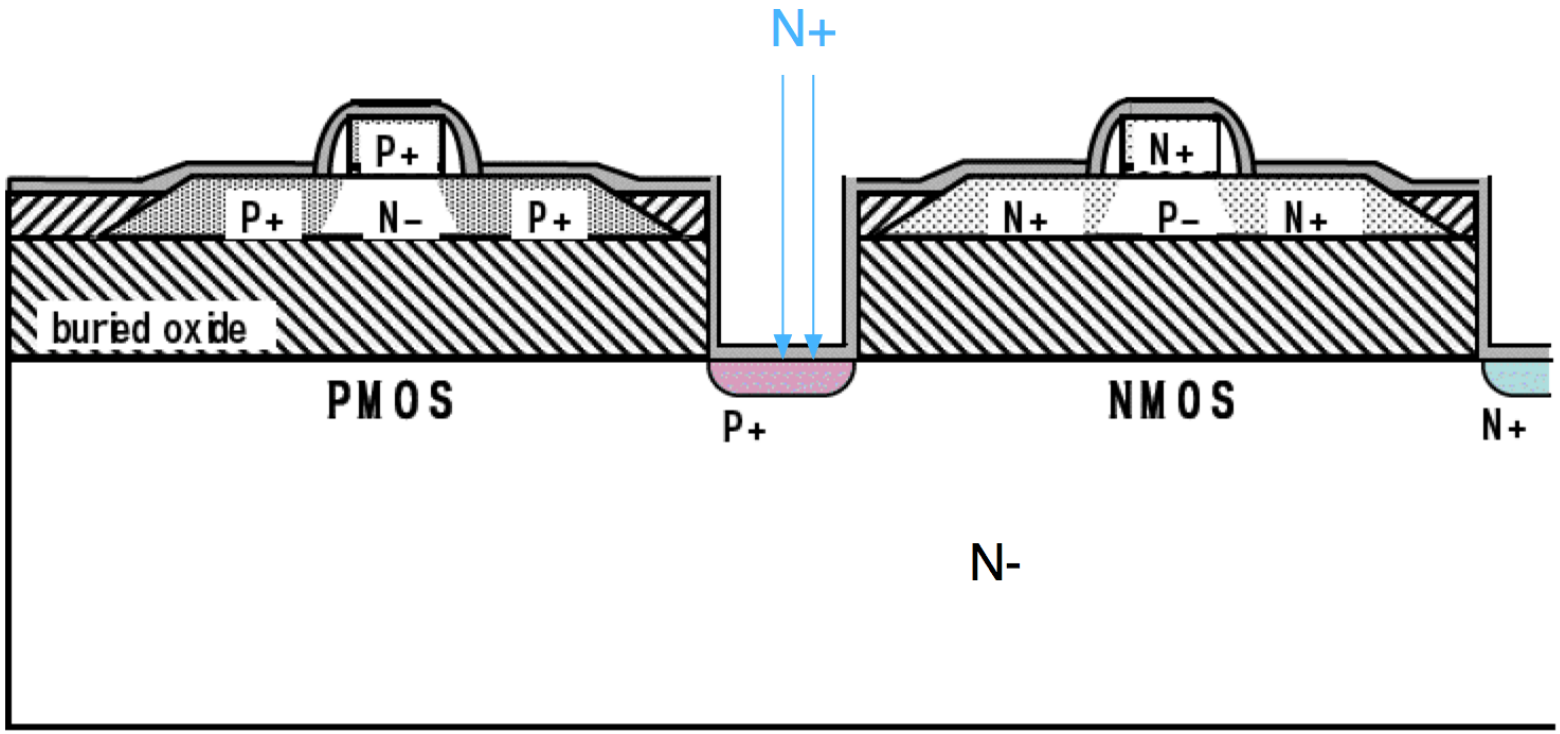


SiO_2 ~ 56A

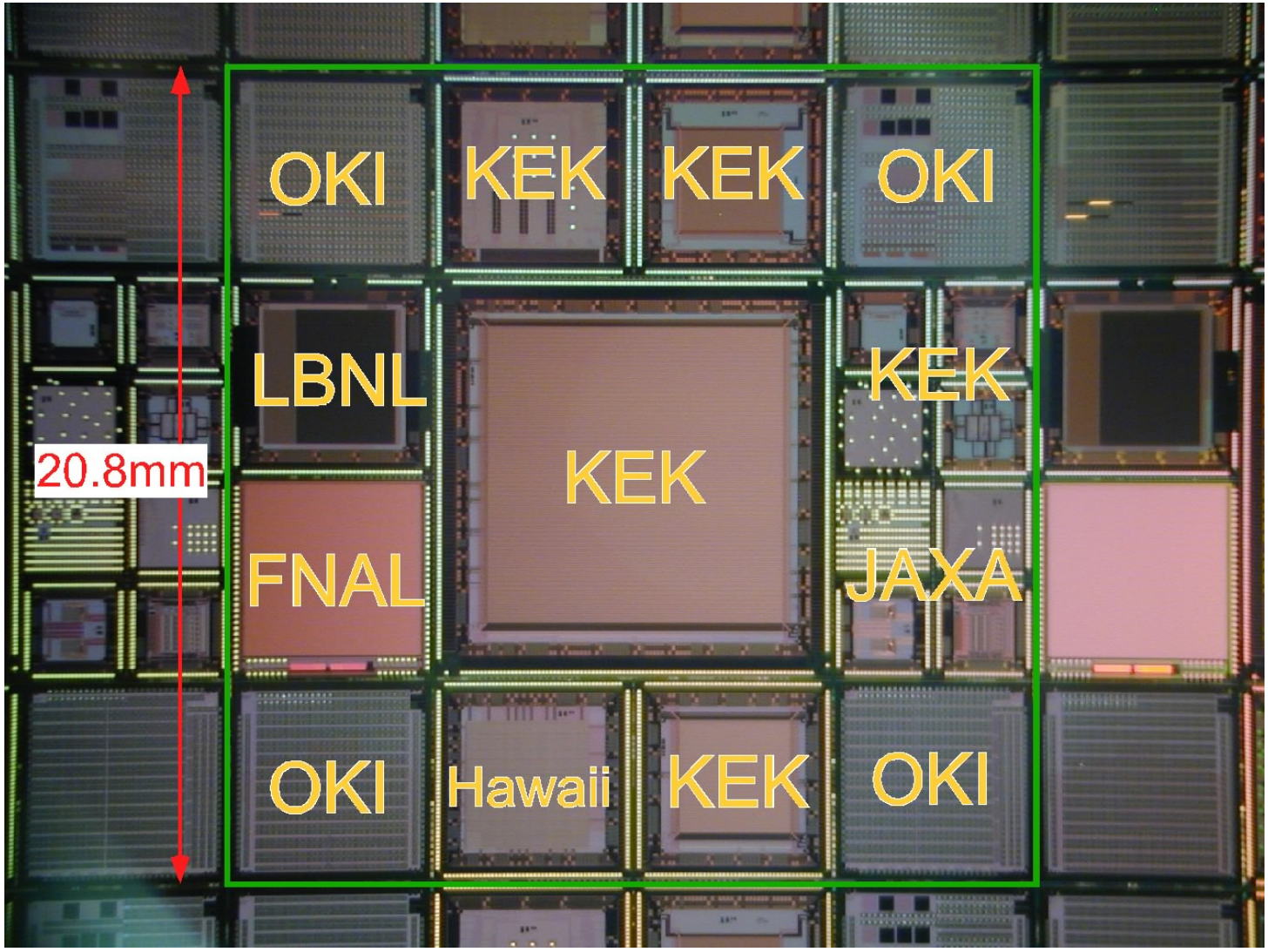
Not Good

Implant Error

Due to a DRC rule error, N+ was erroneously implanted onto some P+ region of handle wafer.
This causes large leakage current in the sensor.
Recovery lot is under processing. It will end at October.

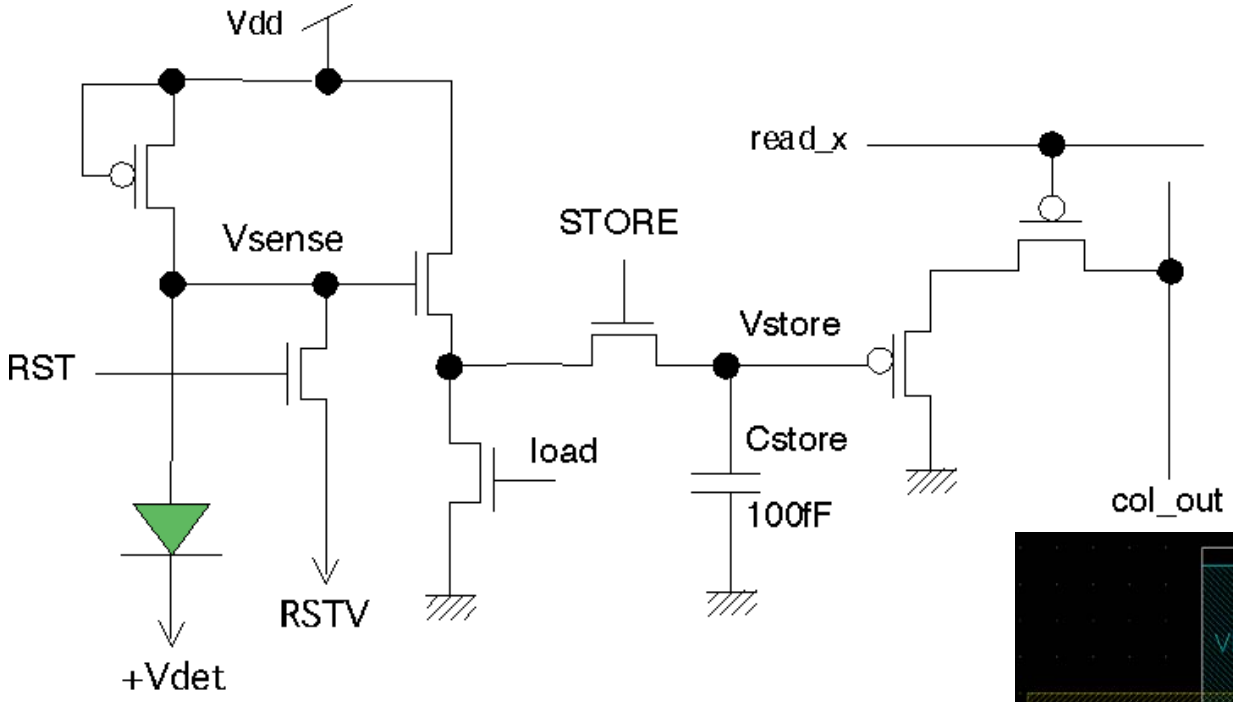


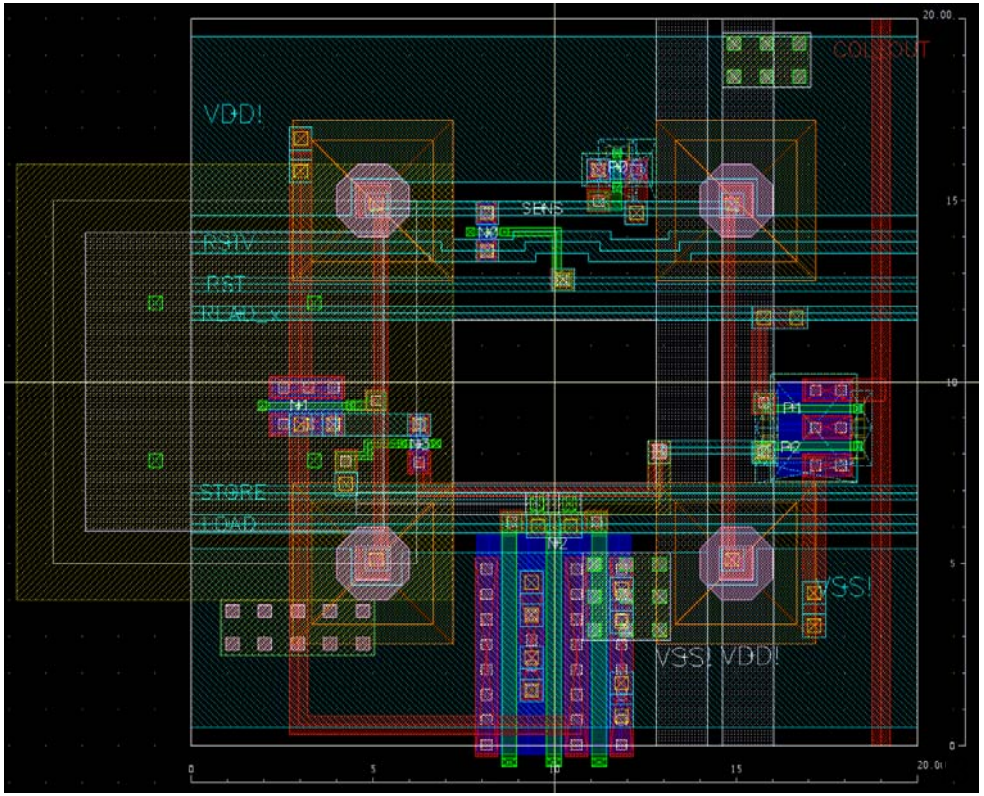
2nd KEK SOI MPW run Preliminary Test Results



Due to the Implant Error, applied voltage of the sensor is limited.

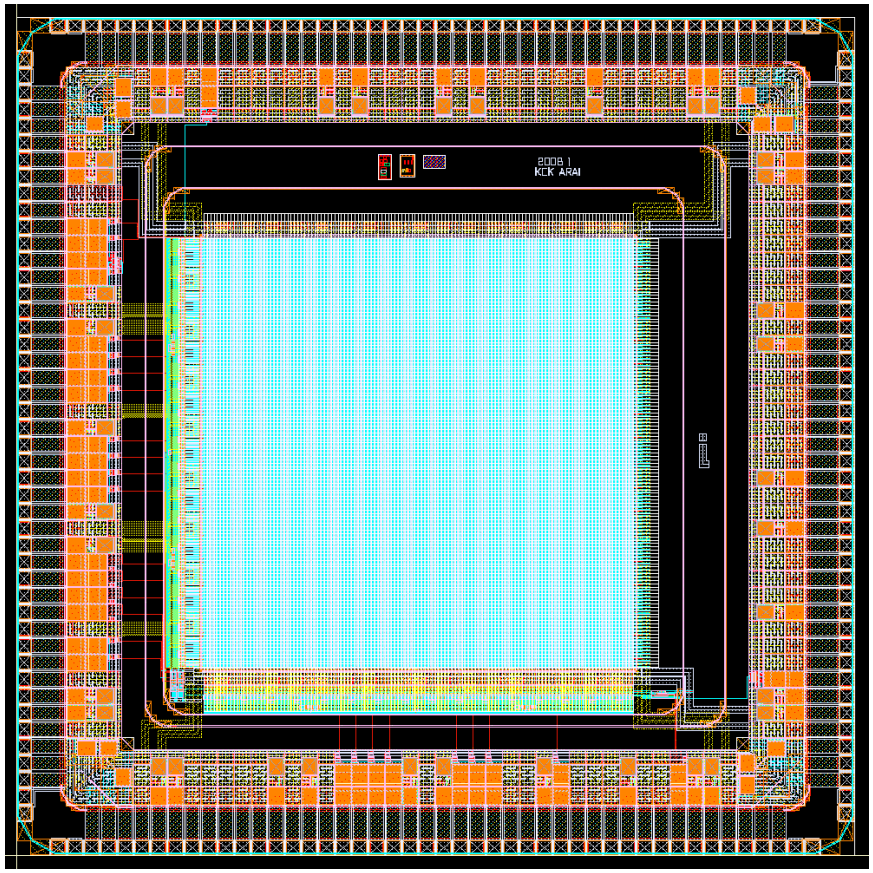
Integration Type Pixel (INTPIX)

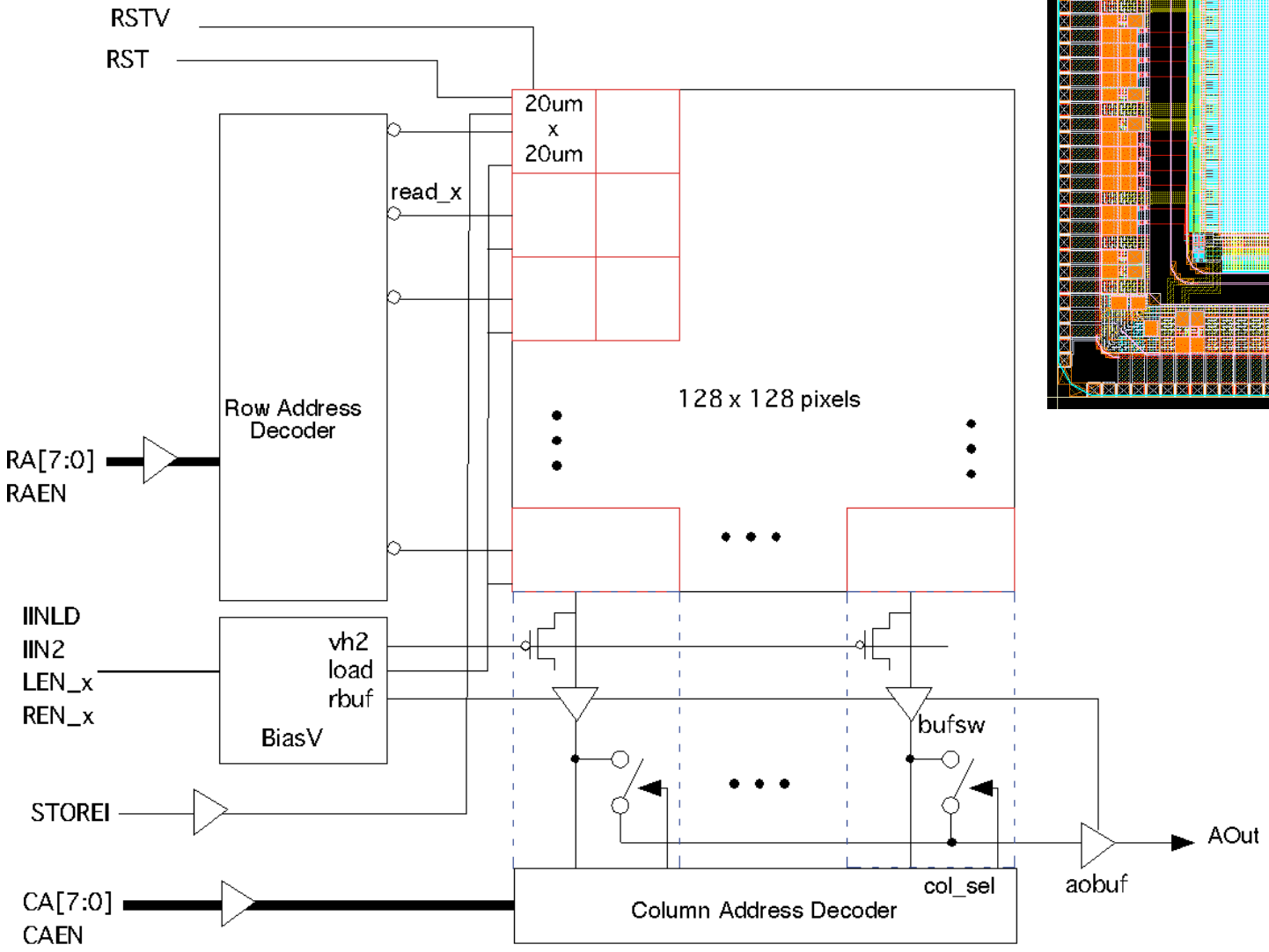




20 μm x 20 μm pixel

INTPIX2





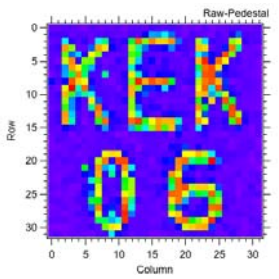
128 x 128 pixels
5 x 5 mm^2

Laser Images

INTPIX2

2006

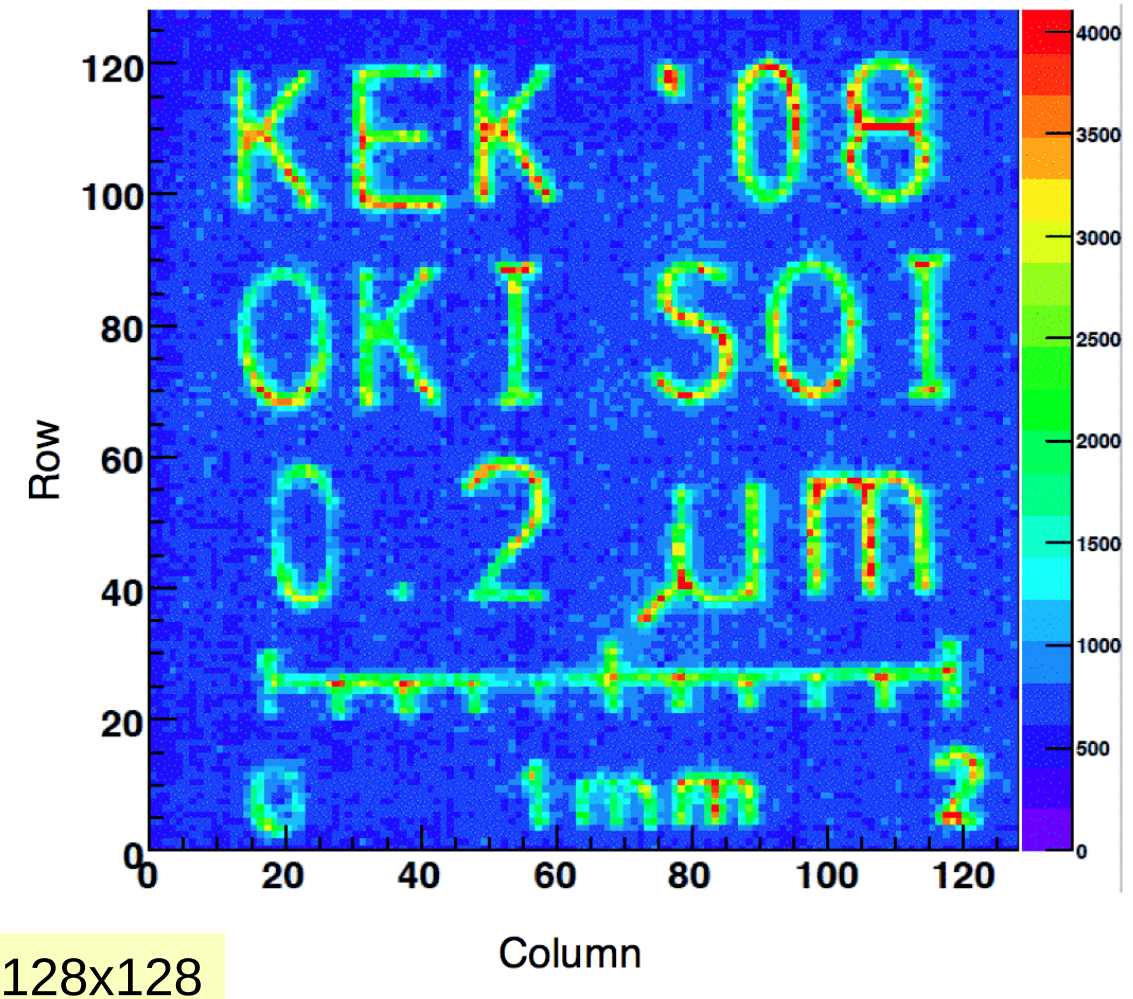
0.64 mm



32x32

2008

2.56 mm

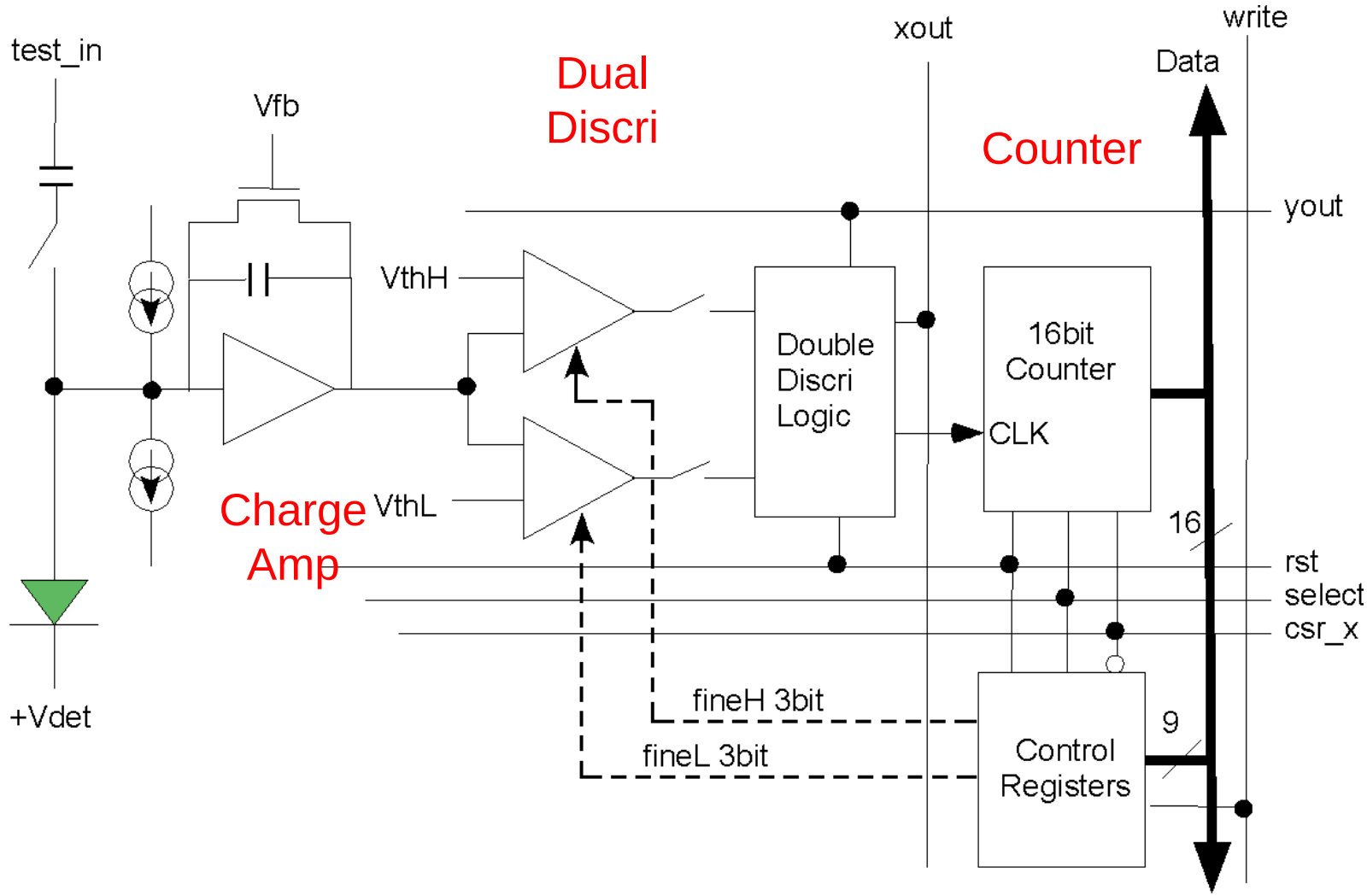


128x128

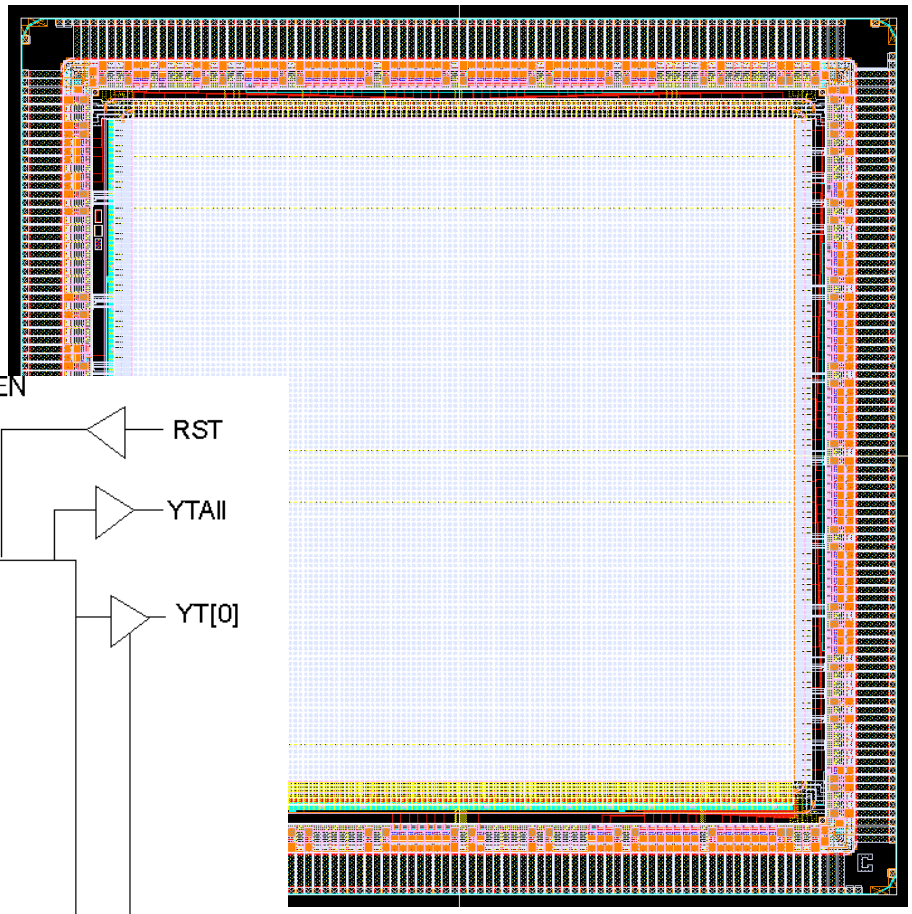
Counting Type Pixel

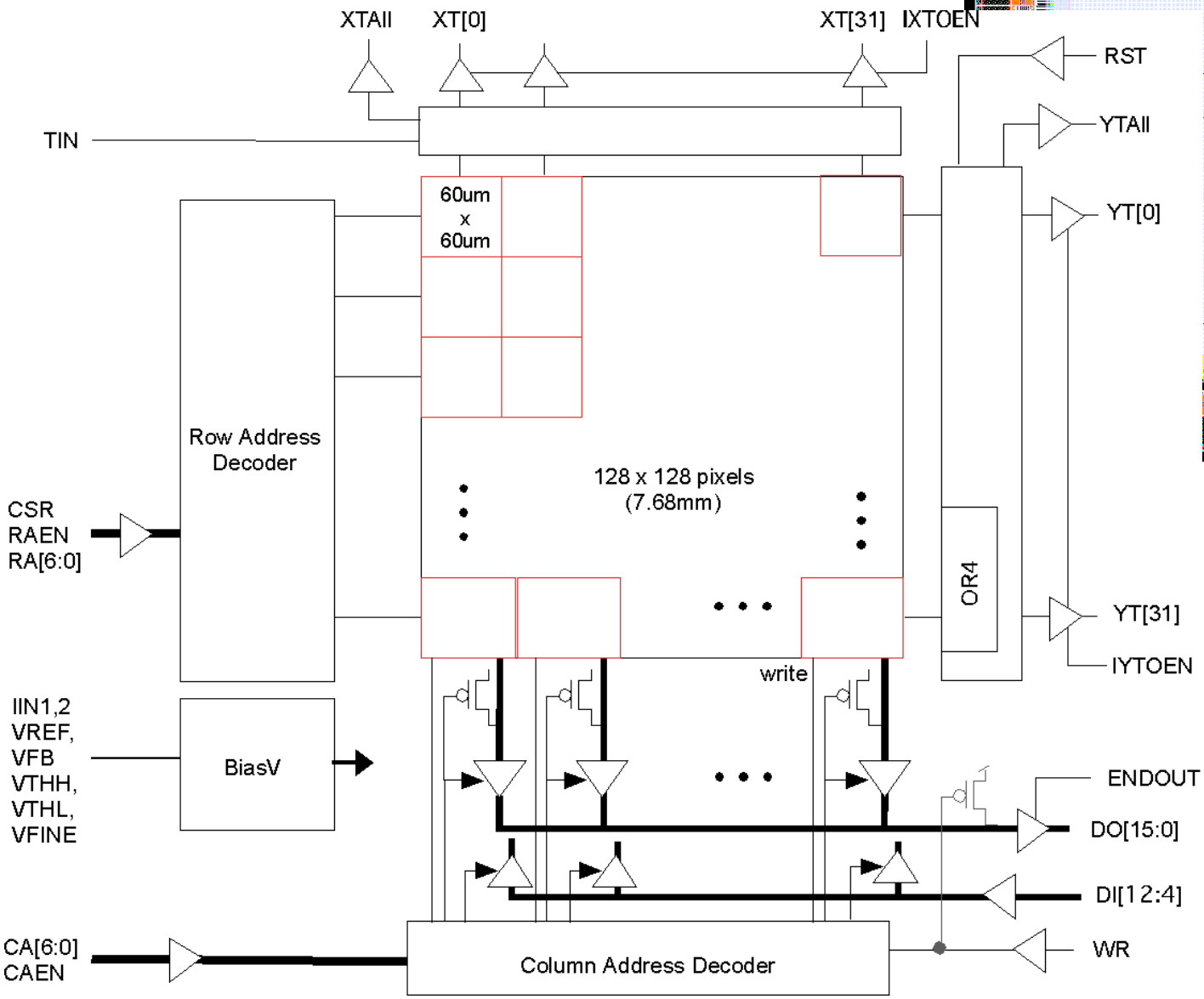
Energy window and counting in each pixel.

10.4 mm□、128 x 128 pix

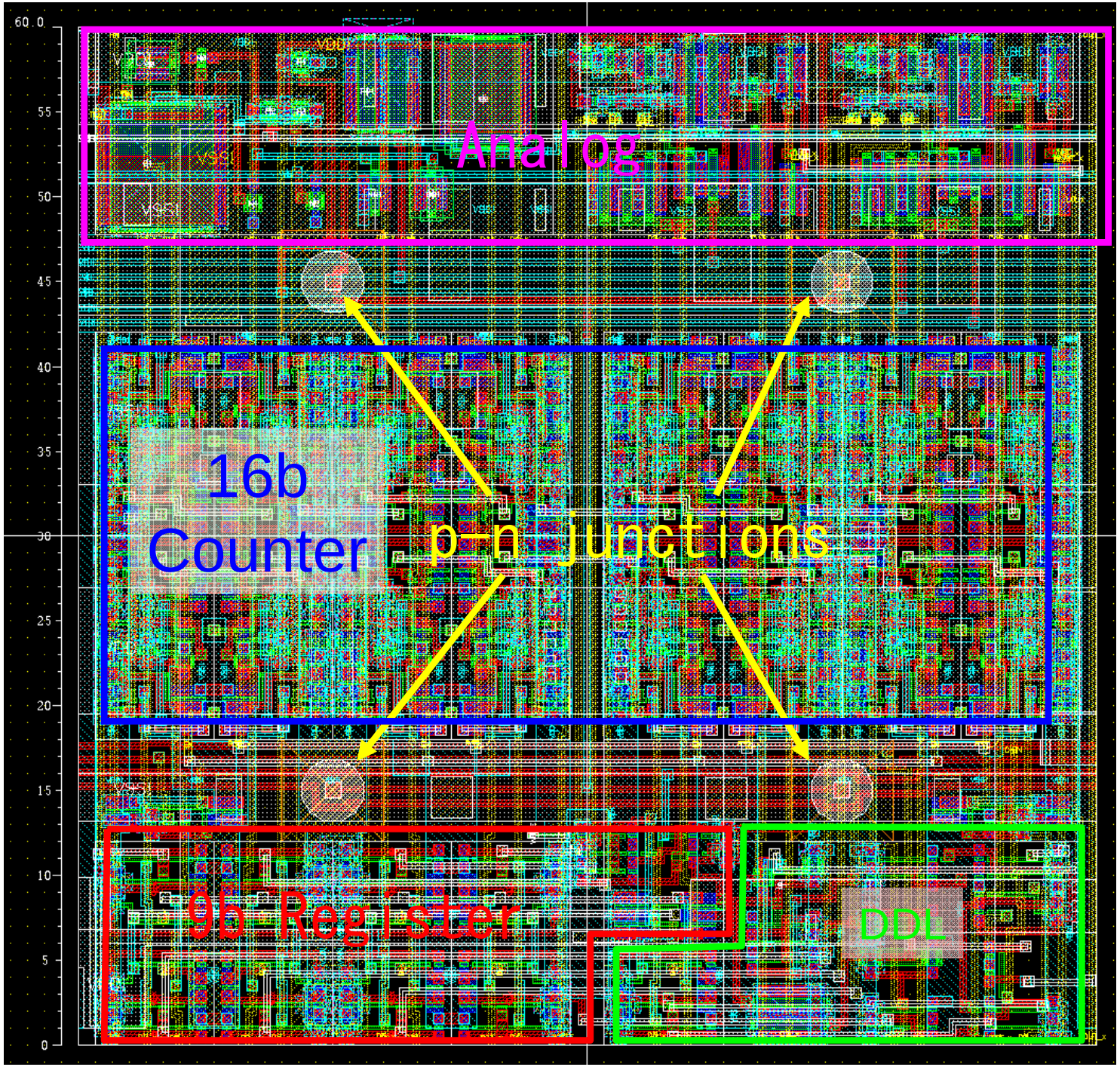


CNTPIX2





10.2x10.2 mm^2



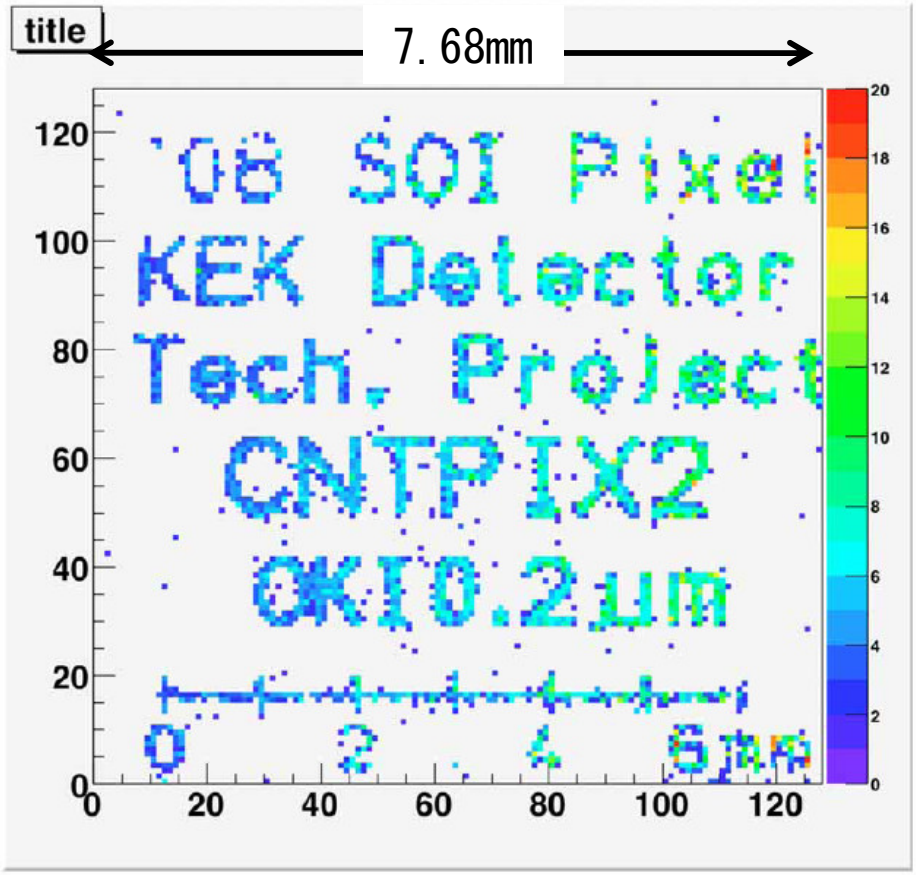
CNTPIX2

~600 Transistors
x 128 x 128
= 10,000,000 Trs

60x60 um^2

Laser Image

CNTPIX2



We found a bug in the 16 bit counter, so right side pixel have larger count.

Vdet=1.5V

Preliminary

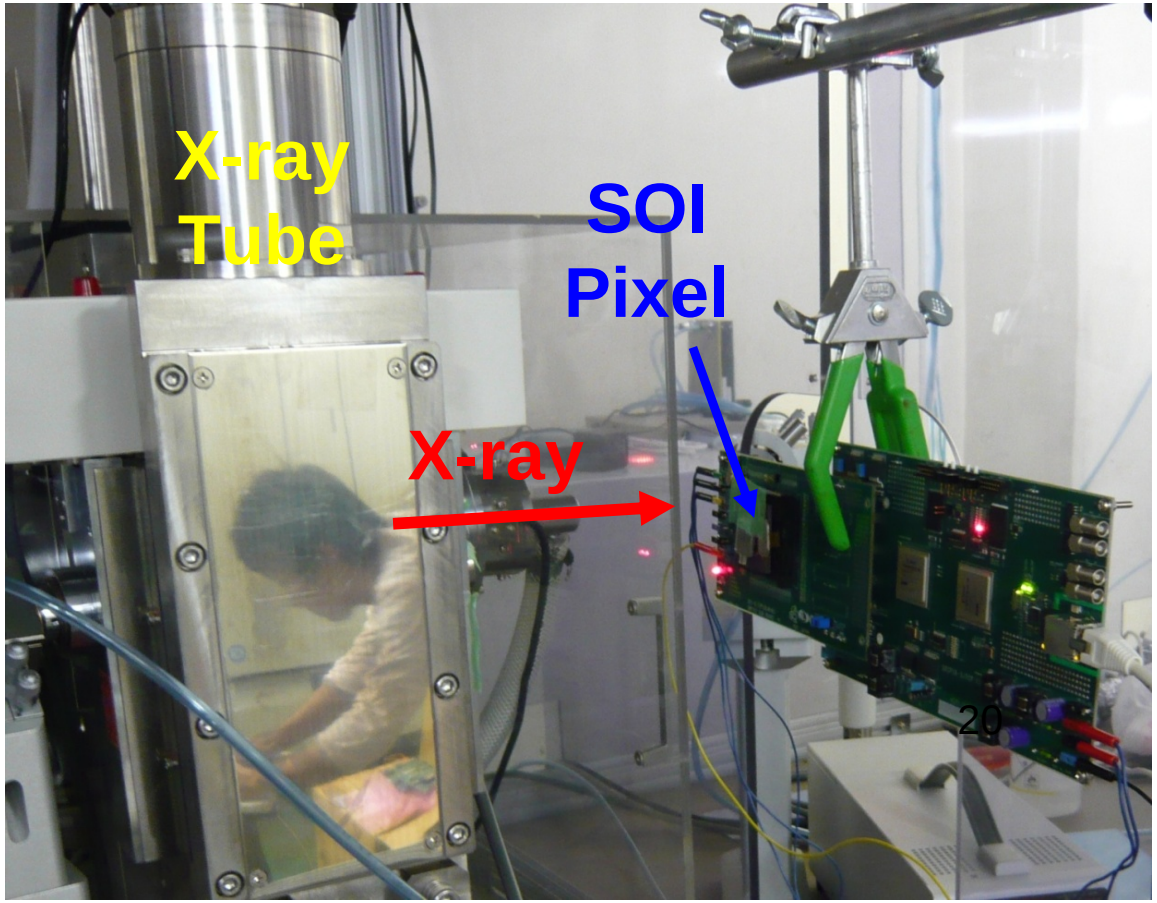
X-ray Irradiation Test

X-ray Generator : Rigaku FR-D

Target : Cu (Cu Kα ~8keV)

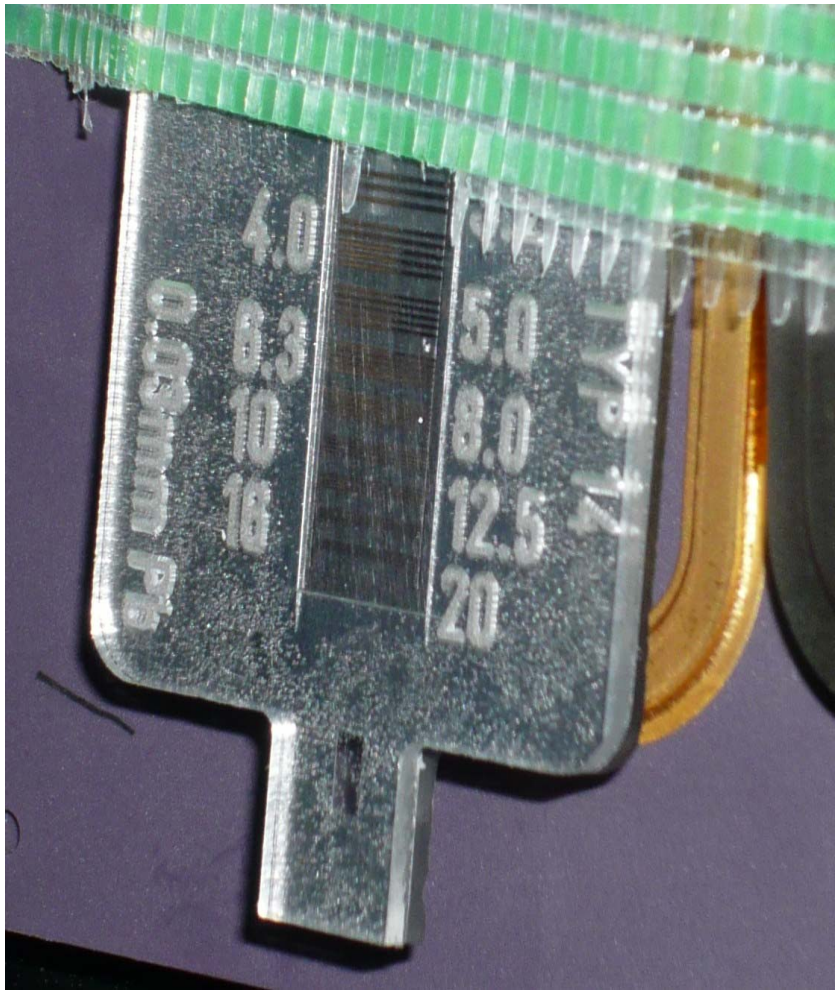
Power : 30-35kV, 10-30mA (max 50kV,60mA)

Intensity : ~10^4 photons/pixel/sec @30kV,10mA

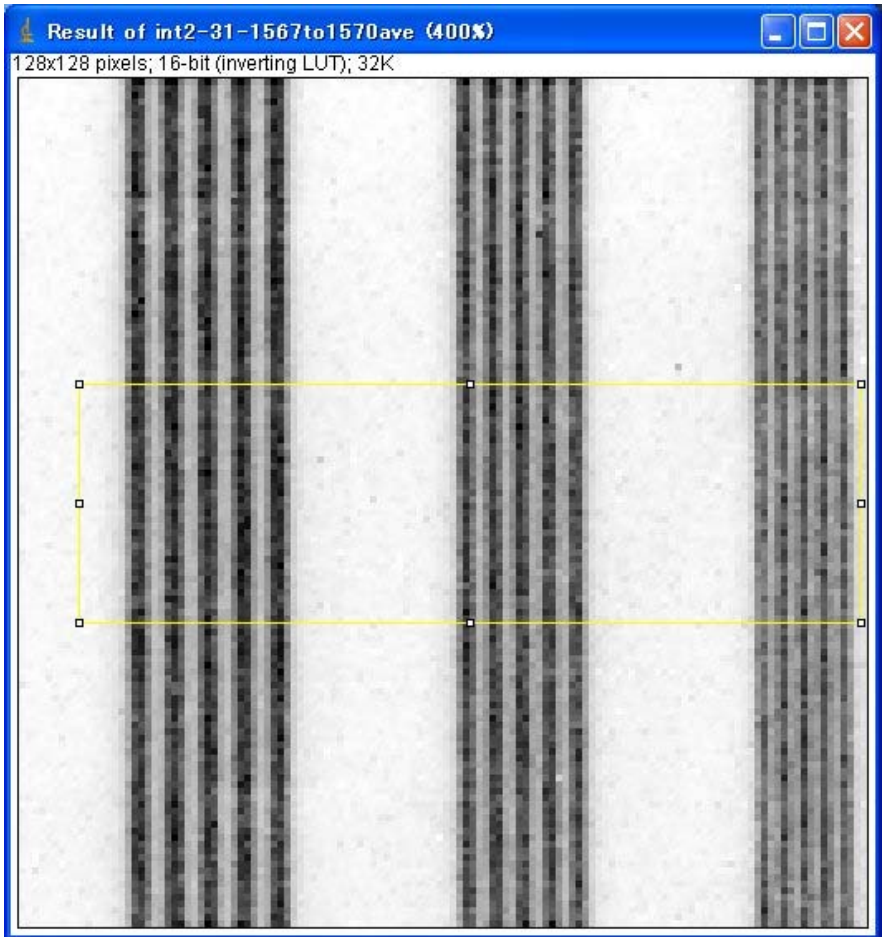


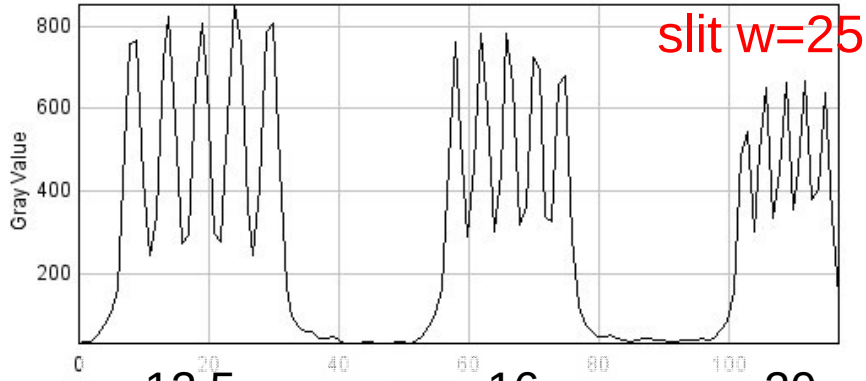
Position resolution
(pixel size=20μm x 20μm)

INTPIX2



X-ray Test Chart





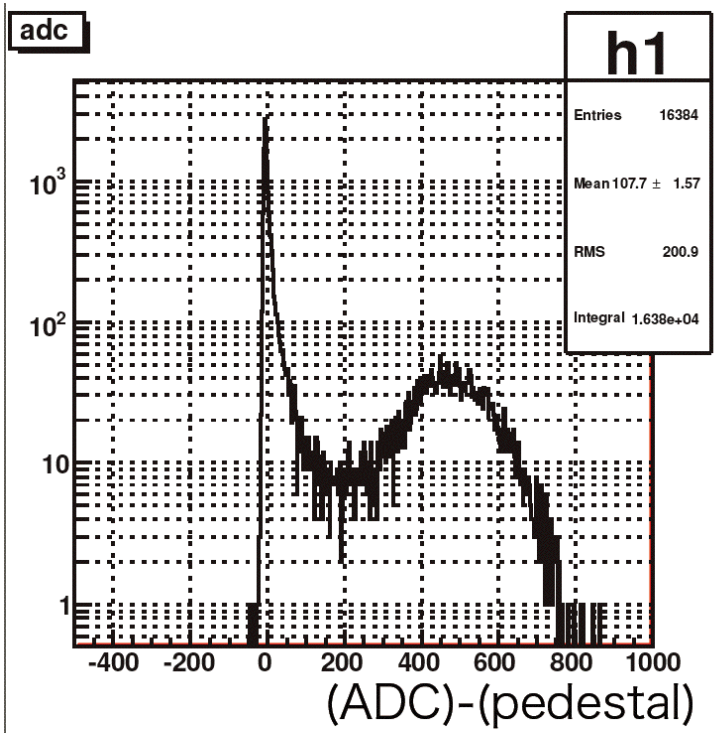
slit w=25μm

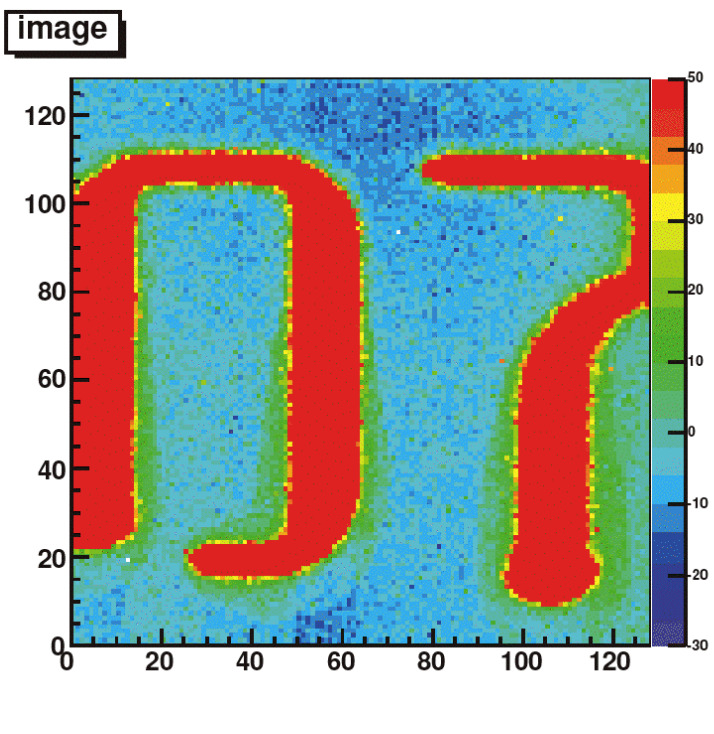
12.5 16 20

[lp/mm]

25 μm Slit is well separated.

INTPIX2



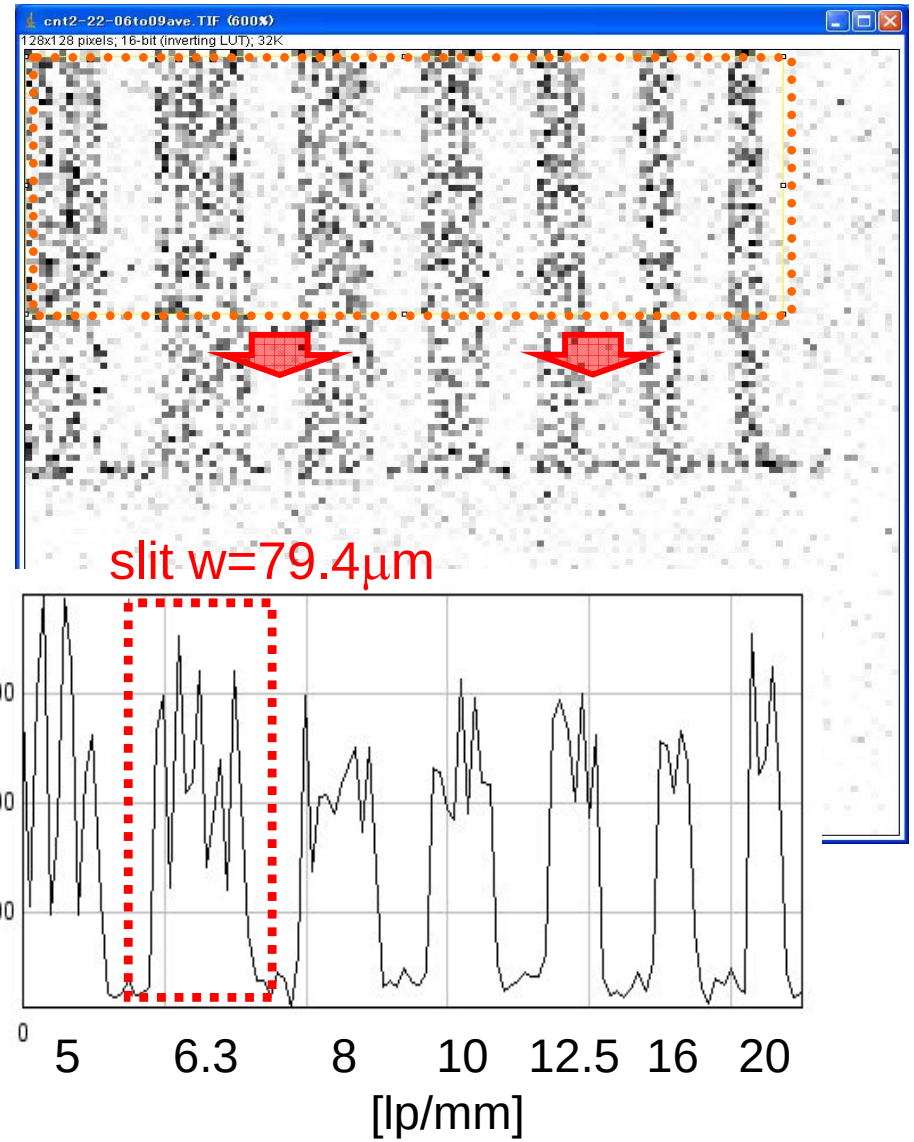


Vdet=1.5V
800 μs Integration Time

Preliminary

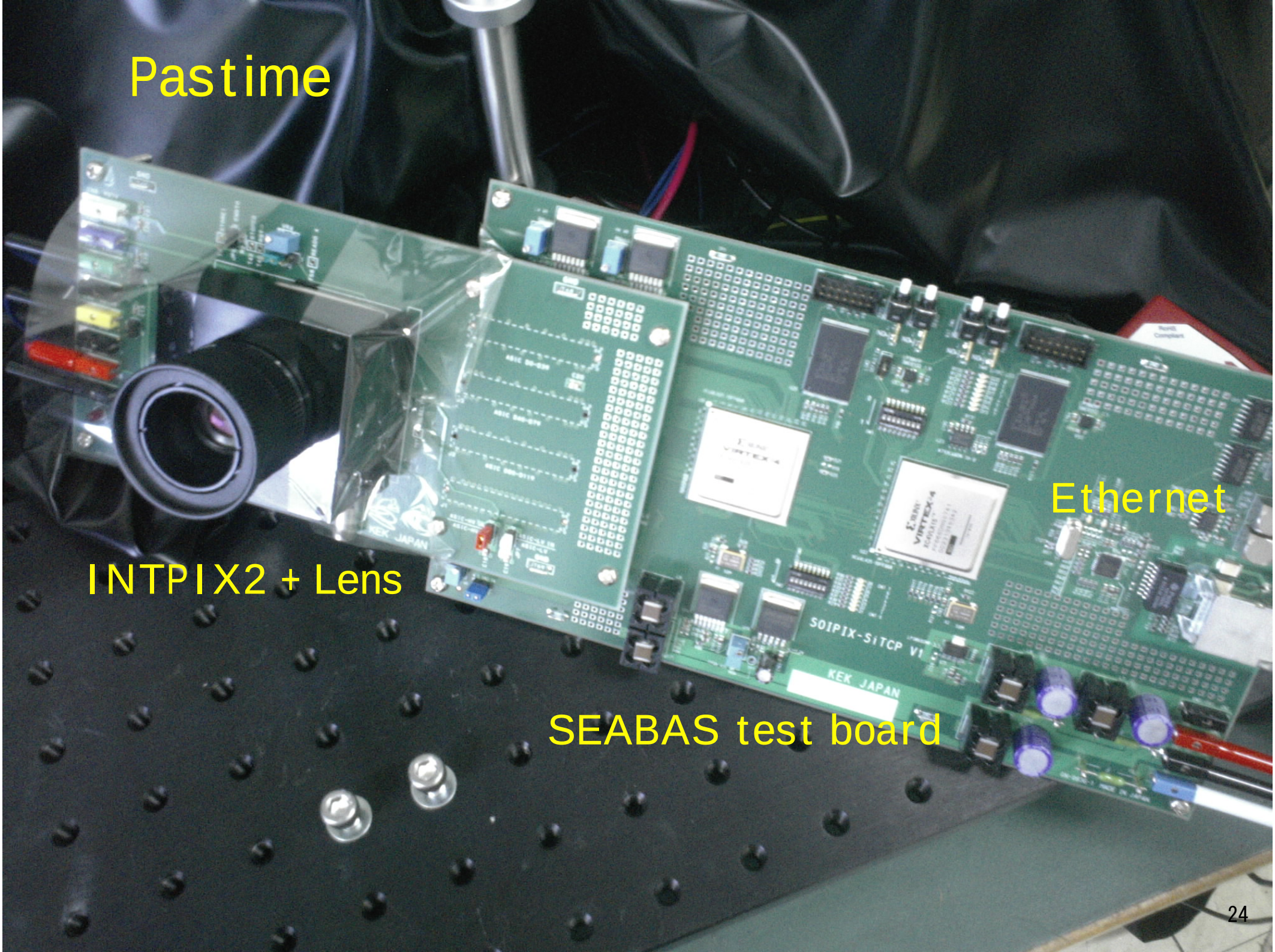
Position resolution
(pixel size=60μm x 60μm)

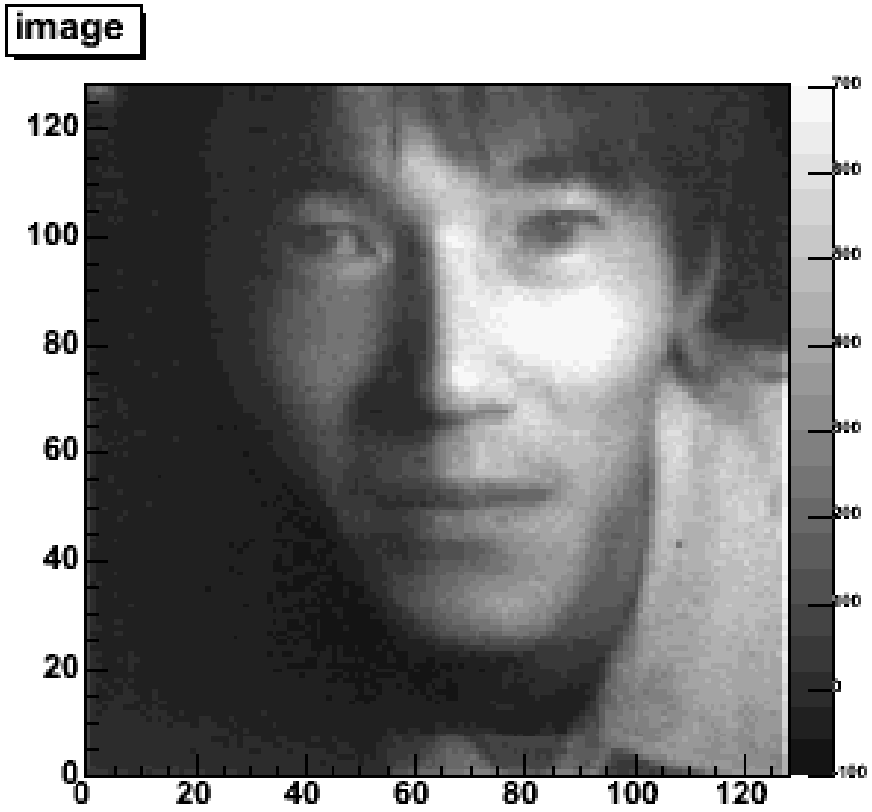
CNTPIX2



Vdet=1.5V
1.6 ms Integration Time

Preliminary!


Pastime
INTPIX2 + Lens
Ethernet
SEABAS test board
SOIPIX-SiTCP V1
KEK JAPAN



Max Readout Speed ~300 frames/sec (200 ns/pixel)

Summary

- The SOI pixel has many unique features (monolithic, low material, high speed ...) and a promising candidate for future pixel detectors.
- We moved from 0.15 μm to 0.2 μm Low Leak process from the present run.
- Although the first 0.2 μm process has suffered from many troubles, we belive 'good coming out of evil'.
- Preliminary test chips are showing good response to light, β-rays, and X-rays.
- We have been organizing MPW runs of the SOI process, and welcome new users for the SOI process.
  (Next submission is schedule on January 2009)