# 3D-LSI Technology for Image Sensor

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**ZyCube**

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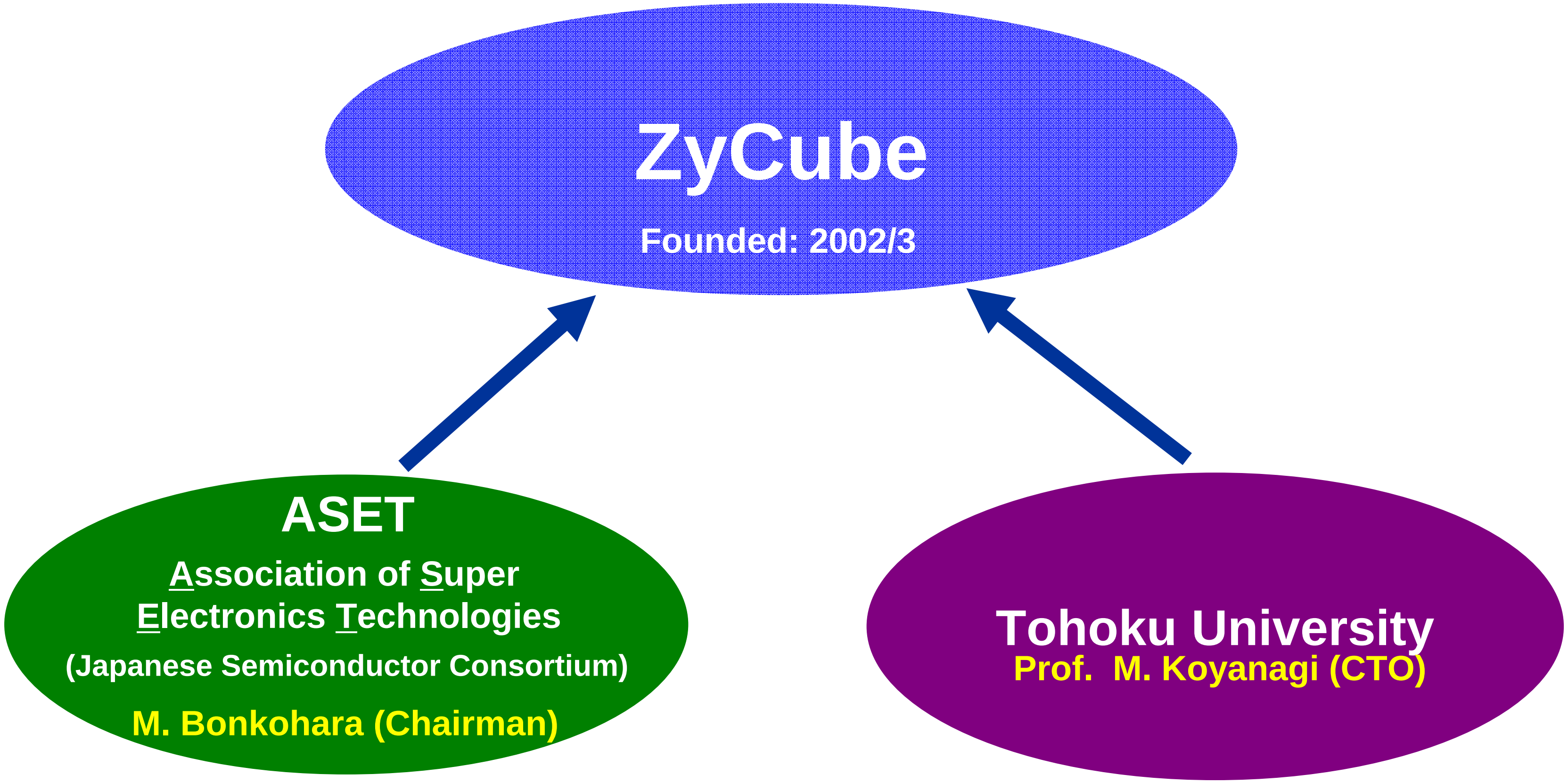
**Tohoku Univ./ZyCube**

# ZyCube History



# Outline

## 1. Introduction

- Advantages of 3D-LSI
- Potential Application

## 2. Technology Approach

- Technology breakdown
- TSV scaling, process
- Bond/Stack approaches

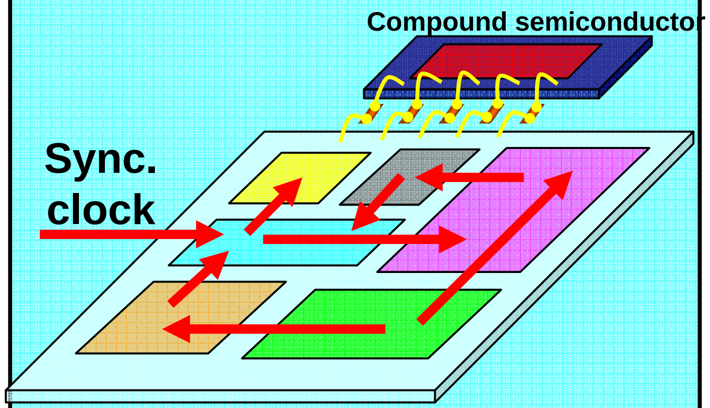
## 3. TSV and μ-bump

- Current technology
  - 3D-LSI for Image Sensor
- Next generation technology

## 4. Summary

# Advantages of 3D-LSI

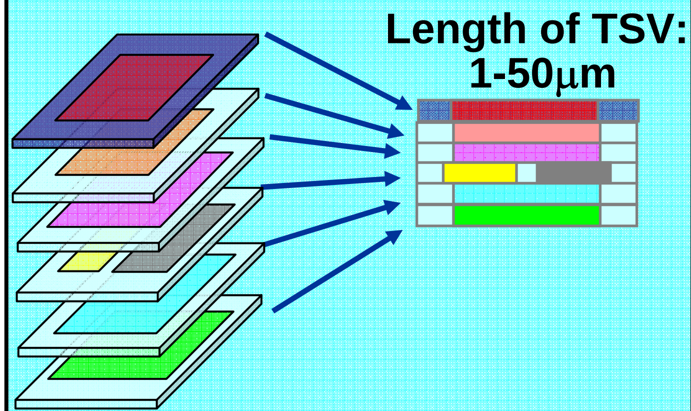
## Conventional SoC




**Long Global interconnect**
**large RC delay, large $C_P$**

*segment 2D-SoC into functional block*

## 3D-SoC




**Short global interconnect**
**small RC delay, small $C_P$**
**High band width**
**Small form factor**

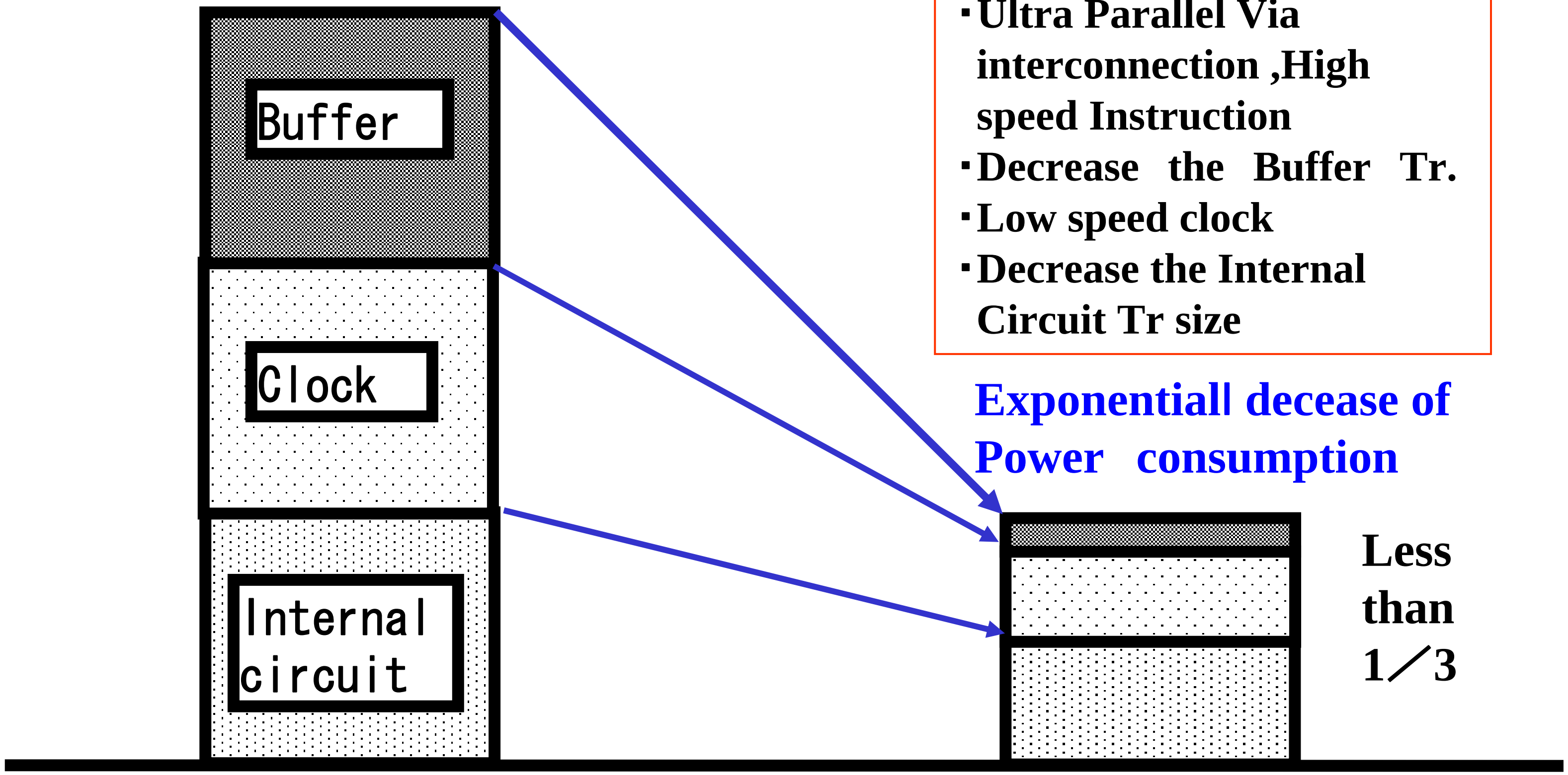
1. Increase of electrical performances
2. Increase of circuit density
3. New Architecture (Hyper-parallel processing, Multifunction, etc)
4. Heterogeneous integration
5. Cost reduction
6. Realize high performance detector with ~100% area factor in chip

# 3D Effect for Power Consumption

## Estimation for MCU

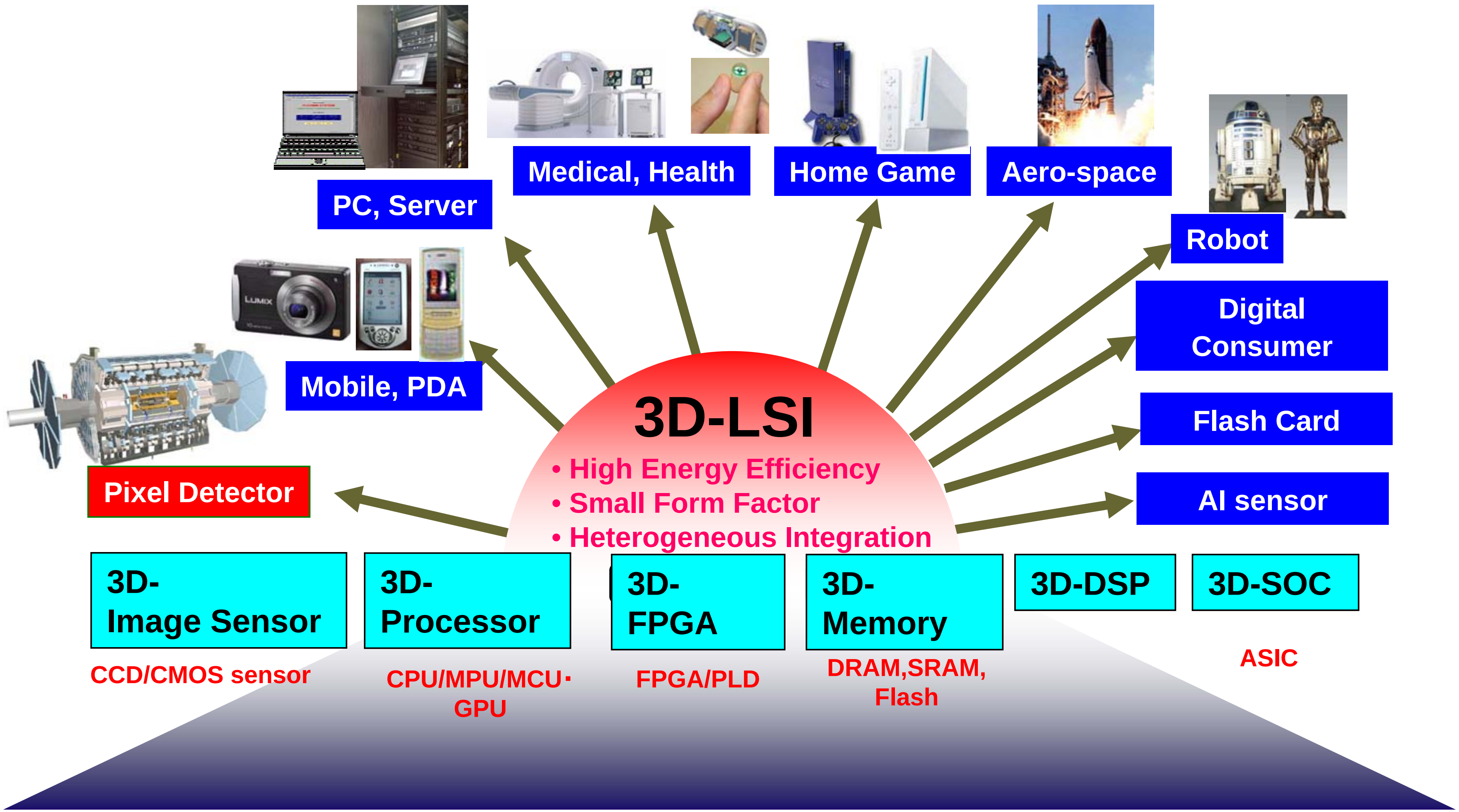
- Ultra Parallel Via interconnection ,High speed Instruction
- Decrease the Buffer Tr.
- Low speed clock
- Decrease the Internal Circuit Tr size

**Exponentiall decease of Power consumption**




**Present 2D LSI PKG** **3D-SoC**

# Potential application of 3D-LSI



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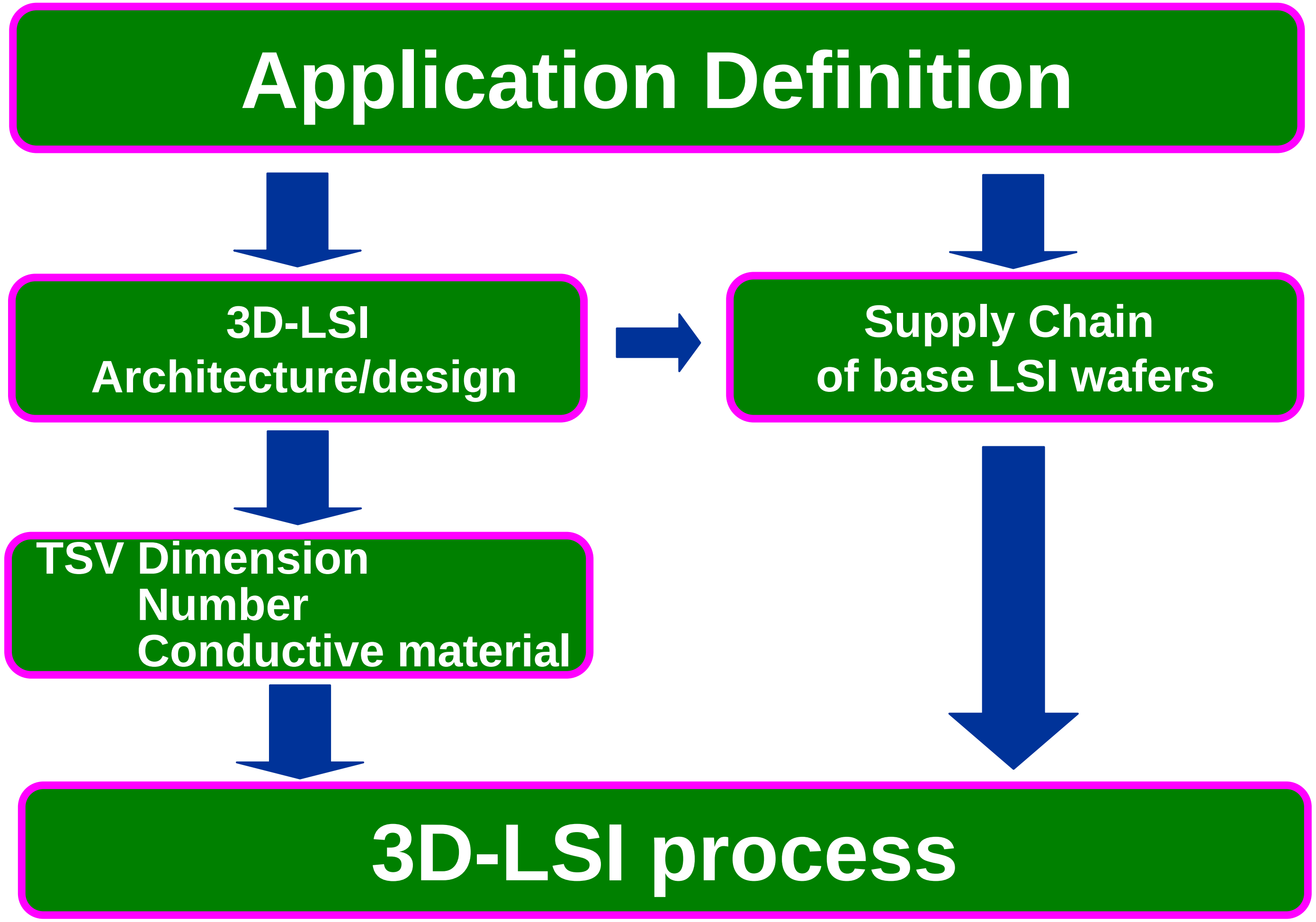
# Determination of the 3D-LSI process



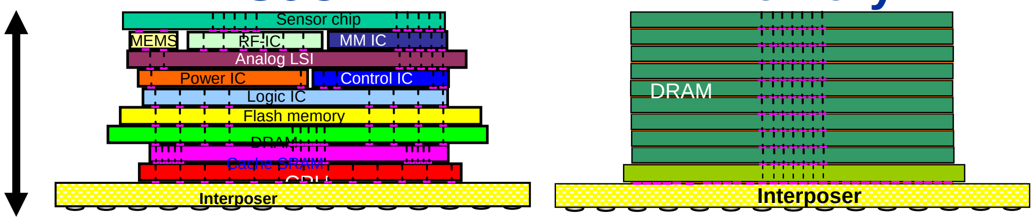
# Technology Break Down

**(1)Base Wafer Process**
- **Substrate:** bulk-Si, SOI,
  Compound Semiconductor, MEMS
- **Thinning:** Grinding, Polish, CMP,
  plasma etch, wet etch
- **Handling:** Thin wafer Support system

**(2)TSV formation**
- **Via opening:** **Laser drilling or DRIE**
- **Conductor:** **Cu, W, PolySi, conductive paste**
- **Filling method:** plating, CVD, sputter, vapor deposition
- **Isolation:** conformal CVD, sputter,
  vapor deposition

**Thickness Budget**
**< 1 mm**

**SoC** **Memory**




**(3) New material**
- Adhesive
  (permanent/temporally)
- Bump metal, barrier metal
- Conductive paste
- etc

**(5)Interposer**
- **Substrate** --silicon or organic?
- **Embedded chips & passives?**

**(4)Stacking approach:**
- **Technology:** Metal Thermo compression,
  Direct Oxide (SiO2), Adhesive bonding…
- **Integration scheme:**
  CoC, CoW or WoW?
  Face to face or face to back?
- **Accuracy?**
- **Throughput ?**
- **How many dies to stack?**

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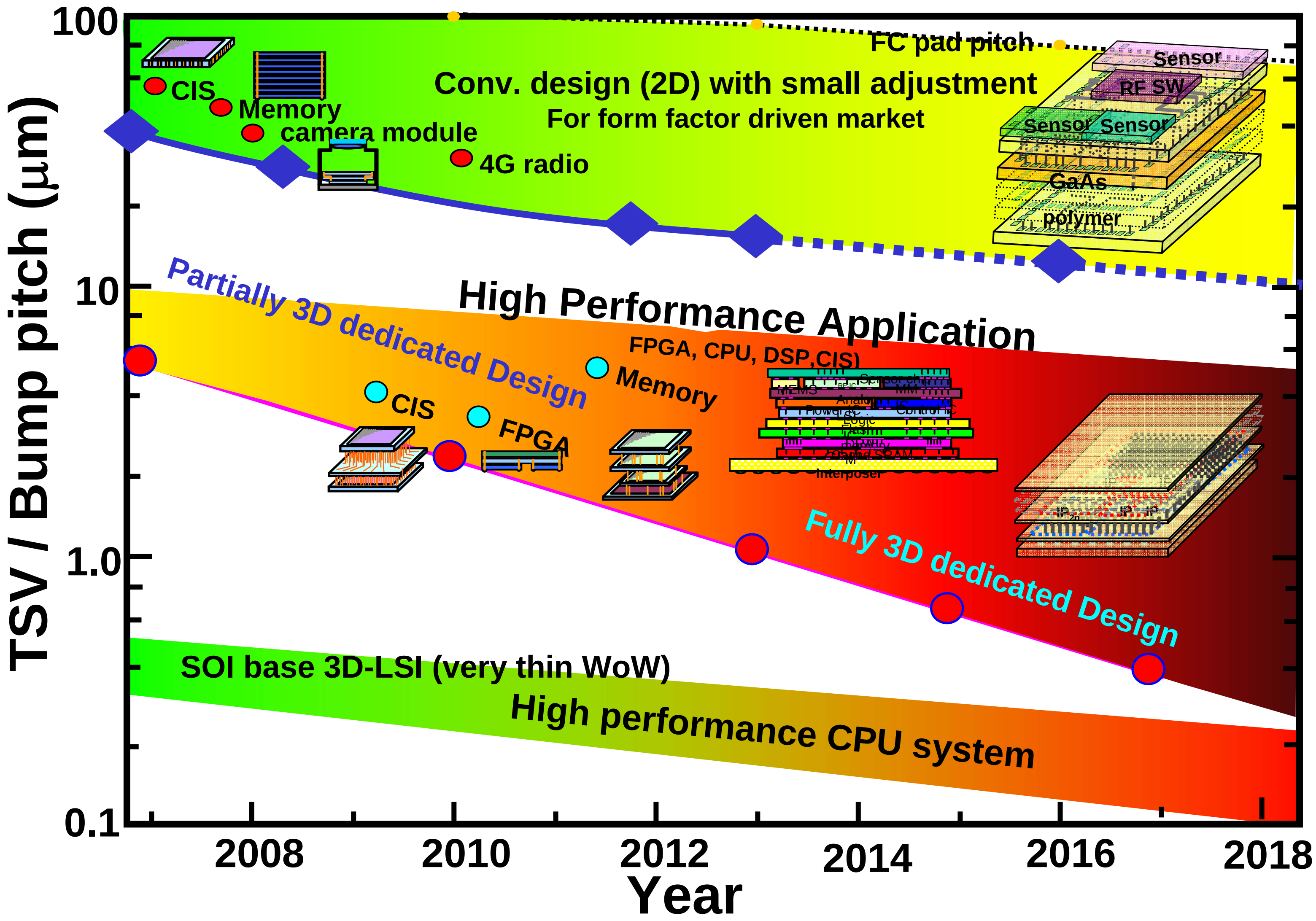
# Road Map of TSV & Bump pitch



# Determination for 3D-LSI process and TSV dimension

**Application** SoC, Memory , Sensor, FPGA

**Supply Chain of base wafer**

procure each wafers from one supplier or multi-supplier

New design or stack conventional LSI chips

**Main purpose of 3D-LSI**

-Performance

-Form Factor

-Cost reduction

-New architecture

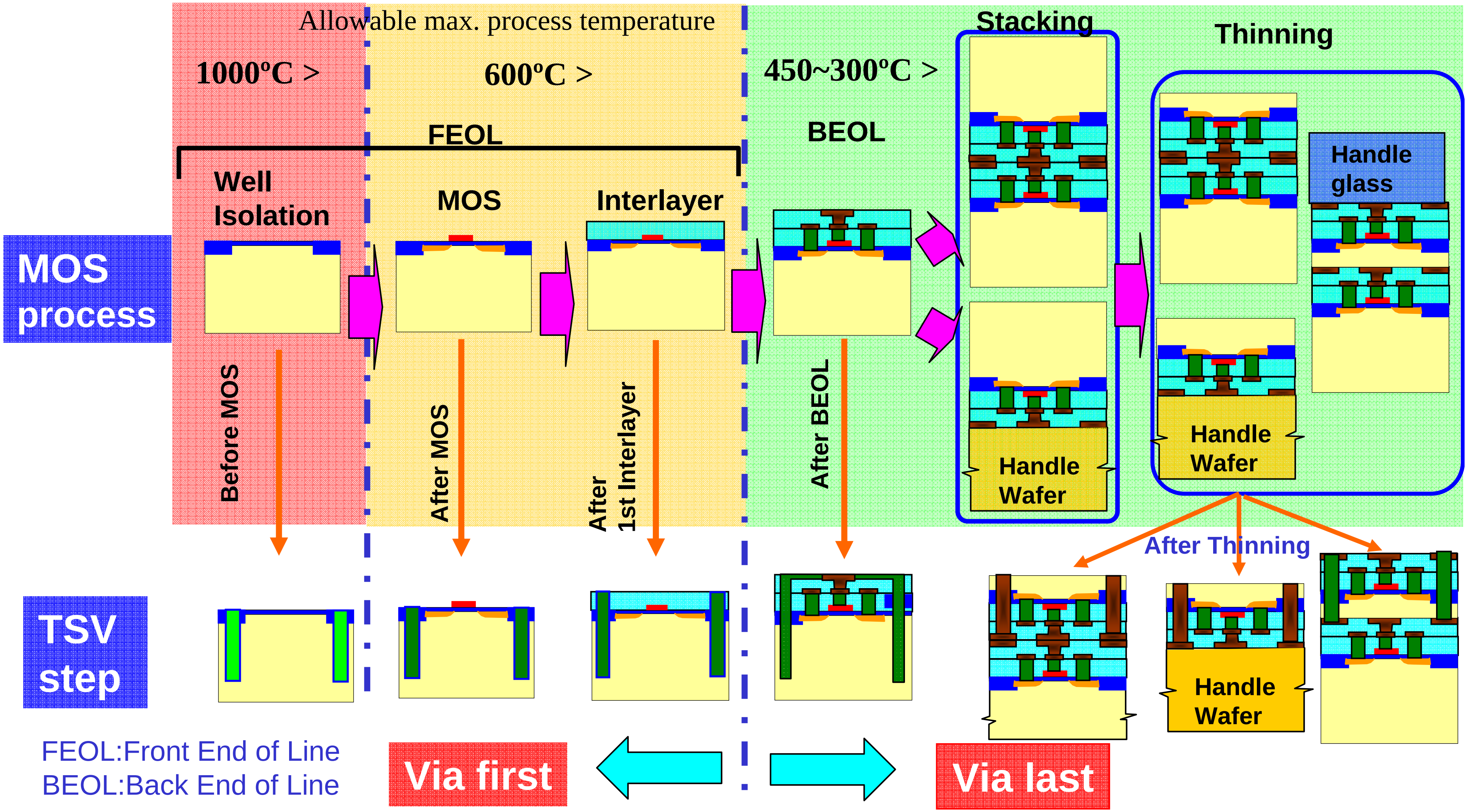
**TSV dimension**

| | | | | |
|---|---|---|---|---|
| TSV diameter | <1um | ~10um | 10~50um | >50um |
| TSV depth | <10um | 10~100um | | >100um |
| TSV density | $<10^6/mm^2$ | $10^2 \sim 10^5/mm^2$ | | $<10^2/mm^2$ |

**TSV process Choice** Via First or Via Last

*TSVs with very wide range of diameter can be realized now. But there are few solution which satisfy target application, base wafer supply chain, purpose of productize 3D-LSI.*

# TSV process classification



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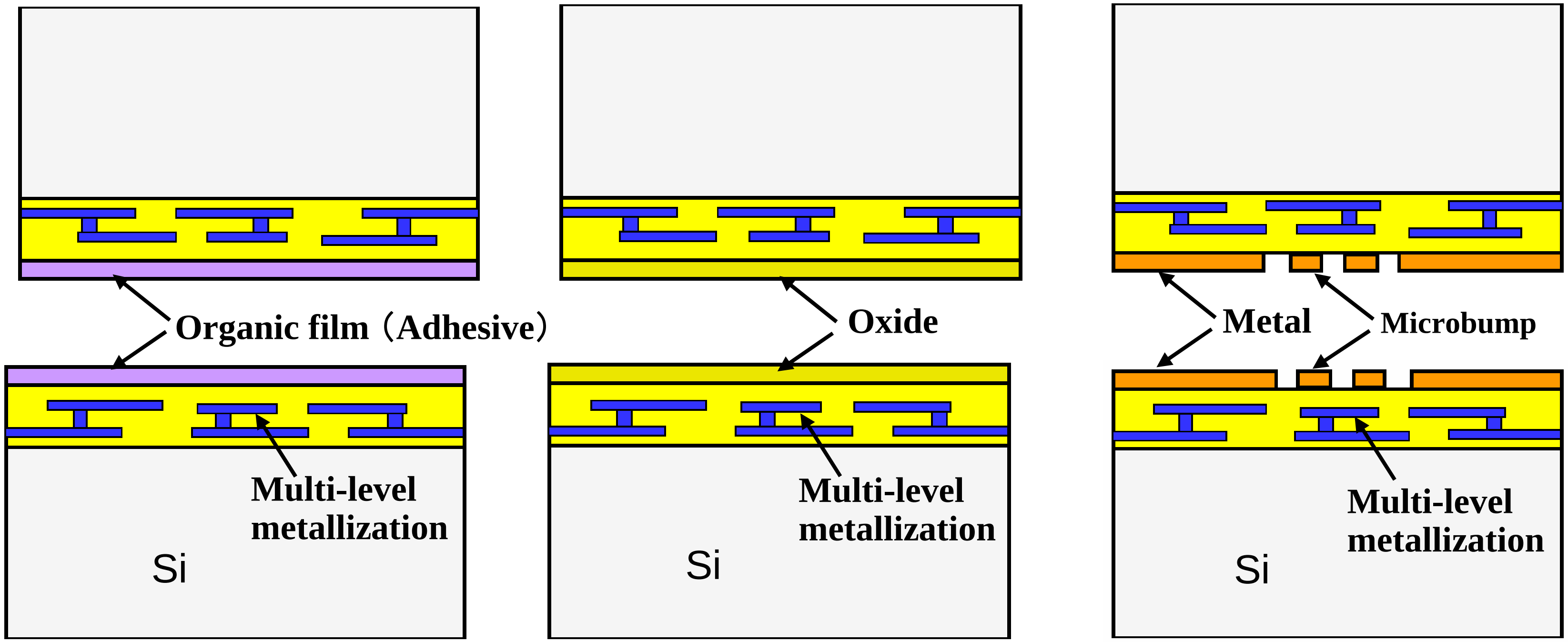
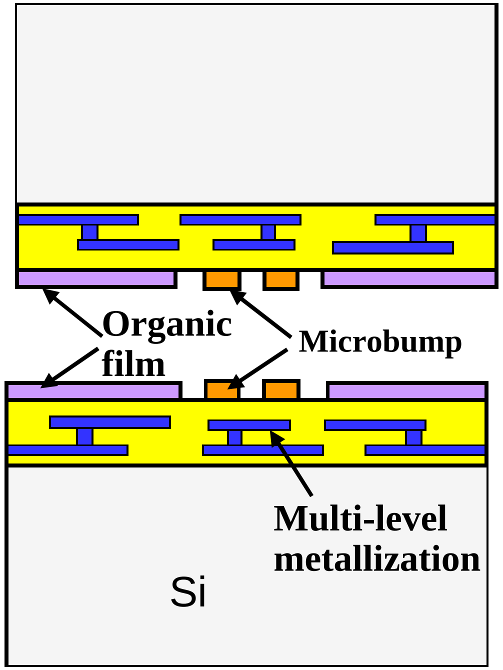
# Various Kinds of Wafer Bonding Methods (1)



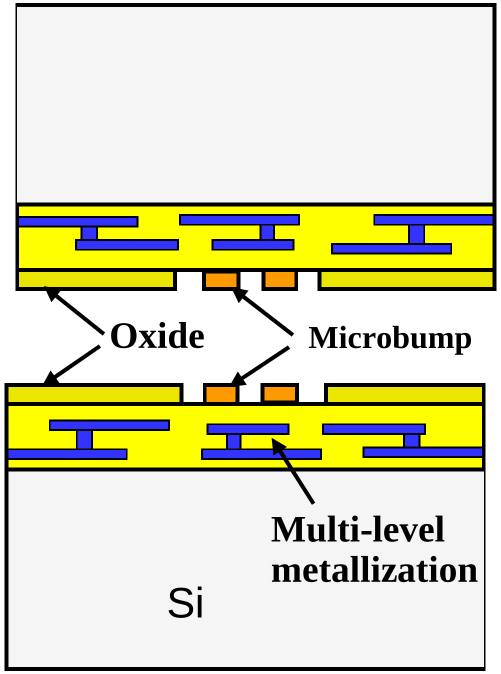

Adhesive Bonding | Direct Oxide Bonding | Direct Metal Bonding

# Various Kinds of Wafer Bonding Methods (2)

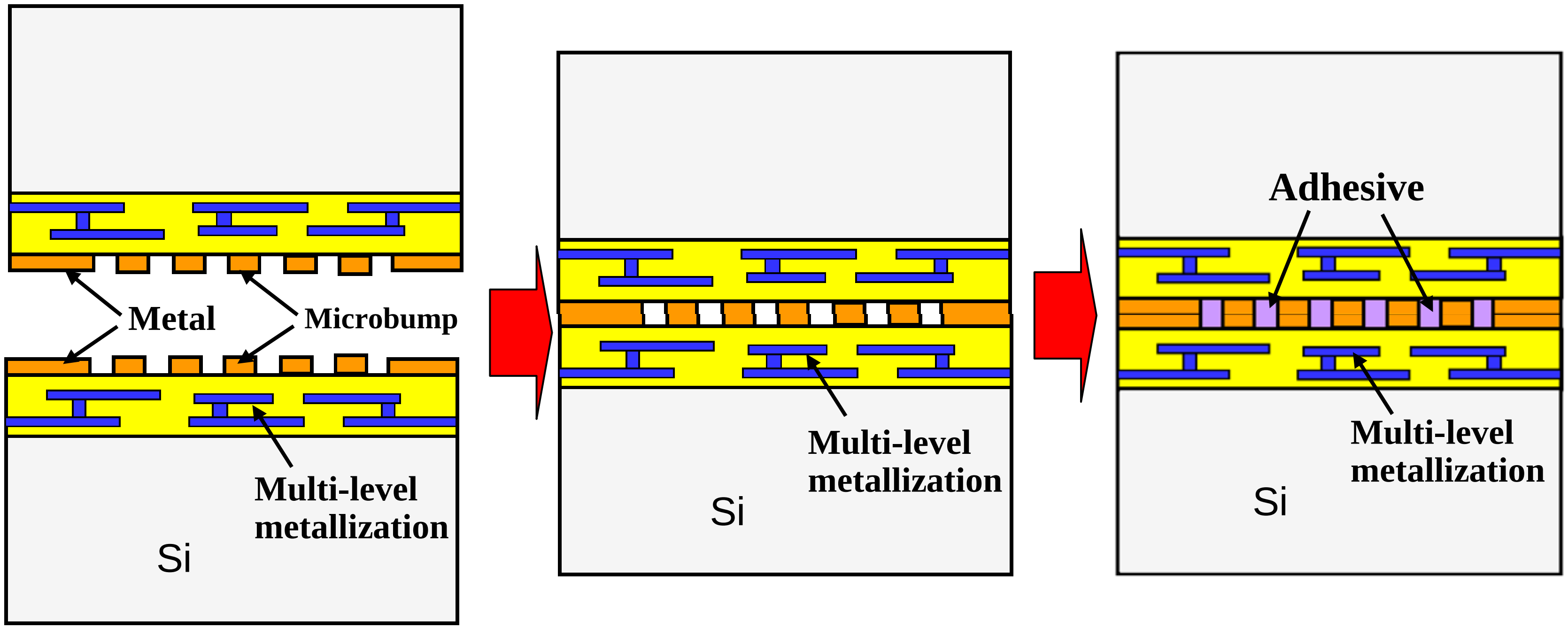



Adhesive/ Metal Bonding




Oxide/ Metal Bonding

# Various Kinds of Wafer Bonding Methods (3)
## (Tohoku University)

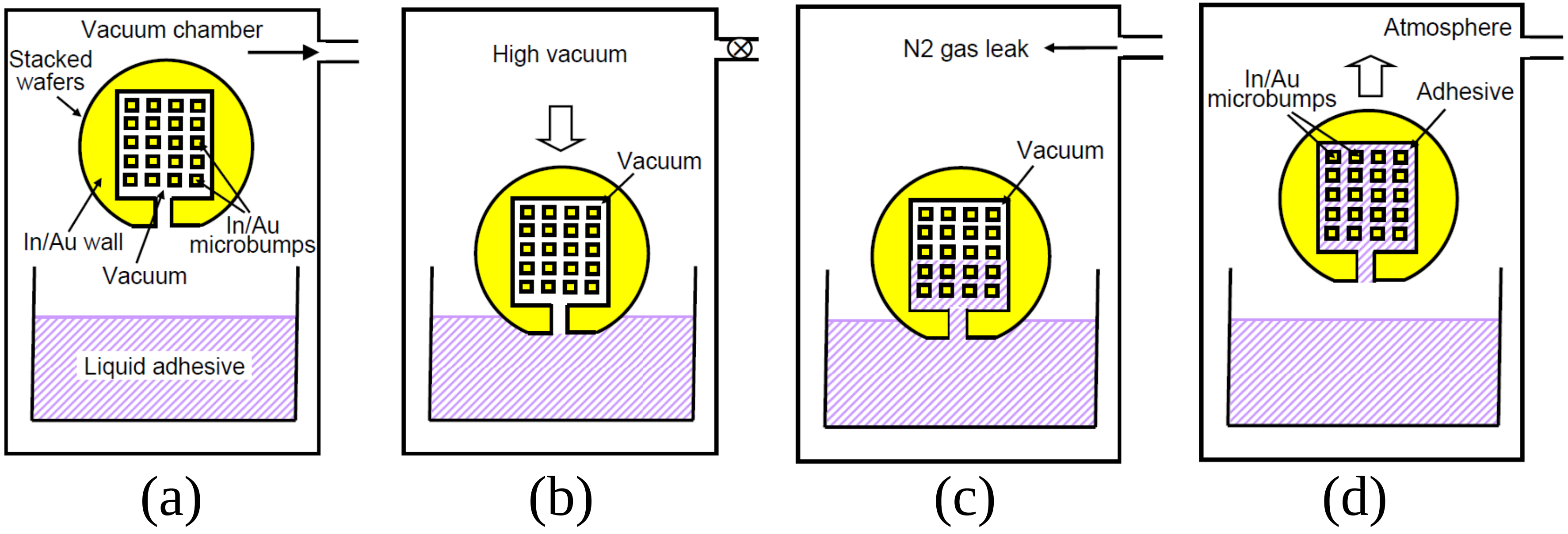



Wafer Alignment

Temporary Bonding (Metal Bonding)

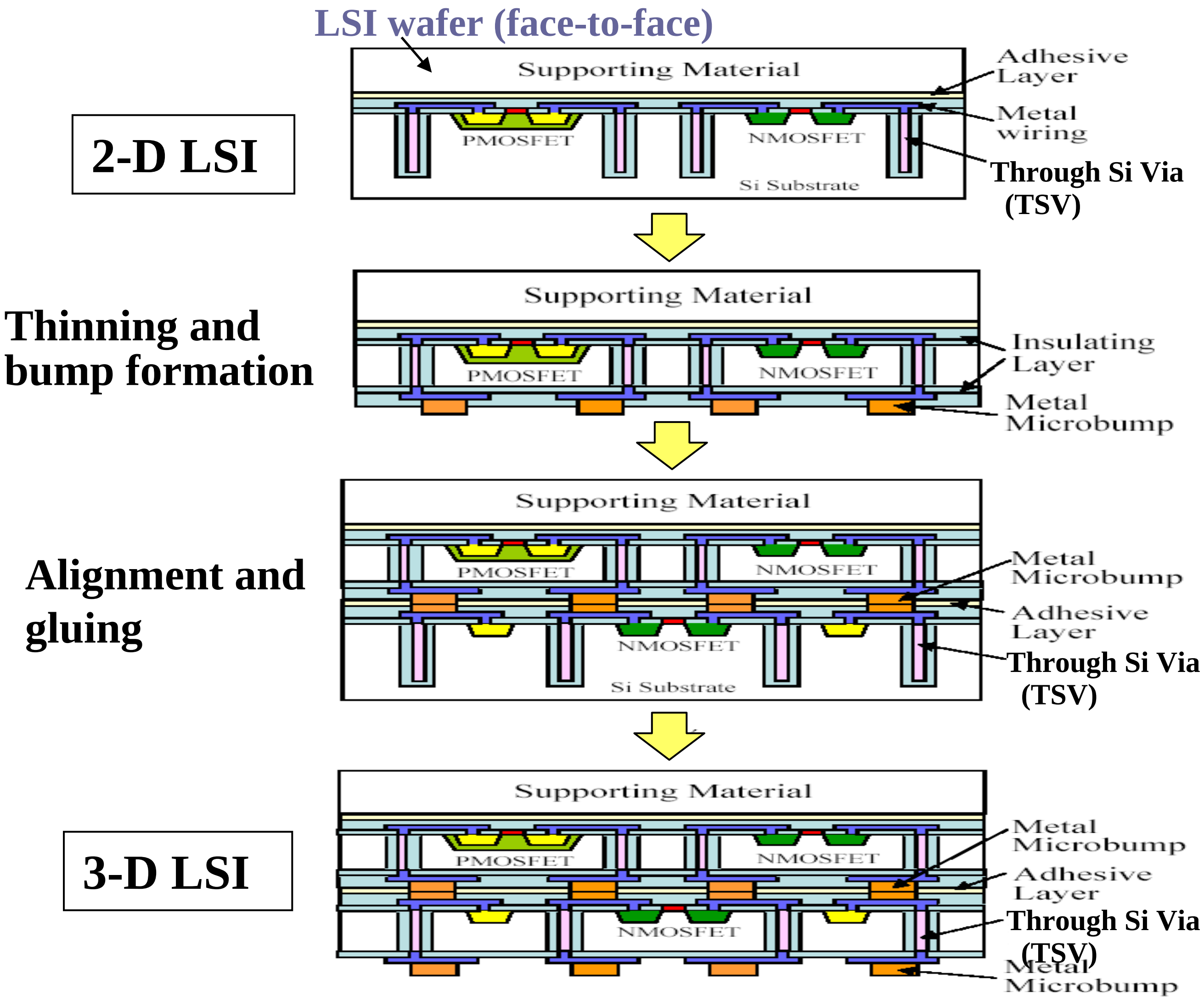
Adhesive Injection

# Process Sequence of Adhesive Injection Method




T. Matsumoto and M. Koyanagi et al, SSDM, pp.460-461, 1997.

# Fabrication Sequence of 3D LSI



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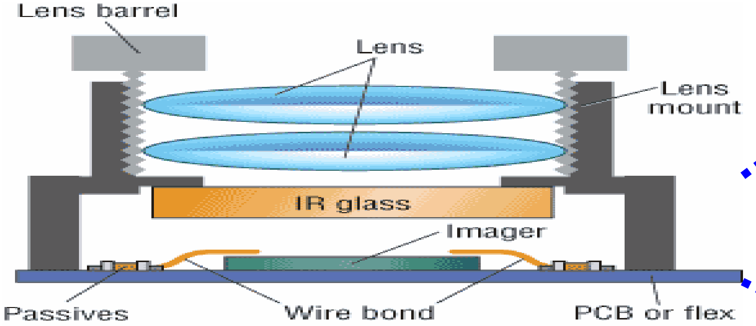
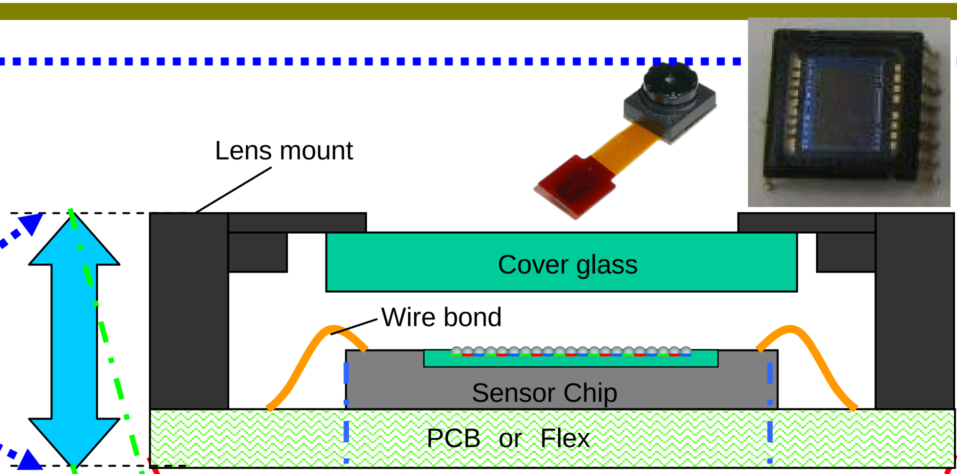
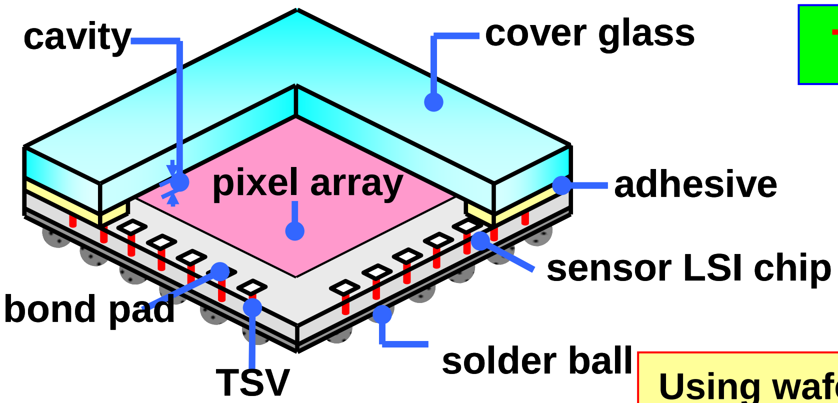
# The necessity of 3D-LSI Technologies for an Image sensor

## 【Conventional COB 】



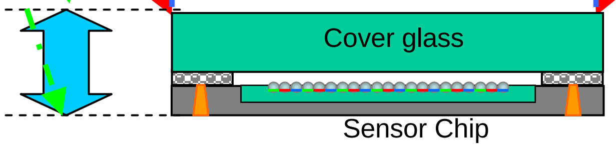




## 【ZyCSP™】



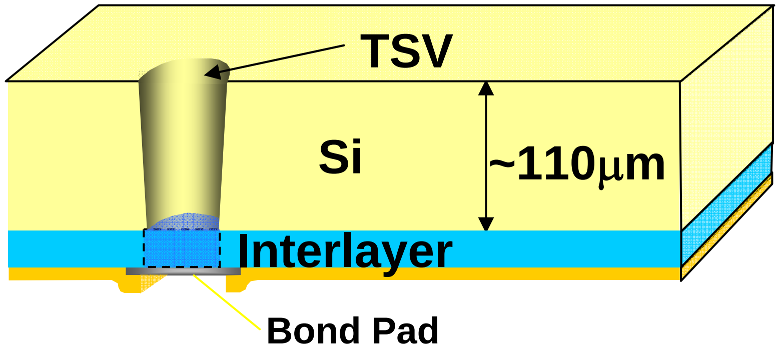

**Thinner**

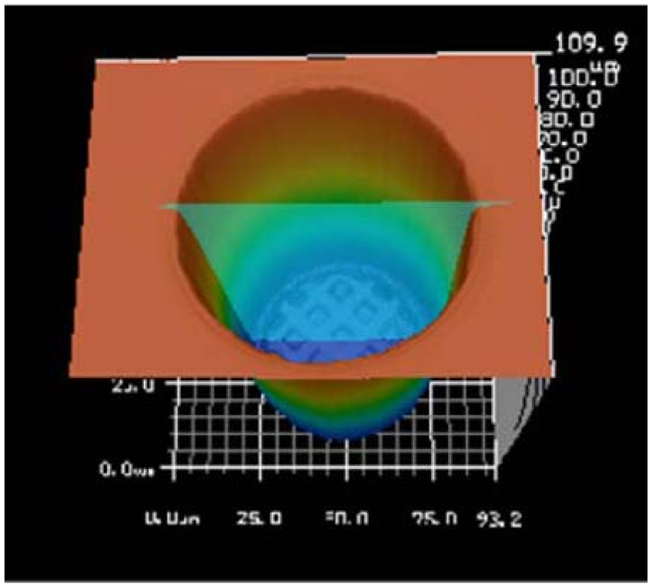
**Smaller**

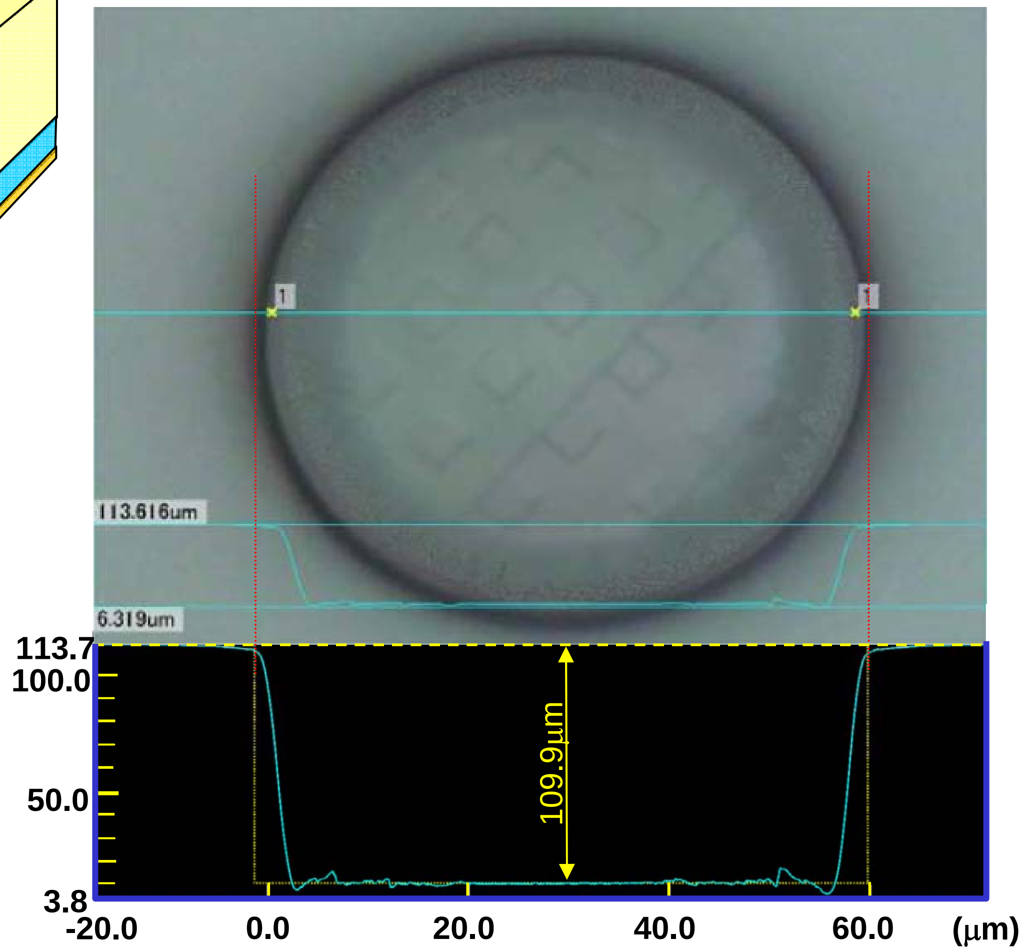



**Using wafer thinning & TSV techniques of 3D-LSI technology**

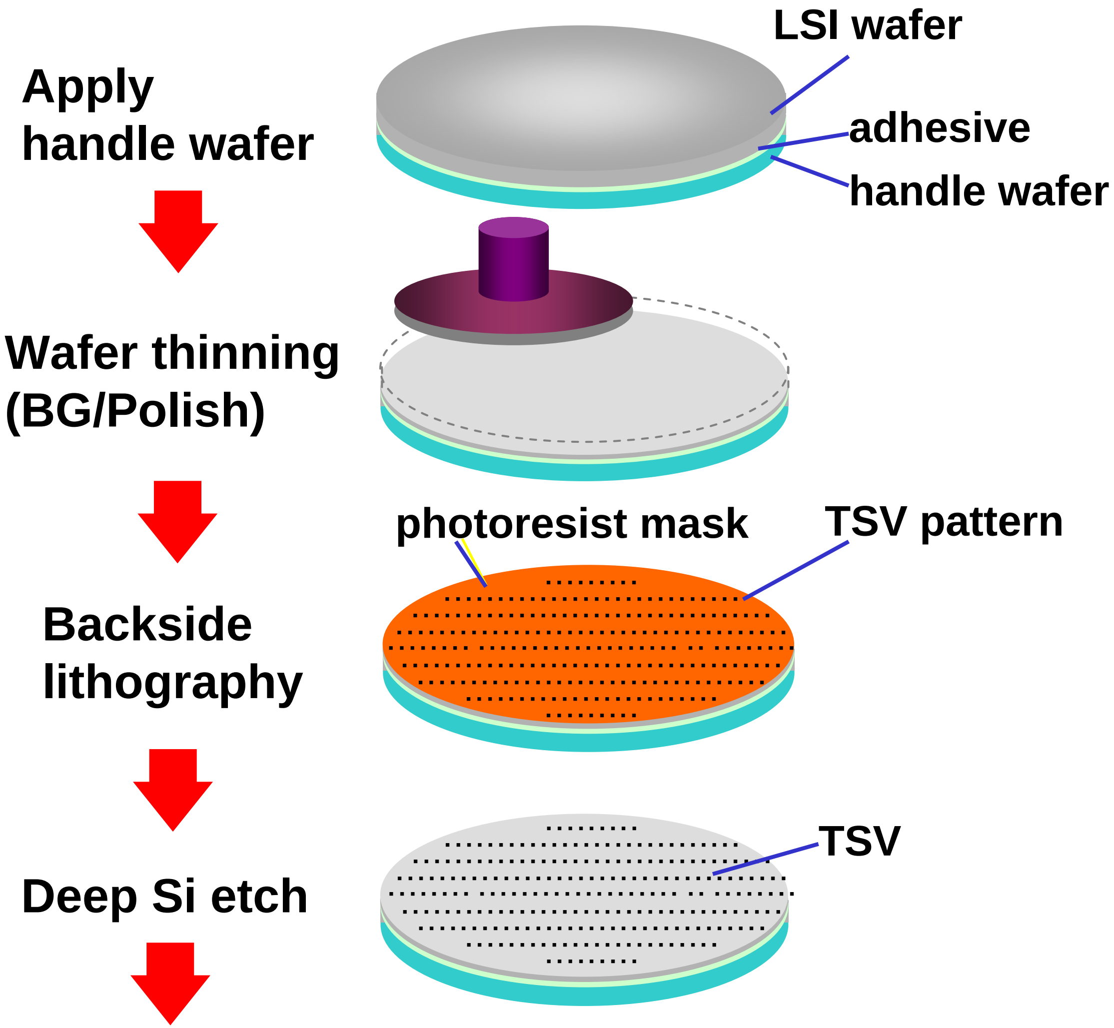
# 50μmϕ (80μm pitch) TSV

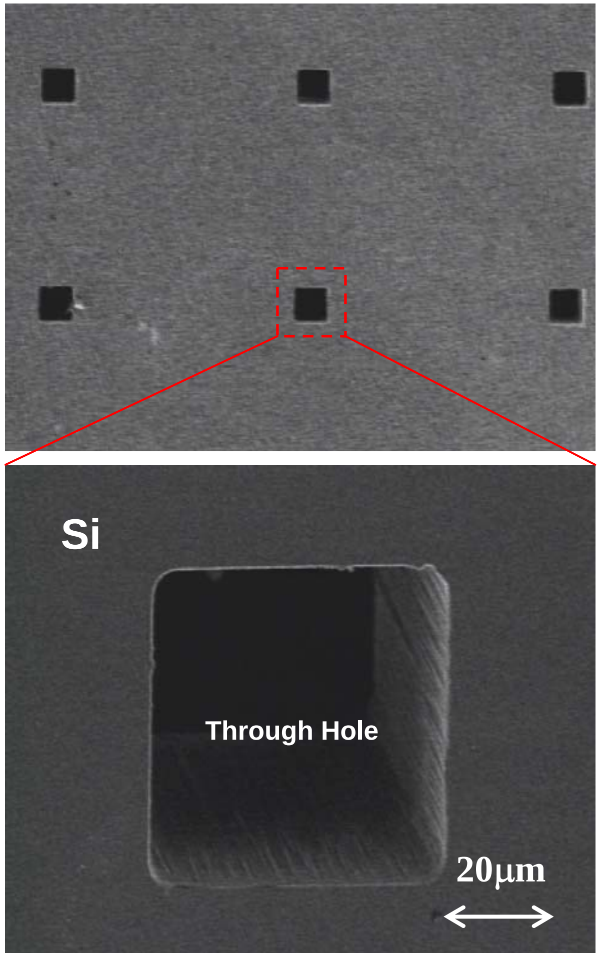


# ZyCSP™ Process Sequence (1)



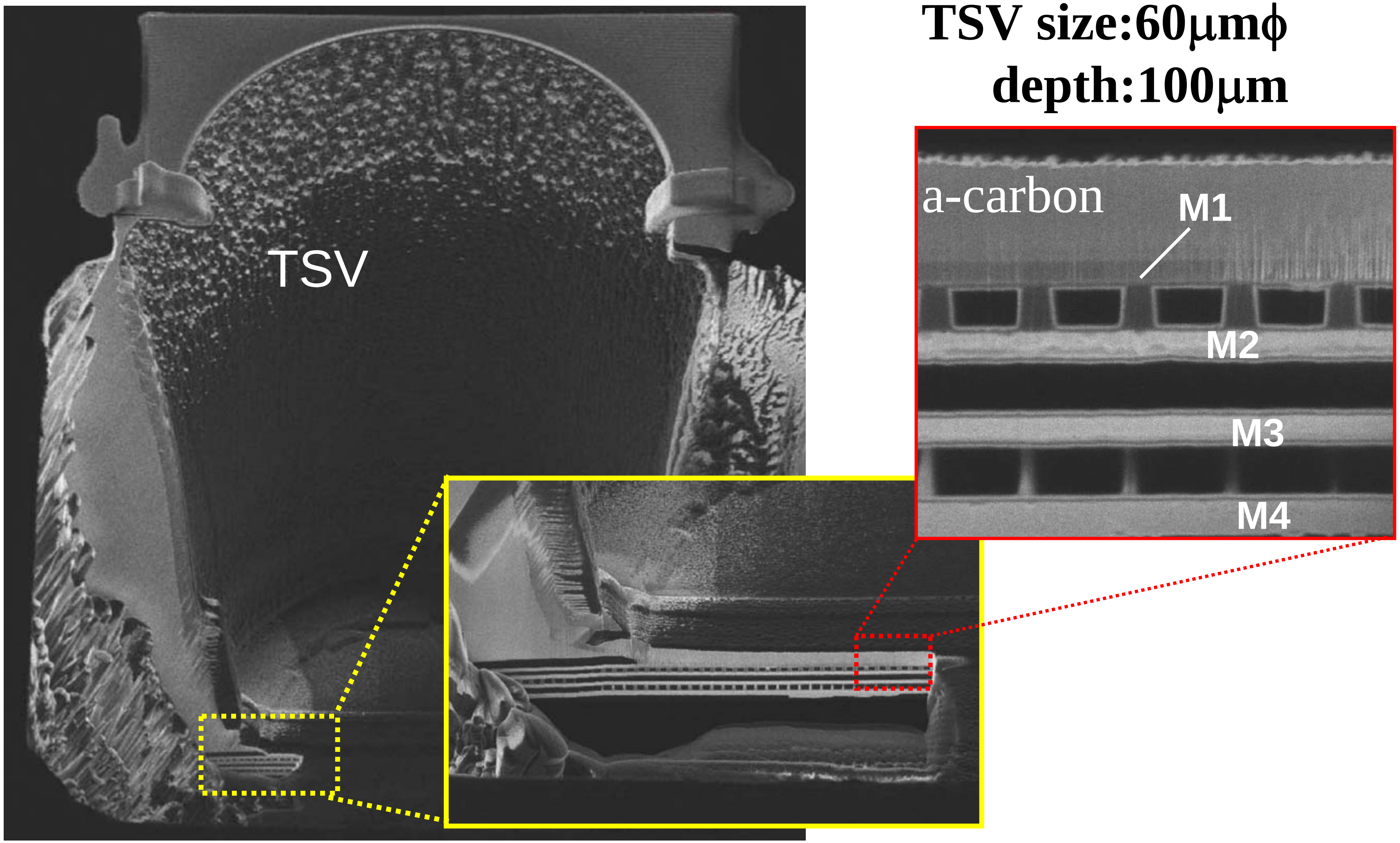




TSV after deep Si etch

# TSV after $SiO_2$ RIE

**TSV size:60μmϕ**
**depth:100μm**

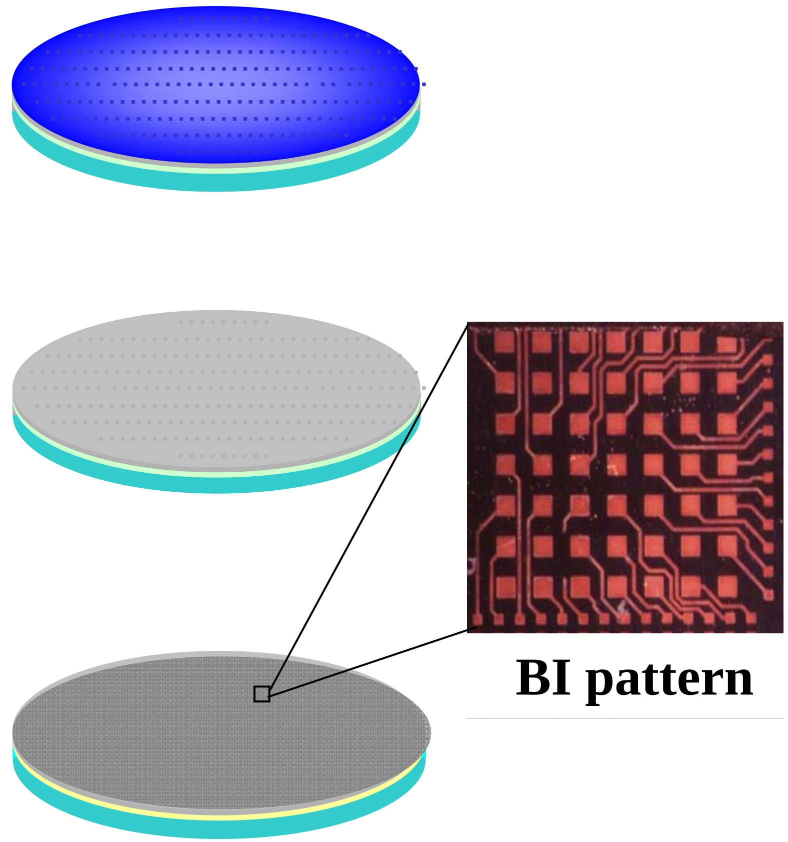


# ZyCSP™ Process Sequence (2)

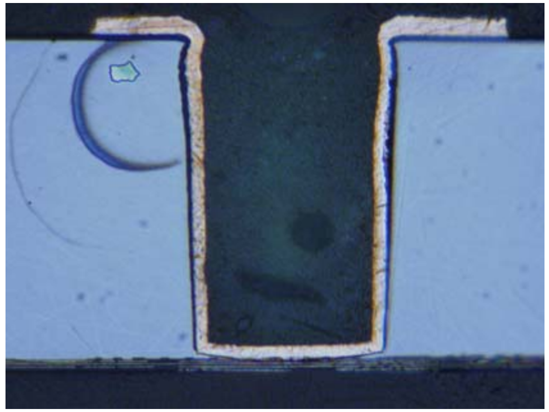
**Side wall insulation**

**Applying metal conductor**

**Form Backside Interconnect (BI)**



**BI pattern**



**TSV cross section after forming BI**

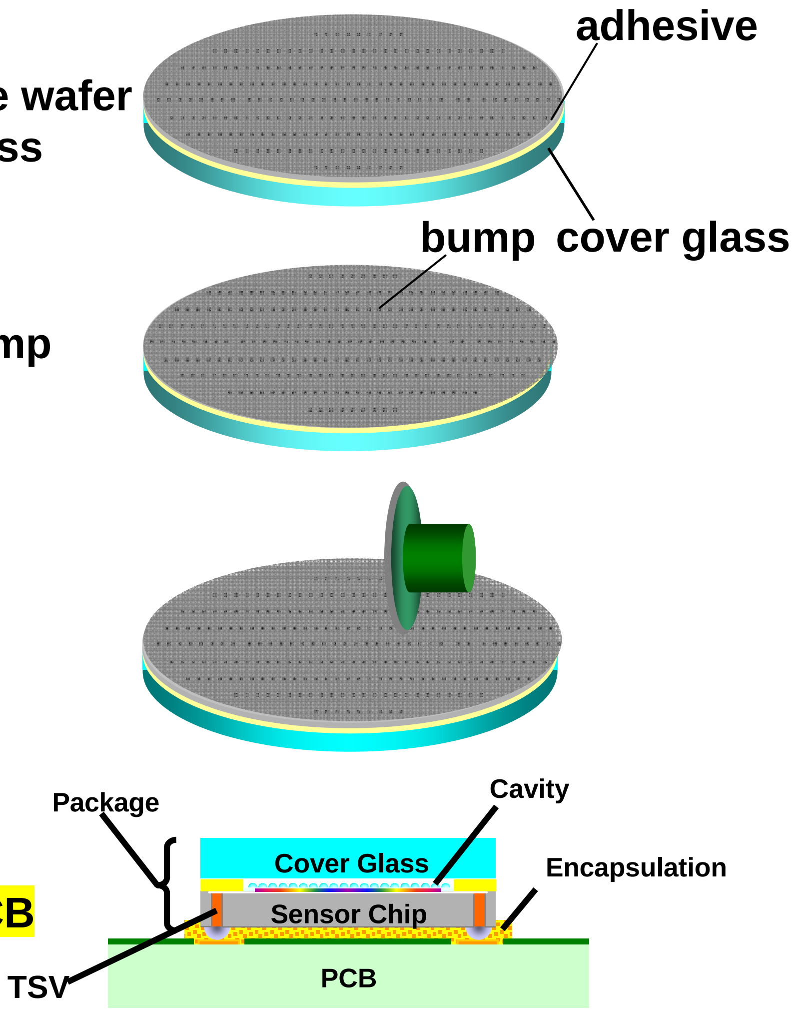
# ZyCSP$^{TM}$ Process Sequence (3)

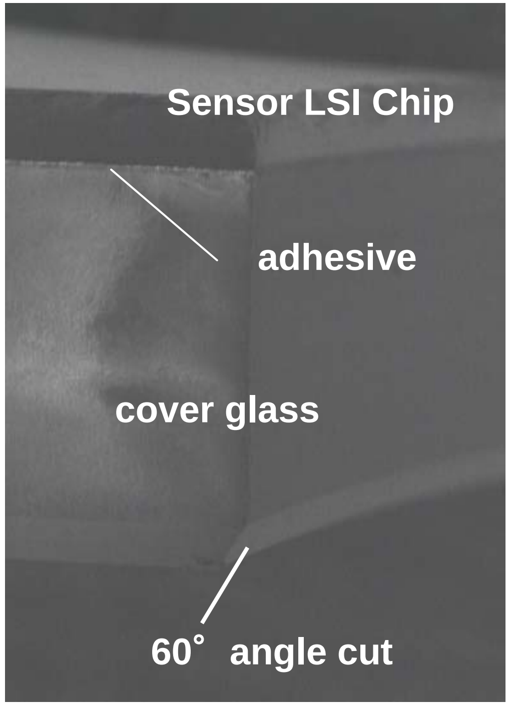
Replace handle wafer with Cover Glass

Forming Bump

Dice

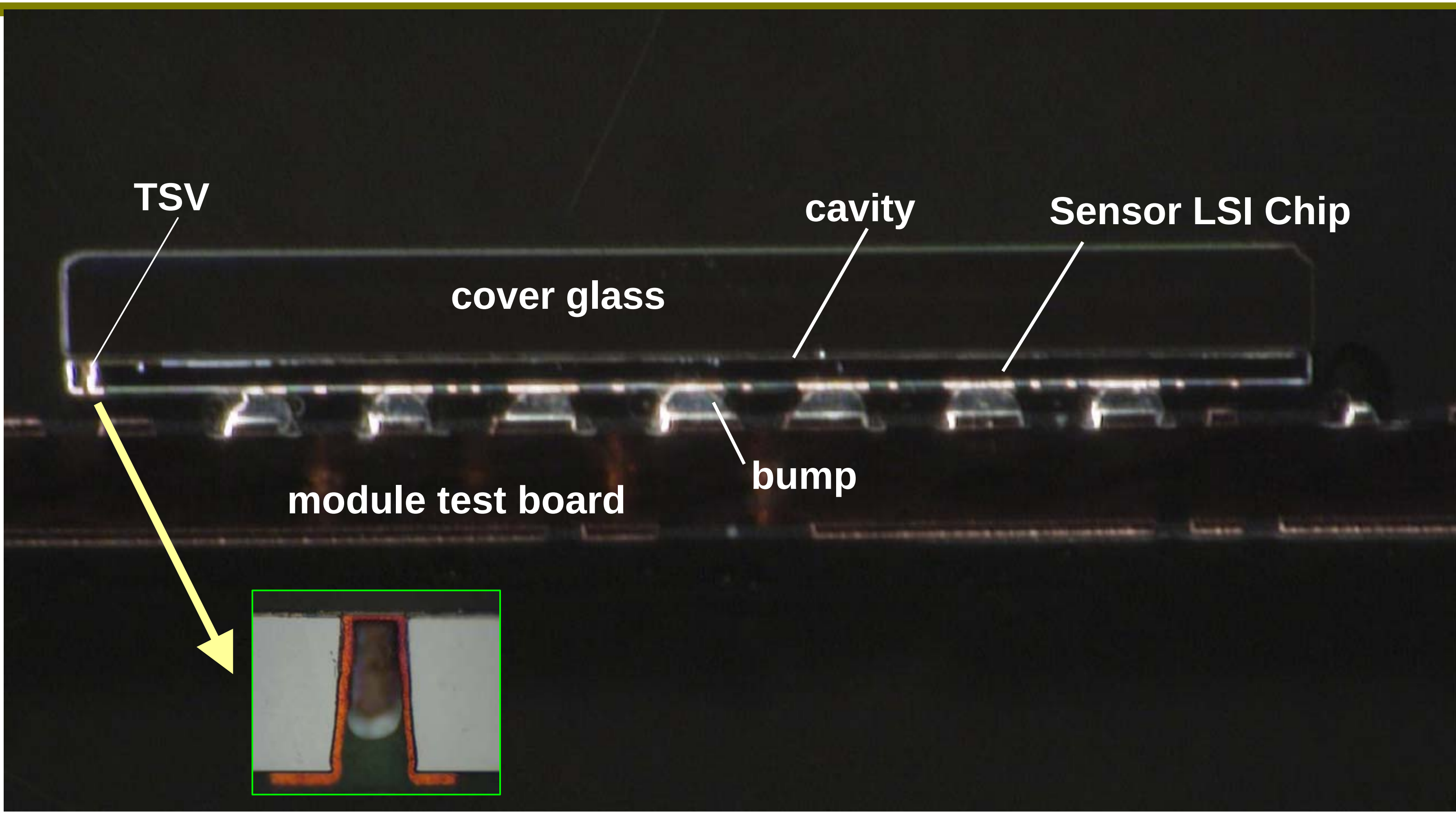
Mount on PCB




Edge of ZyCSP$^{TM}$

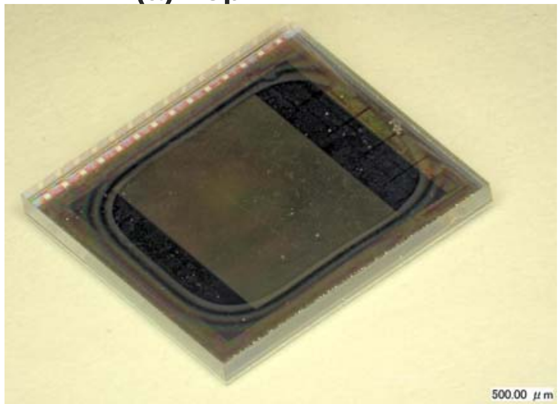
# ZyCSP™ mounting on the test board



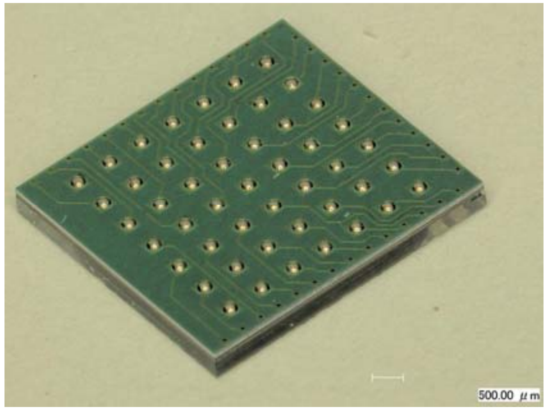
# The ZyCSP™ for the camera module

## 1.3M pixel Sensor LSI

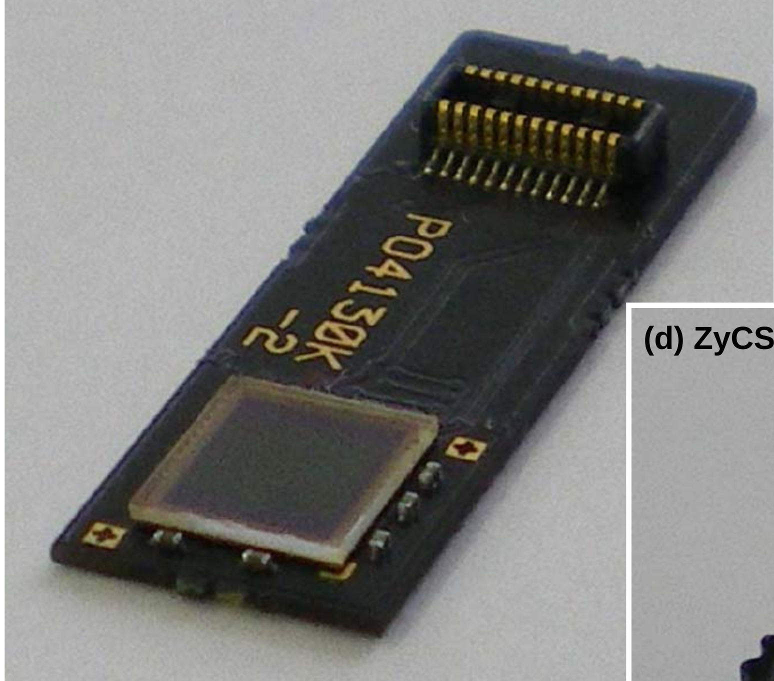
(a) Top




(b) backside

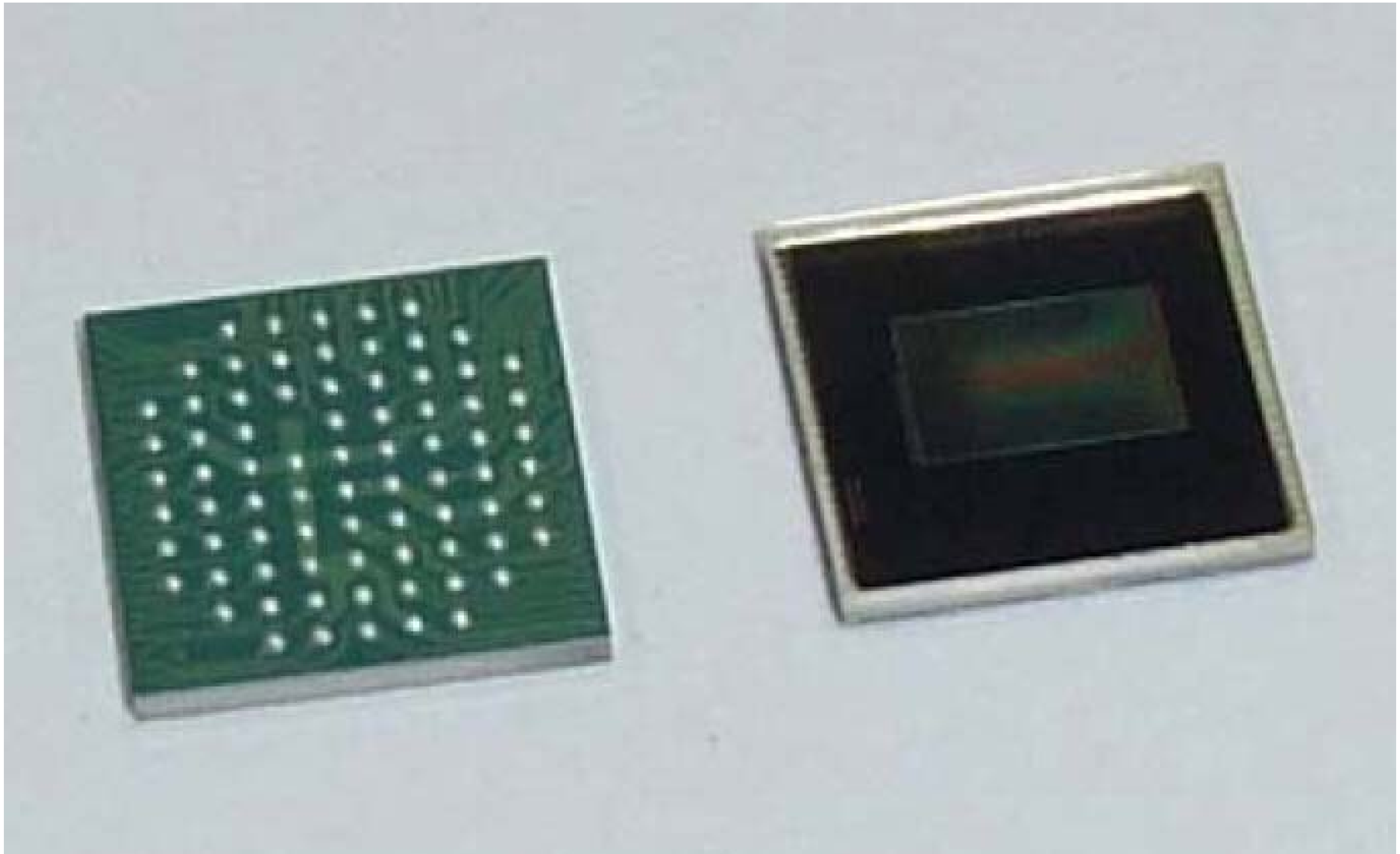



(c) ZyCSP mounting on module board



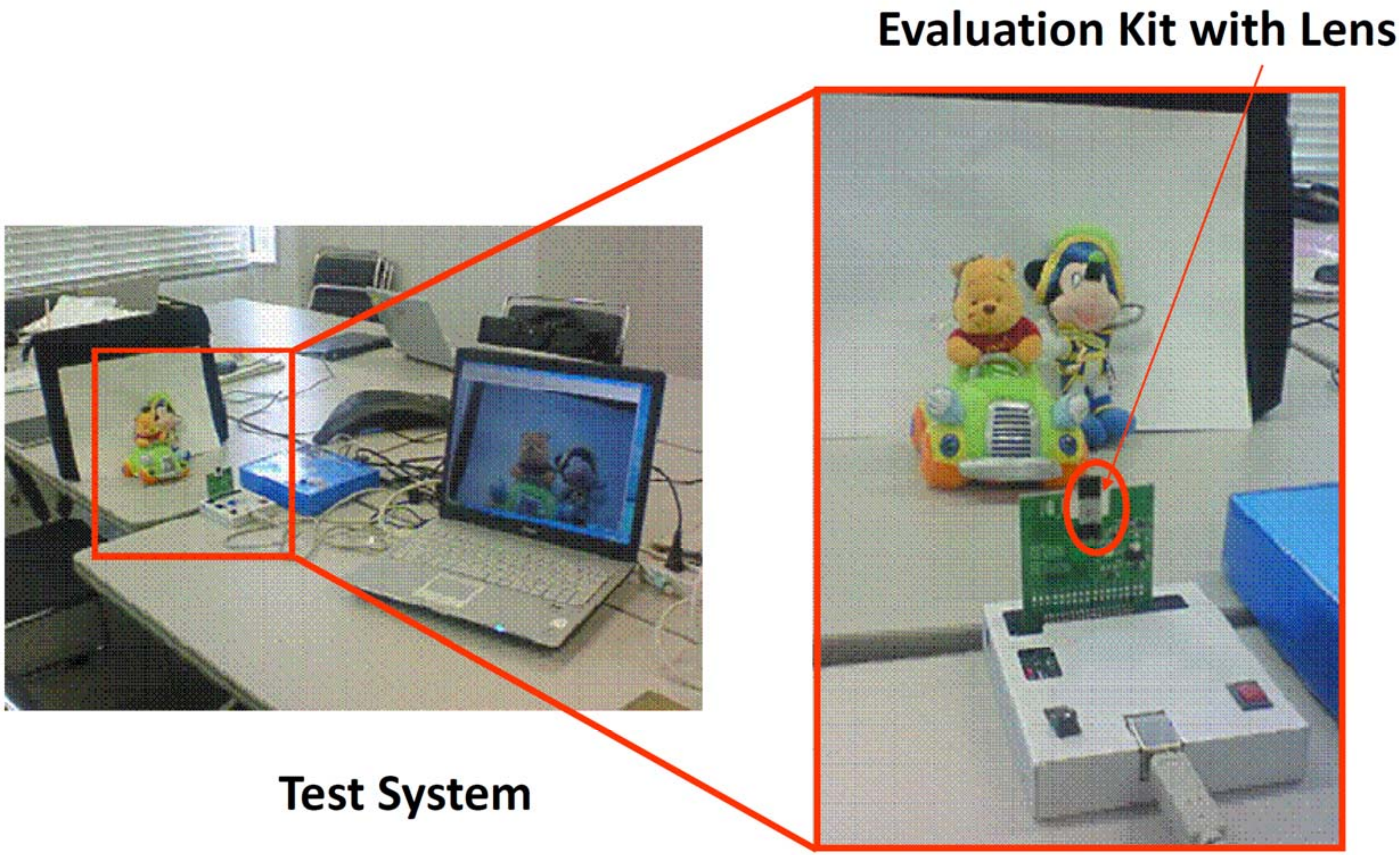

(d) ZyCSP module with a Lens unit

# 2M pixel Sensor CSP

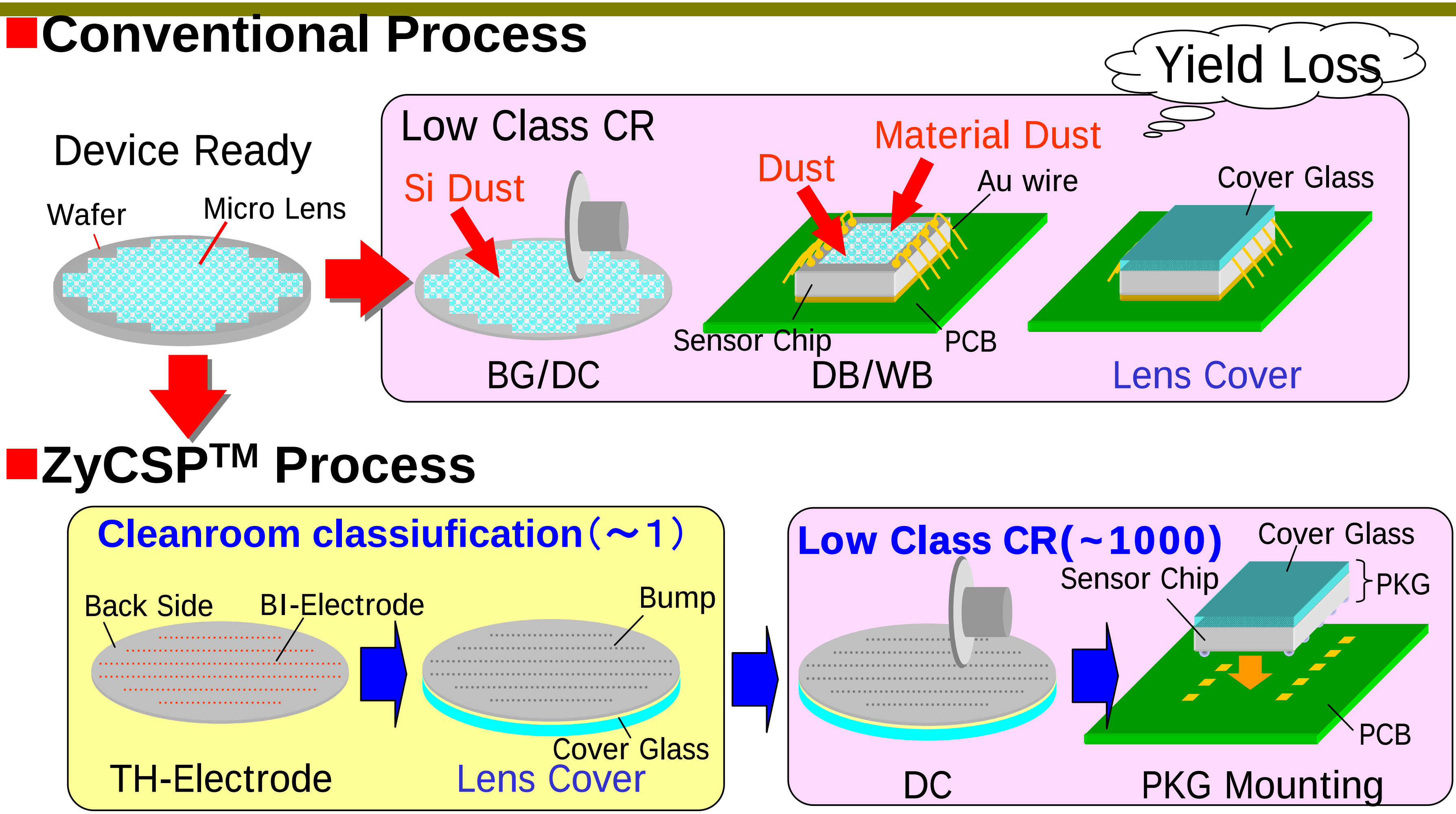


# Working Sample Test System



# Fabrication Processes Comparison




*High Yield utilizing Wafer Level Process*

# Outline



# Current 3D-LSI Technologies

**Advantages**

-Available to use existing LSI chip design w/o or w/ minor modification

-Reduce foot print eg. multifunctional SoC, High density memory

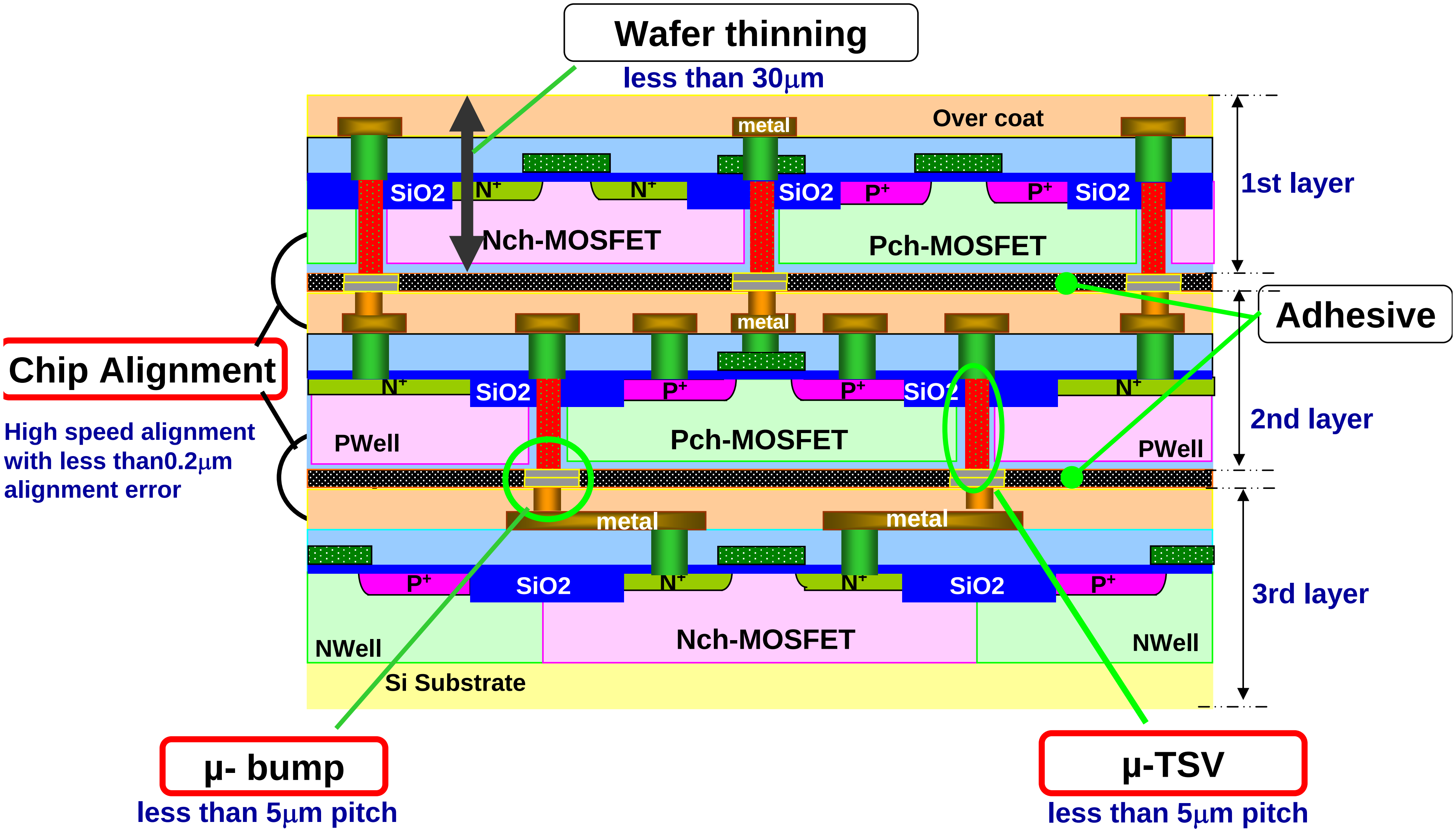
Get the best performance out of 3D-LSI

# Next Generation 3D-LSI Technologies

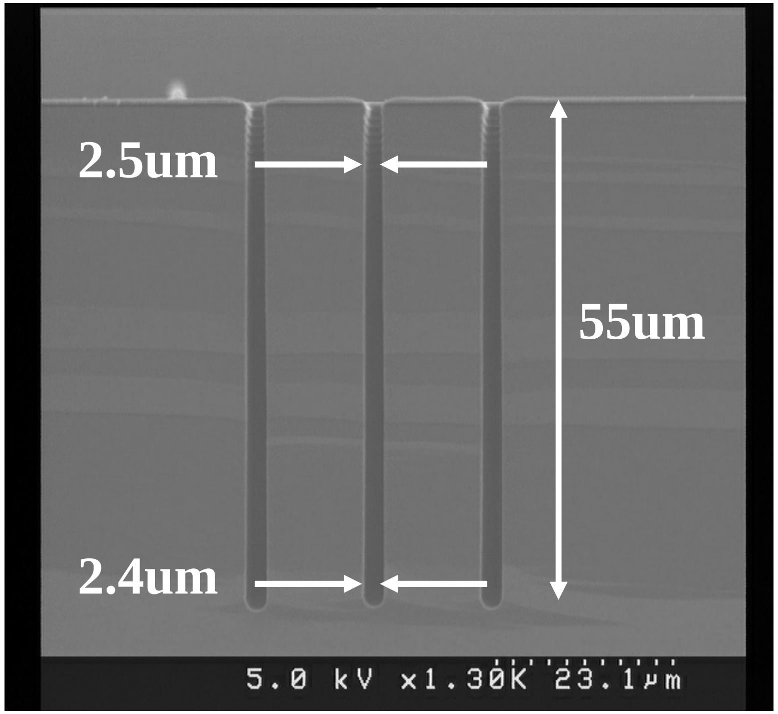
  

# Next Generation 3D-LSI Technologies

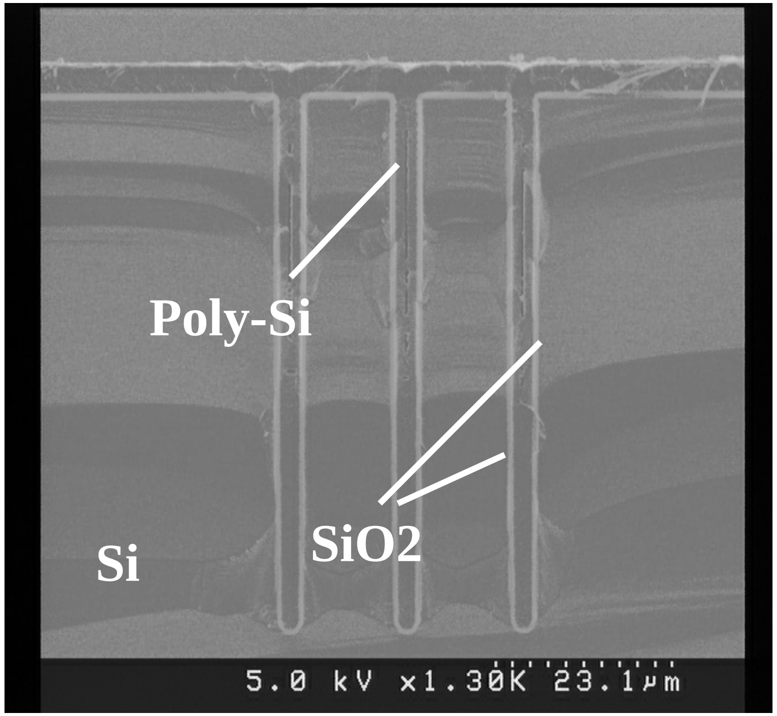
## 5Key technologies



# SEM Cross Section of Poly-Si TSV
## (Via first)




(a) Si deep trench etching

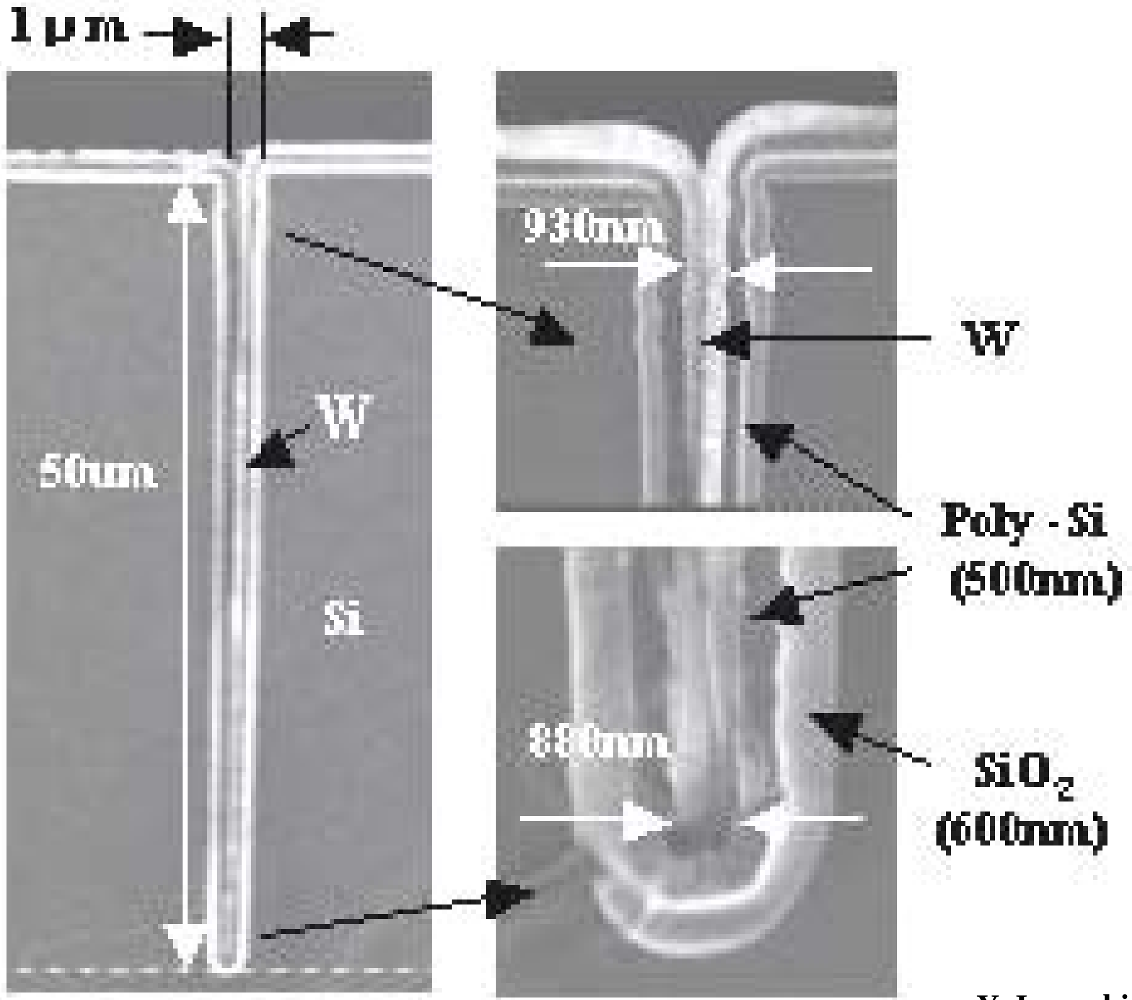



(b) Filling with Poly-Si

T. Matsumoto and M. Koyanagi et al., SSDM, 1995.

# SEM Cross Section of W/ Poly-Si TSV

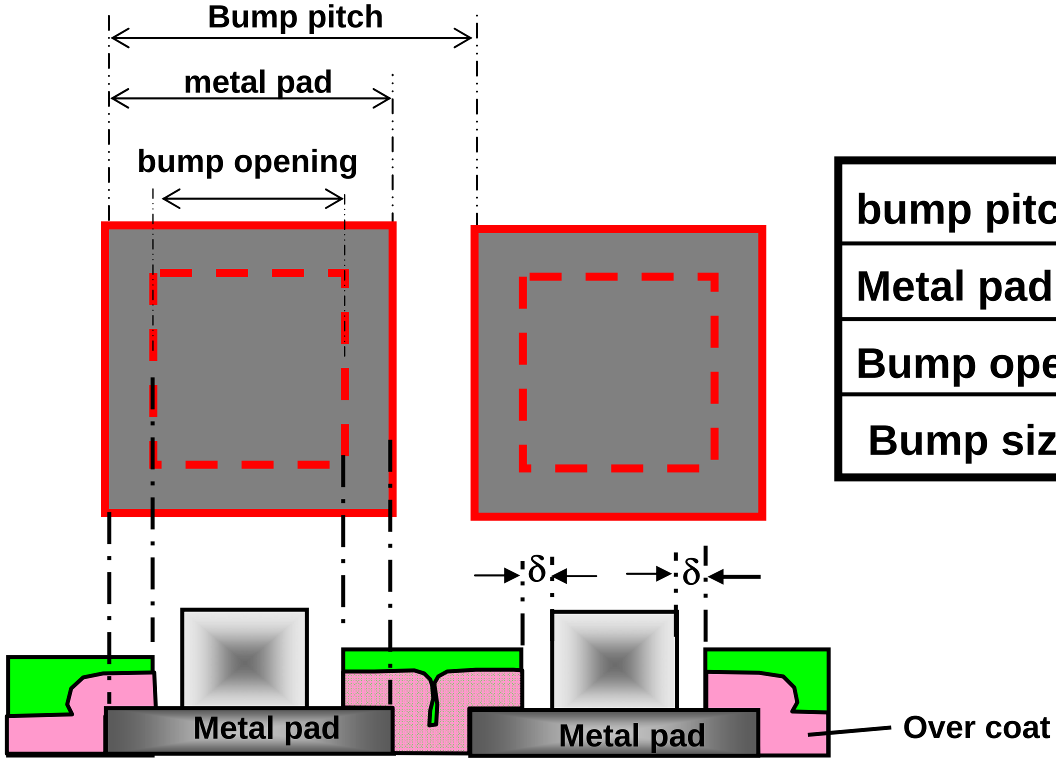
## (Via first or Via before BEOL)




**Adsorption time**
**tad = 1sec**
**Reduction time**
**tred = 15sec**
**Evacuation time**
**tevc1 =5sec**
**tevc2 = 5sec**
**Deposition temperature**
**350℃**

**Y. Igarashi and M. Koyanagi et al., SSDM, 2001.**

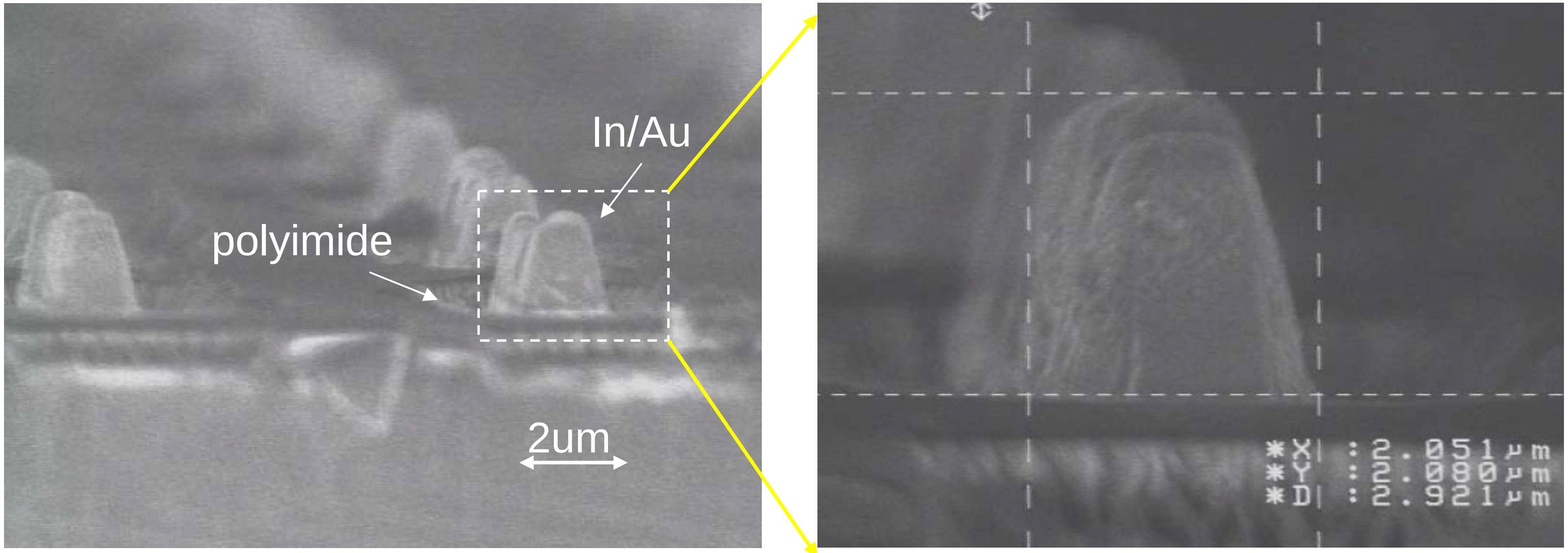
# Schematic Diagram of micro-bump structure using new micro-bump fabrication process



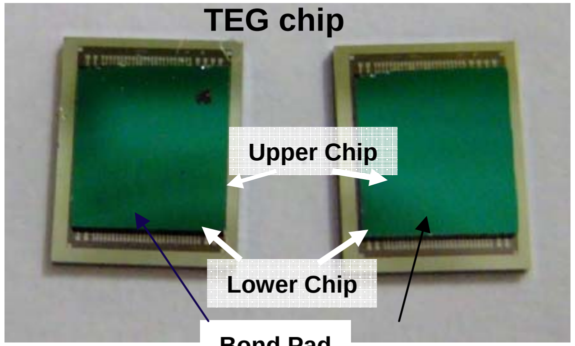

| | |
|---|---|
| bump pitch | 5.0 μm |
| Metal pad | 4.0 x 4.0 μm |
| Bump opening | 3.0 x 3.0 μm |
| Bump size | 2x2 μm (bottom) |

**Clearance groove (δ) between bump opening and bump are formed by self-aligned process**

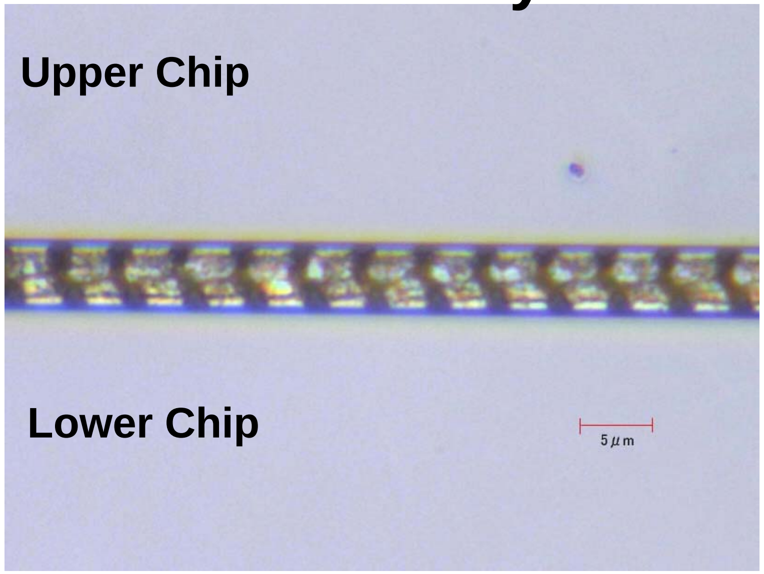
# 2μm x 2μm Bumps



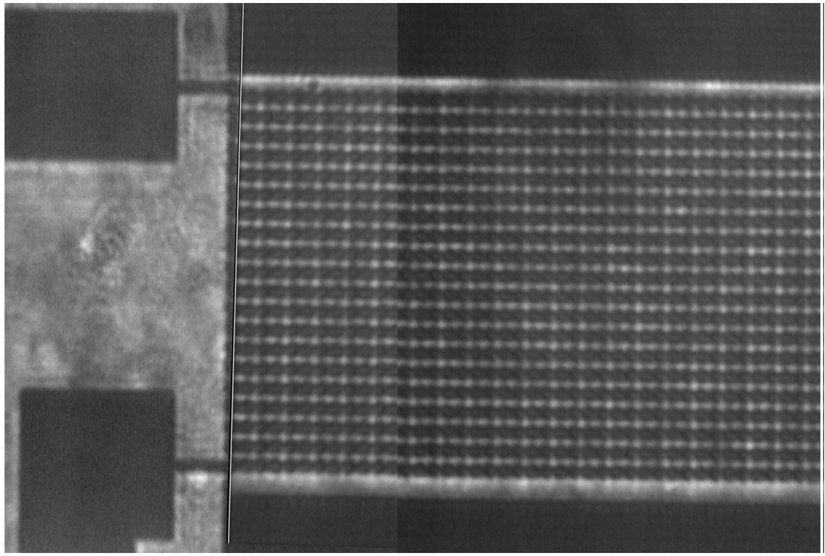
# 5μm pitch μ-bump




## Daisy Chain with $10^4$ m-bumps



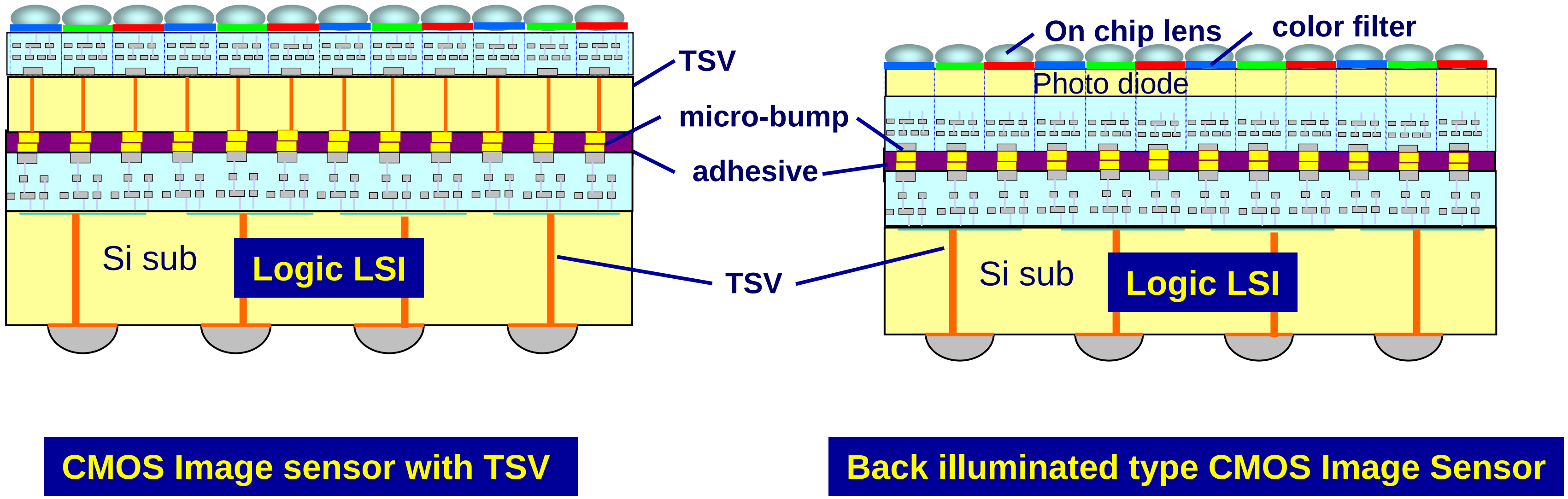

Cross section



Plain View（IR microscope)

Tohoku Univ. / ZyCube

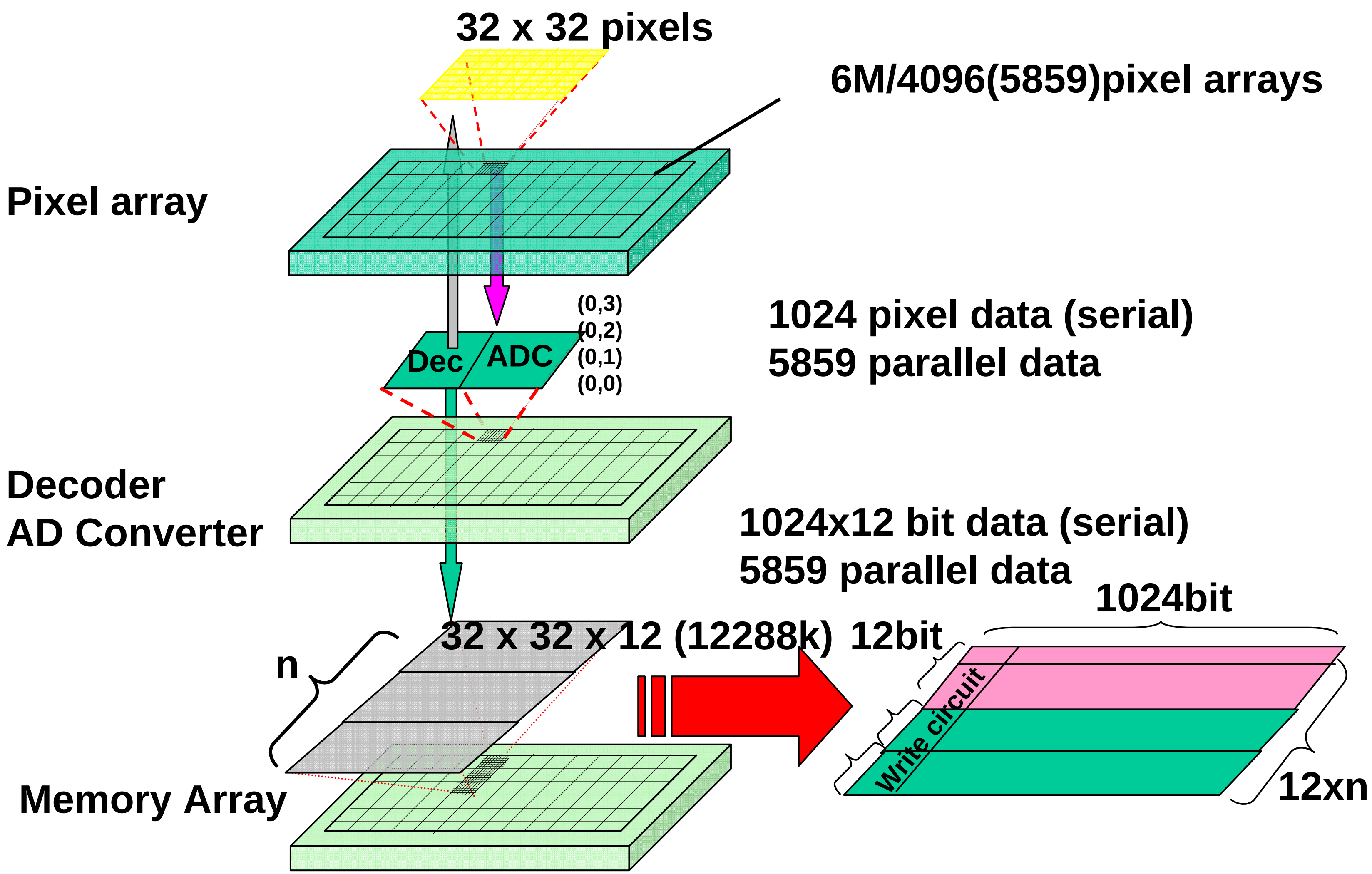
# Image sensor module with μ-bump & μ-TSV




*By connecting the back illuminated type CMOS image sensor to Logic LSI, a high speed Pixel detector system with 100% fill factor will be realize.*

ZyCube

# High Speed Parallel Processing Image Sensor with Memory



# 3D LSI Prototype Chips Fabricated in Tohoku Univ.

## Real-Time Image Processing System

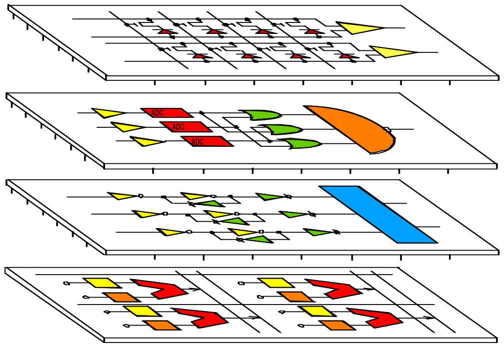


Image Sensor

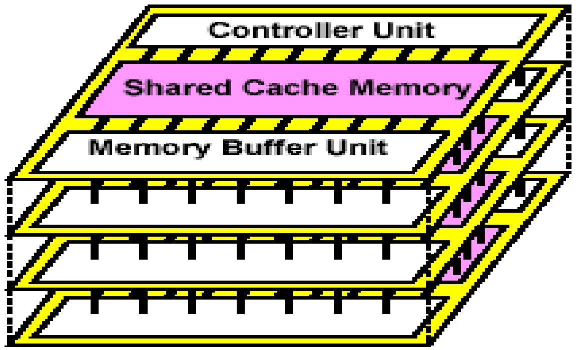
AMP & ADC

Register

Processor

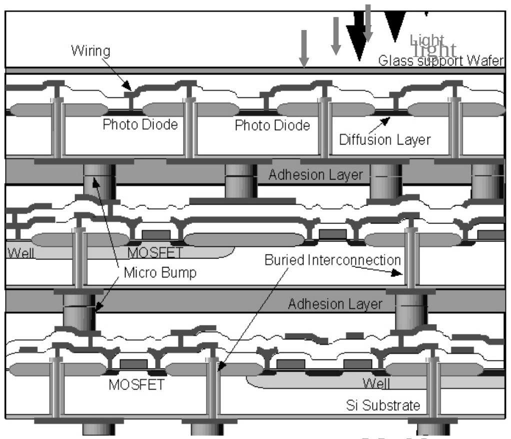
H. Kurino, M. Koyanagi *et al.*, IEDM (1999)

## 3D shared memory




K. W. Lee, M. Koyanagi *et al.*, IEDM (2000)

## 3D artificial retina chip




Quartz glass

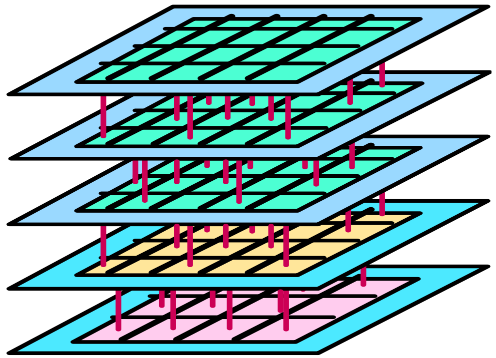
Photoreceptor layer

Horizontal cell &
bipolar cell layer

Ganglion cell layer

M. Koyanagi *et al.*, ISSCC (2001)

## 3D microprocessor chip



DRAM

DRAM

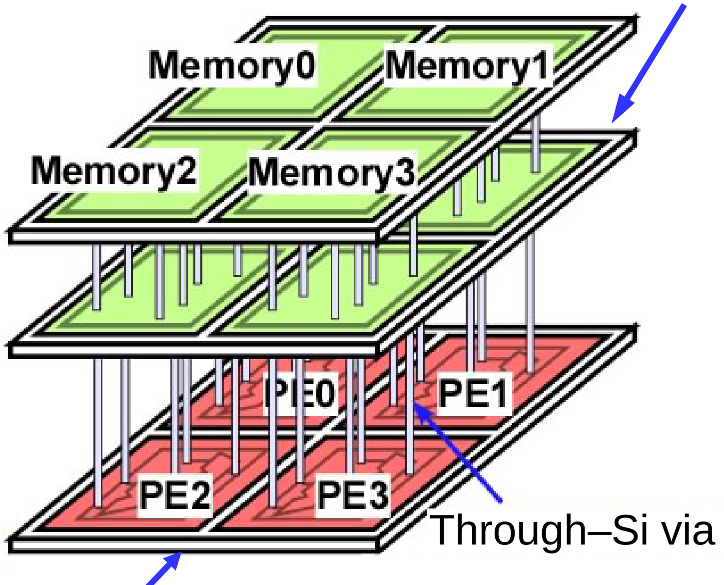
DRAM

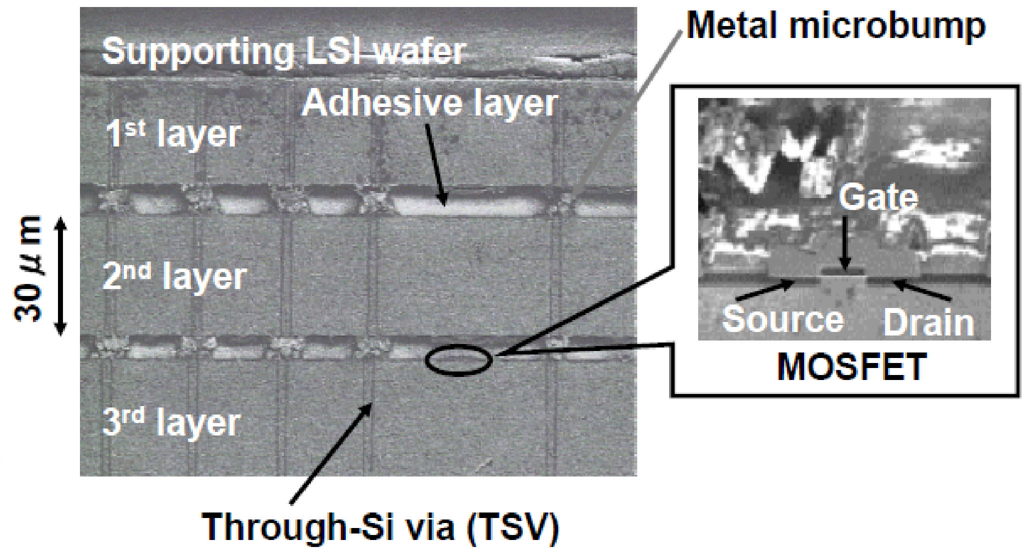
SRAM

Processor

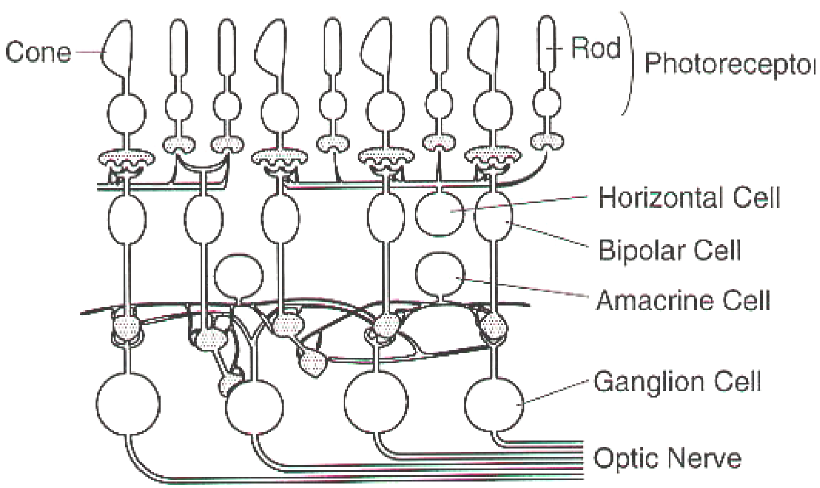
T. Ono, M. Koyanagi *et al.*, IEEE COOL Chips (2002)

# SEM Cross-Sectional View of 3-D Microprocessor Chip Fabricated by Wafer-to-Wafer Bonding

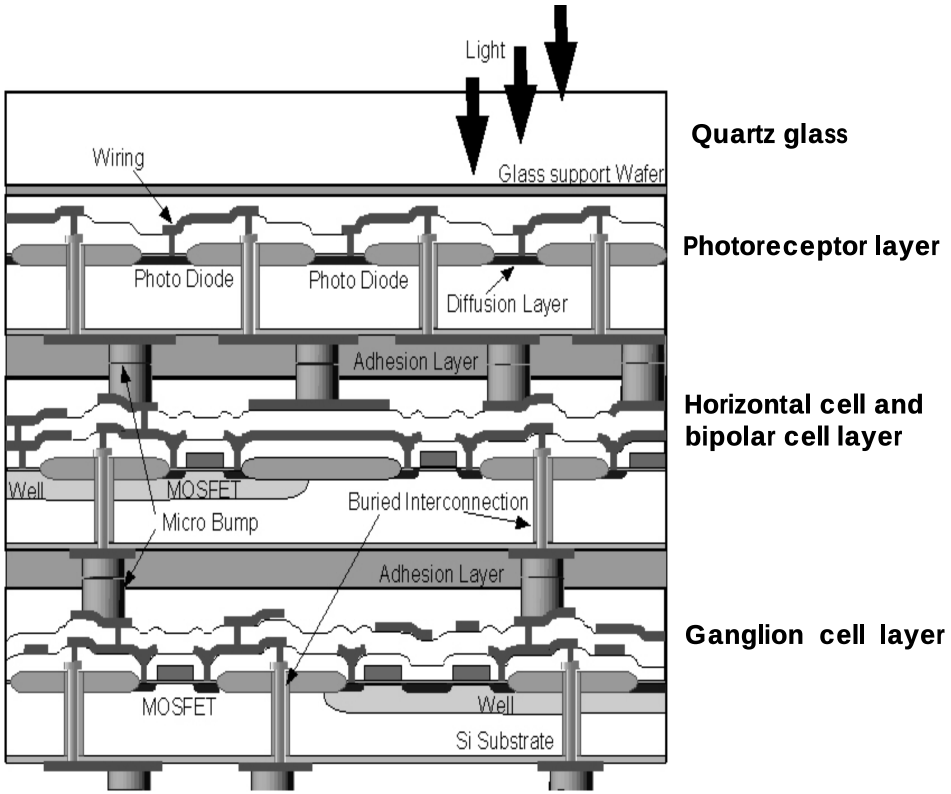


# Cross-Sectional Structures of Human Retina and 3D Artificial Retina Chip

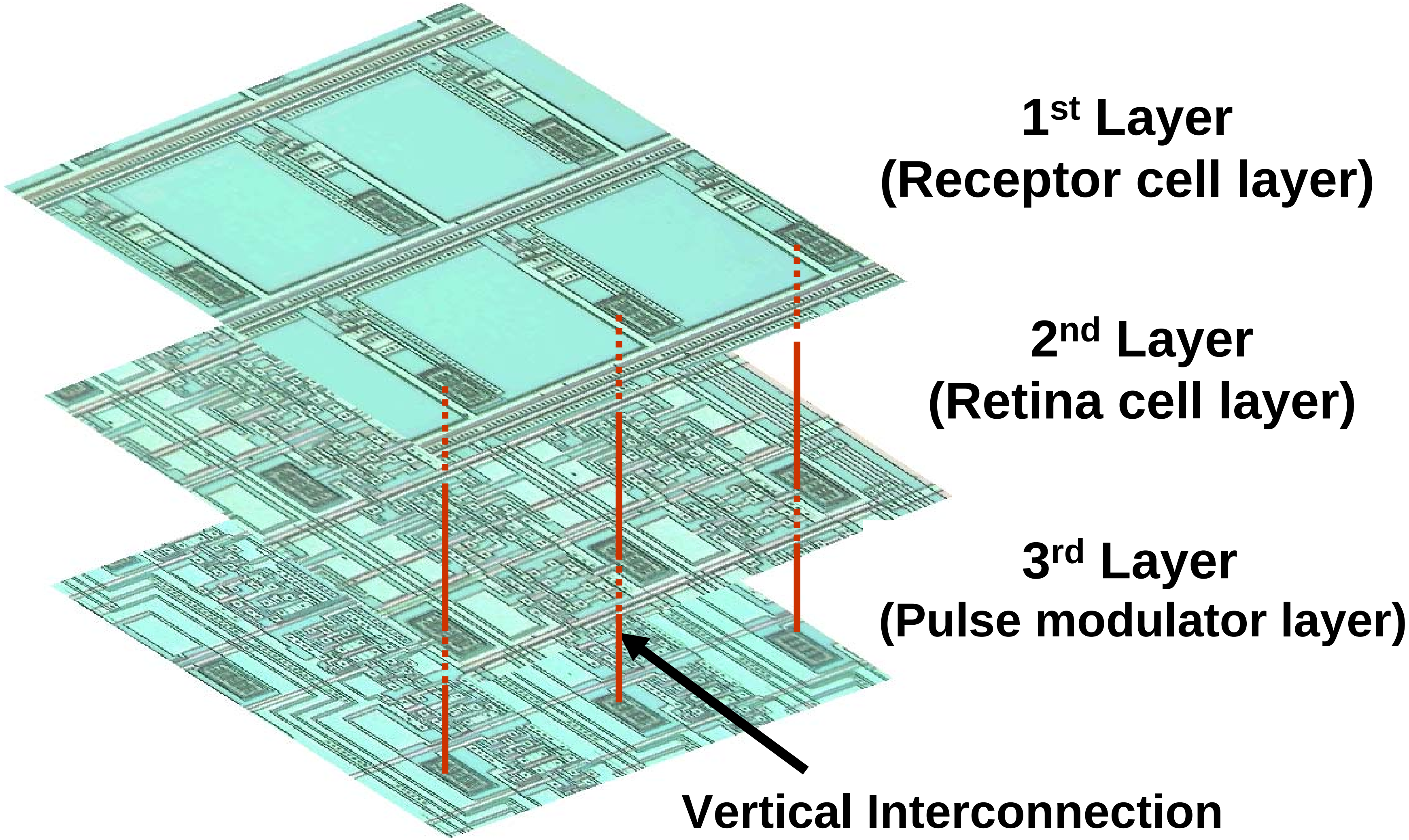



(a) human retina



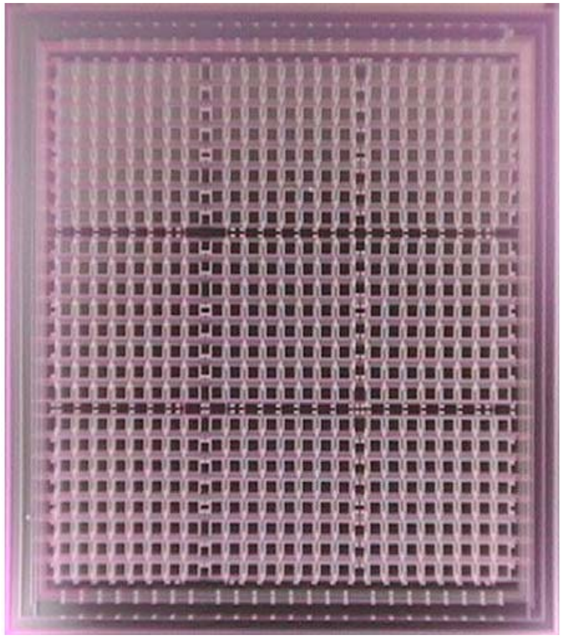

(b) 3D retina chip

# Photograph of 3D Artificial Retina Chip

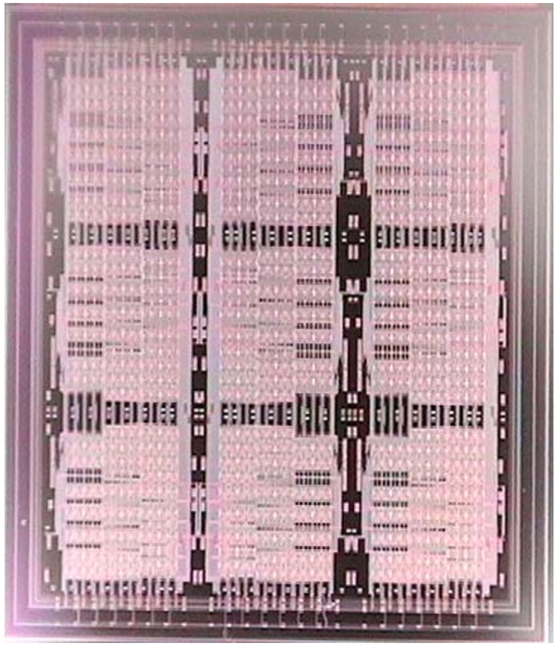


# Photograph of Respective Chip in 3D Stacked Image Sensor Chip with Three Stacked Layers

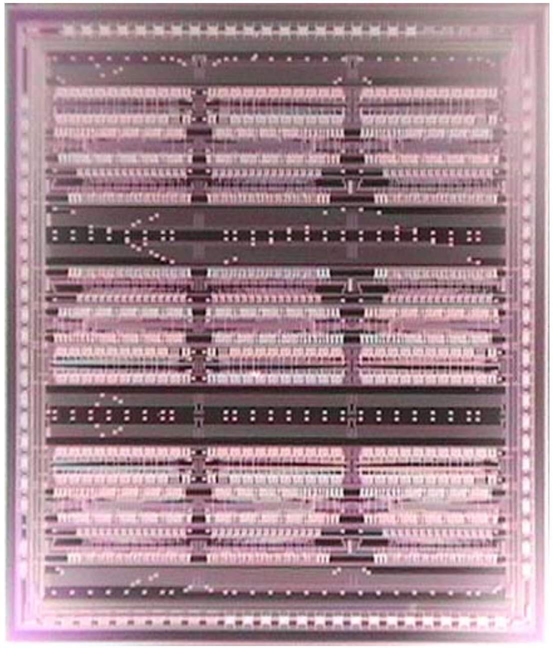
**1st Layer (Photosensor circuit)**



**2nd Layer (Register circuit)**

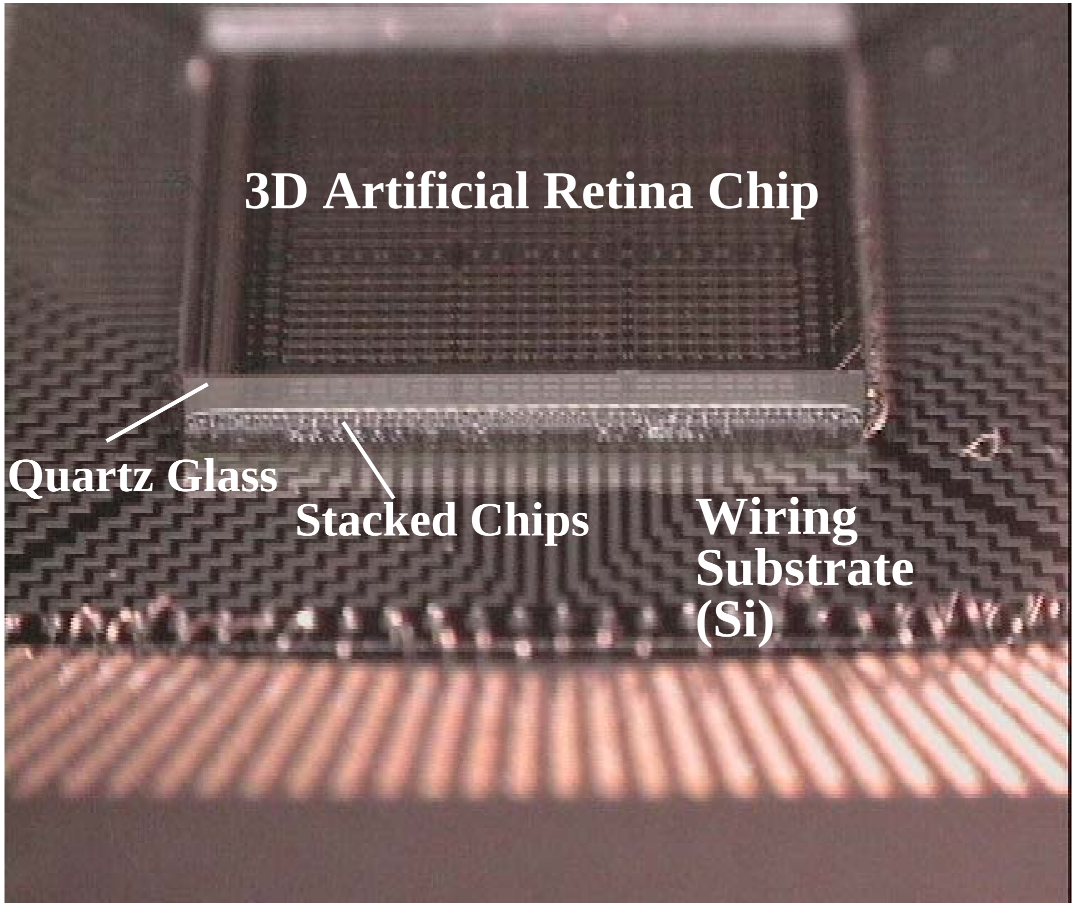


**3rd Layer (ADC & ALU circuit)**



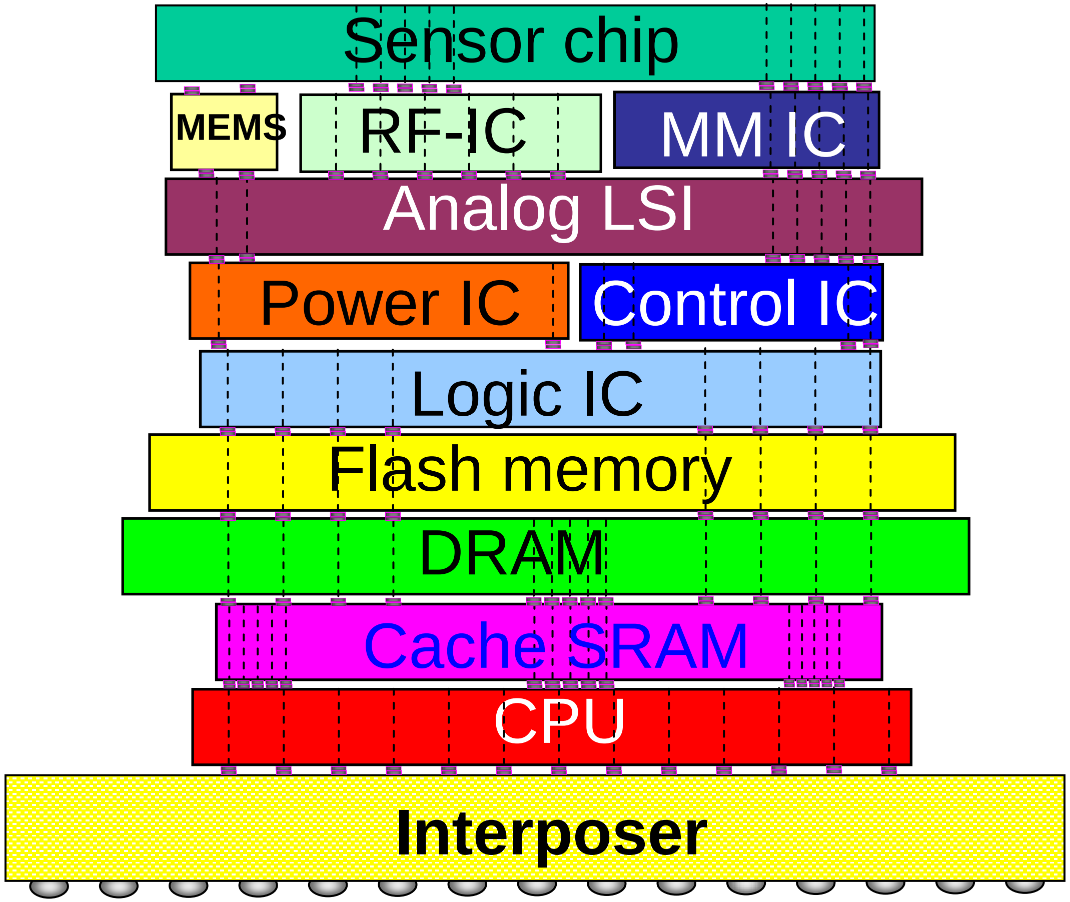
**( Chip size : 6 mm x 6 mm, 112 pins )**

# Photomicrograph of 3D Artificial Retina Chip



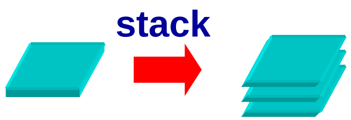
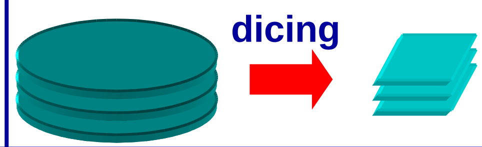

  

# Configuration of 3D Super Chip




Tohoku Univ. / ZyCube

# Current 3D-LSI stack approaches

| | COC (chip on chip) | COW (chip on wafer) | WOW (wafer on wafer) |
|---|---|---|---|
| |   |   |   |
| **Process cost** | **High** | **High~Middle** | **Low** |
| **Stack chips with different chip size** | **Easy** | **Easy** | **Impossible** |
| **Chip alignment accuracy <0.2μm (3σ)** | **Difficult from economical stand point** | | **possible ?** |
| **Miscellaneous** | | | **Need high yield wafers** |

➡ ***Need a high speed COW technology with the high alignment accuracy and the practical process cost***

# High speed and high accuracy Chip Alignment

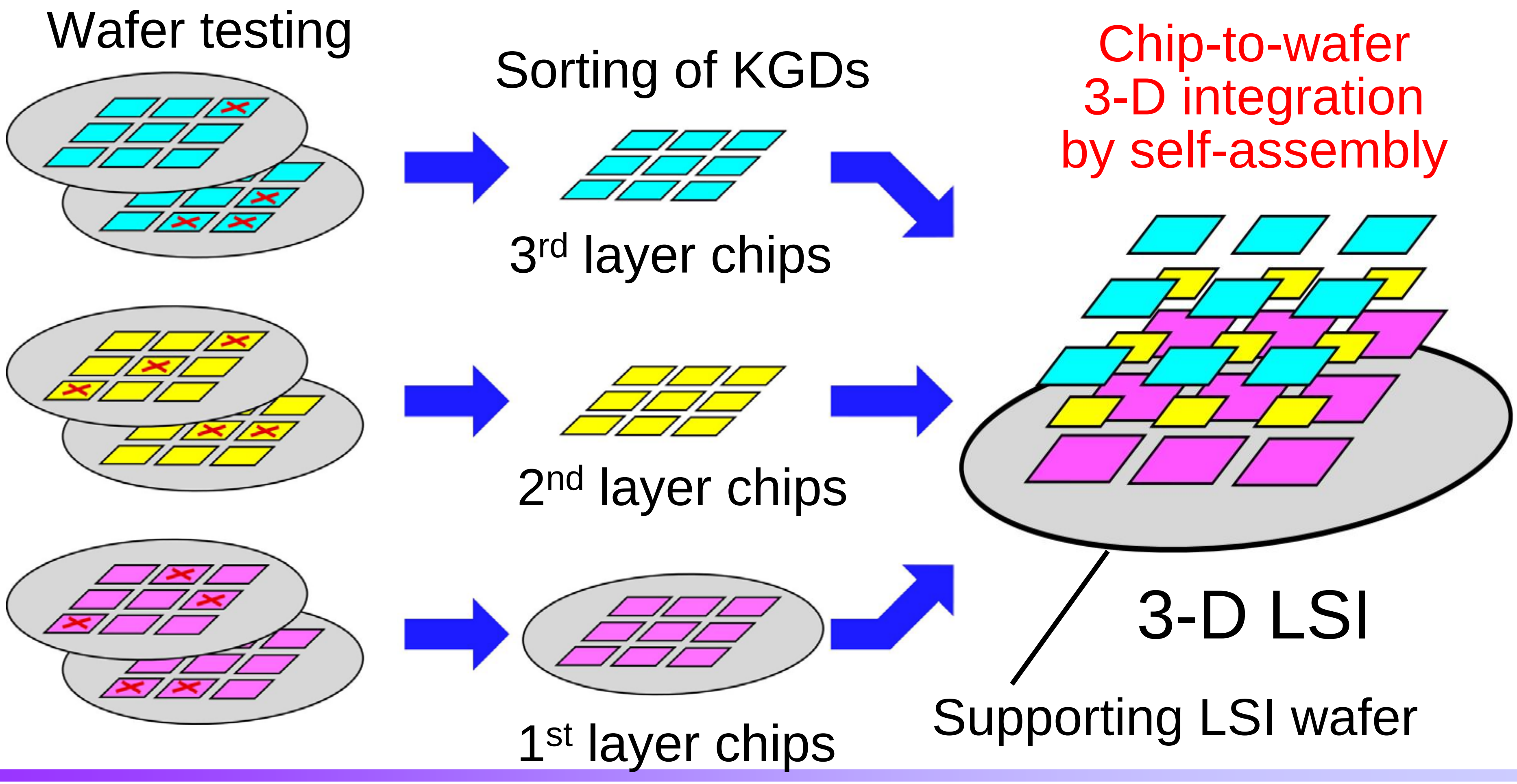
**Requirement**

| | |
|---|---|
| **Alignment Error** | **< 0.2um** |
| **TAT (turn around time)** | **~ wafer process** |

***In order to reduce cost, short process time (batch process) is indispensable***

# 3-D Technology Based on New Chip-to-Wafer Bonding in Tohoku University : Super-Chip Integration

**Batch alignment** | **Chip Self-Assembly**



# 3D-LSI Process Selection *--Which is best ?--*

| TSV process / Conductor Mat. — Stack Approach | | Via first: Before MOS (Poly-Si) | Via first: FEOL (After MOS) (Poly-Si, W) | Via last: after BEOL before Stack (W, Cu, etc) | Via last: after Stack (W, Cu, etc) | Process cost | Chip Stack with different chip size |
|---|---|---|---|---|---|---|---|
| WoW | Bulk | Tohoku Univ. (ZyCube)<br>IBM<br>Dalsa | TSMC<br>Tezzaron<br>RPI<br>Ziptronix<br>Chartered Semi. | Tohoku.U<br>ZyCube<br>Toshiba<br>Samsung<br>IMEC | Ziptronix<br>Albany NanoTech<br>IMEC<br>Samsung<br>••••••••••• | Low | Impossible |
| | SOI | | | Tohoku.U | IBM<br>MIT(Lincoln Lab.)<br>RPI | | |
| CoW w/ self-assembly technique | | Tohoku U. | | Frounhofer IZM<br>ZyCube/Tohoku U.<br>Samsung<br>CEA-LETI<br>Ziptronix<br>IMEC ••••••••••• | | Low | Easy |
| CoC | | Tohoku U.<br>Elpida | | ZyCube<br>ASET<br>Intel, Infineon, IMEC,<br>Samsung, Toshiba,<br>Fujitsu<br>Renesas ,NEDO | <Sidewall connection><br>TESSERA<br>3Dplus<br>VCI | High | Easy |
| Stack in wafer process | | NAND Memory | TFT-NAND（Samsung）<br>BiCS-NAND(Toshiba) | | | | |

# Summary

1. The Current & future 3D-LSI technologies with TSV were described.

2. Advantages of 3D-LSIs are
    - (a) Increase of electrical performances
    - (b) Increase of circuit density
    - (c) New Architecture (Hyper-parallel processing, Multifunction, etc)
    - (d) Heterogeneous integration
    - (e) Cost reduction

3. Many 3D-Integration approach have been reported. Considering supply chain of the base LSIs and variety of application, it is difficult to unify.

4. The CSP for 1.3M pixel CMOS image sensor was successfully fabricated without performances degradation.

5. By connecting the back illuminated type CMOS image sensor to Logic LSI, a high speed Pixel detector system with 100% fill factor will be realize.

3. In order to enter mass market for 3D-LSI, suppressing a rise in price of chip stack is essential. In this standpoint, for realizing 3D-Super chip, the high speed and high accurate CoW will be indispensable.