Monolithic Pixel Detector with SOI technology
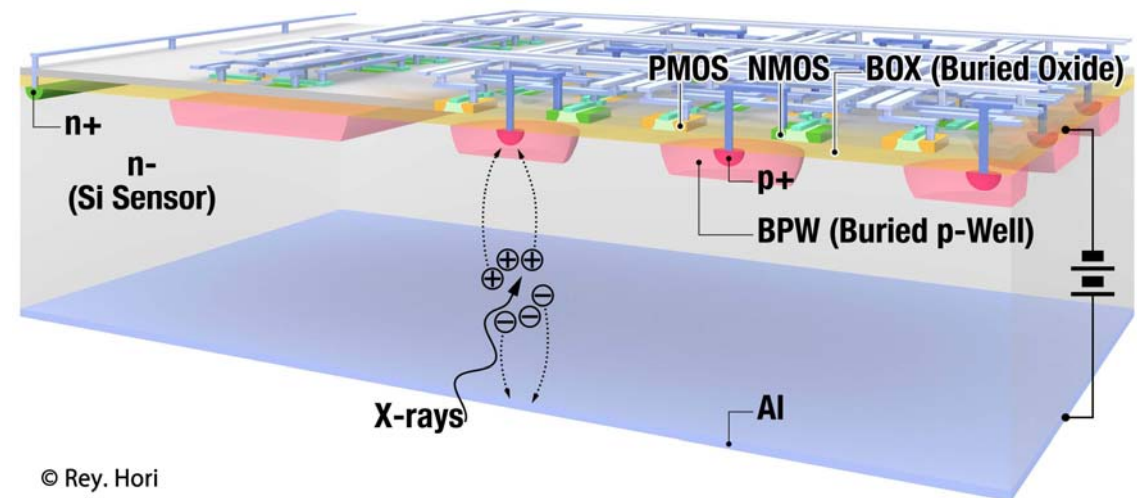
July. 1, 2011
@AGH Krakow
Yasuo Arai, KEK
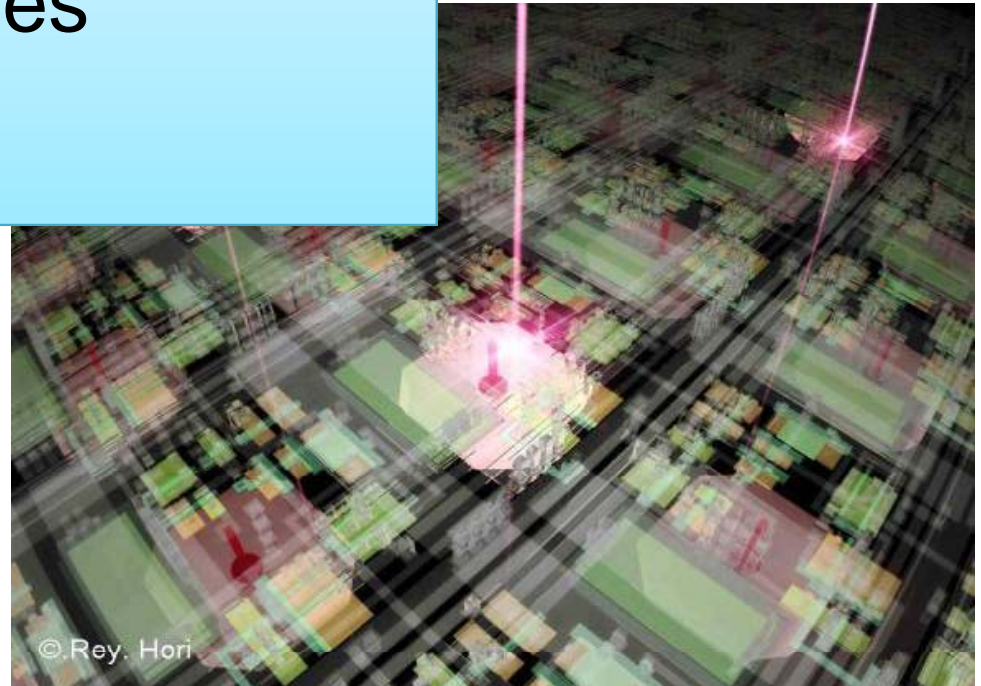yasuo.arai@kek.jp
http://rd.kek.jp/project/soi/

© Rey. Hori

OUTLINE

- Introduction of SOI Pixel Project

- SOI Detectors

- Developing Techniques

- Summary

©.Rey. Hori

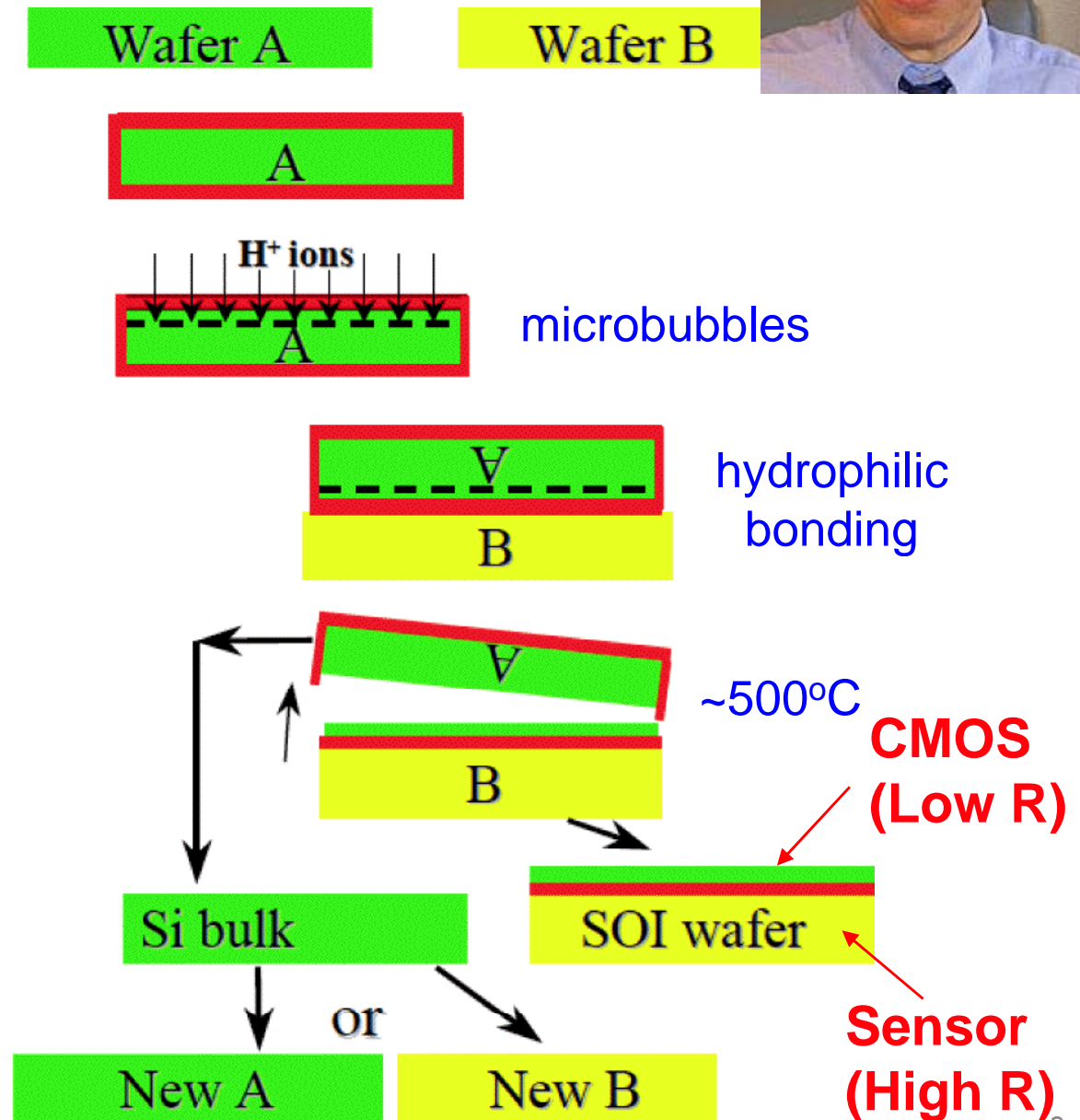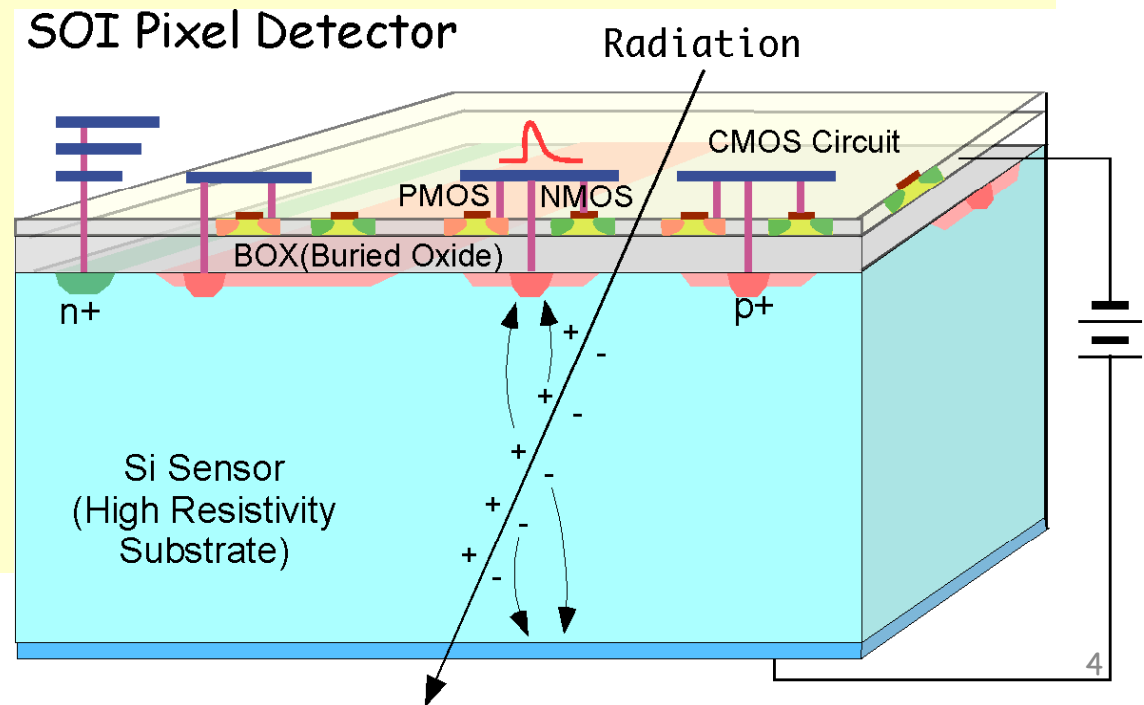# SOI Wafer (UNIBOND™)
(1995, LETI -> SOITEC)

① Initial silicon wafers A & B

② Oxidation of wafer A to create insulating layer

③ Smart Cut ion implantation induces formation of an in-depth weakened layer

④ Cleaning & bonding wafer A to the handle substrate, wafer B

⑤ Smart Cut - cleavage at the mean ion penetration depth splits off wafer A

⑥ Wafer B undergoes annealing, CMP and touch polish => SOI wafer complete

⑧ Split-off wafer A is recycled, becoming the new wafer A or B

Wafer A

Wafer B

A

H⁺ ions

A

microbubbles

A

B

hydrophilic bonding

A

B

~500°C

CMOS (Low R)

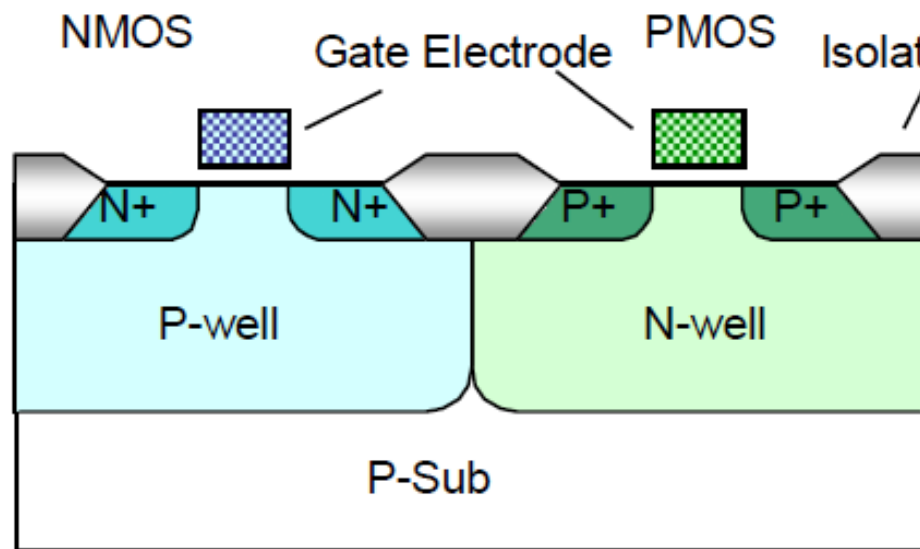Si bulk

SOI wafer

Sensor (High R)
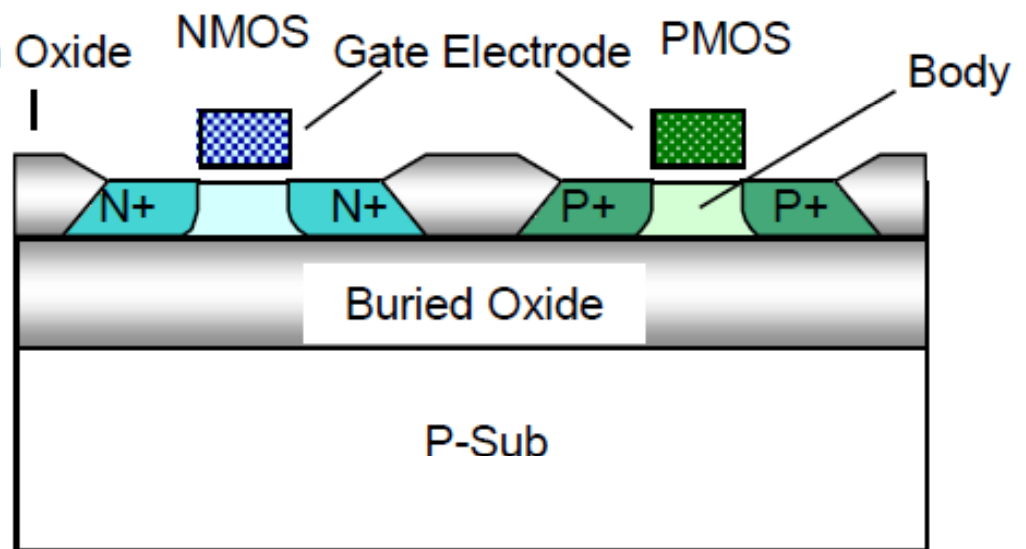
or

New A

New B

3

Features of SOI Pixel Detector

- Bonded wafer : High Resistivity (Sensor) + Low Resistivity (CMOS) .

- Truly Monolithic Detector (-> High Density, Low material, Thin Device).

- Standard CMOS can be used (-> Complex functions in a pixel).

- No mechanical bump bonding (-> High yield, Low cost).

- Fully depleted sensor with small capacitance of the sense node
  (~10fF, High conversion gain, Low noise)

- Based on Industrial standard technology (-> Cost benefit and Scalability)

- No Latch Up, Low SEE σ.

- Low Power

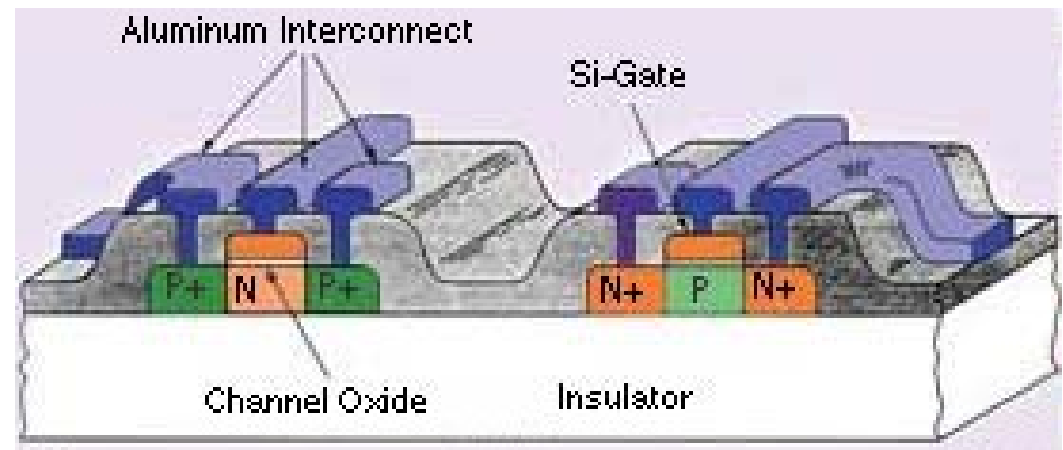- Operate in wide temperature (4K-570K(300°C)) range.

- ...

SOI Pixel Detector

Radiation

CMOS Circuit

PMOS NMOS

BOX(Buried Oxide)

n+   p+

Si Sensor
(High Resistivity
Substrate)

Bulk CMOS vs. SOI CMOS

Bulk CMOS

NMOS | Gate Electrode | PMOS | Isolation Oxide

N+ | N+ | P+ | P+

P-well | N-well

P-Sub

SOI CMOS

NMOS | Gate Electrode | PMOS | Body

N+ | N+ | P+ | P+

Buried Oxide

P-Sub
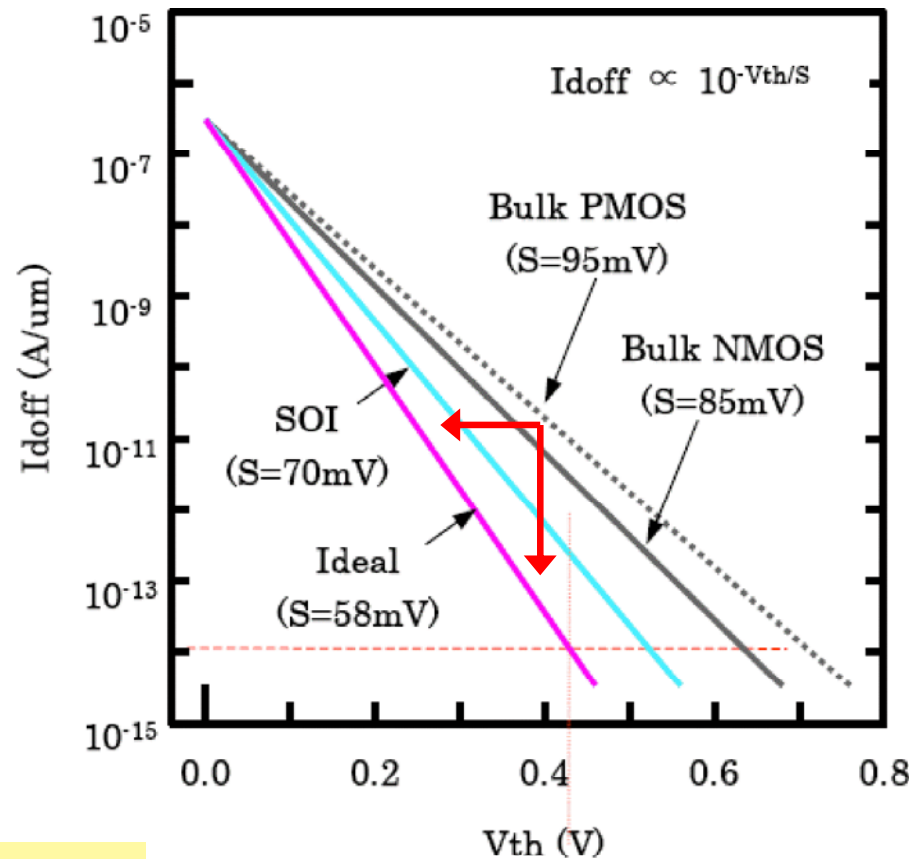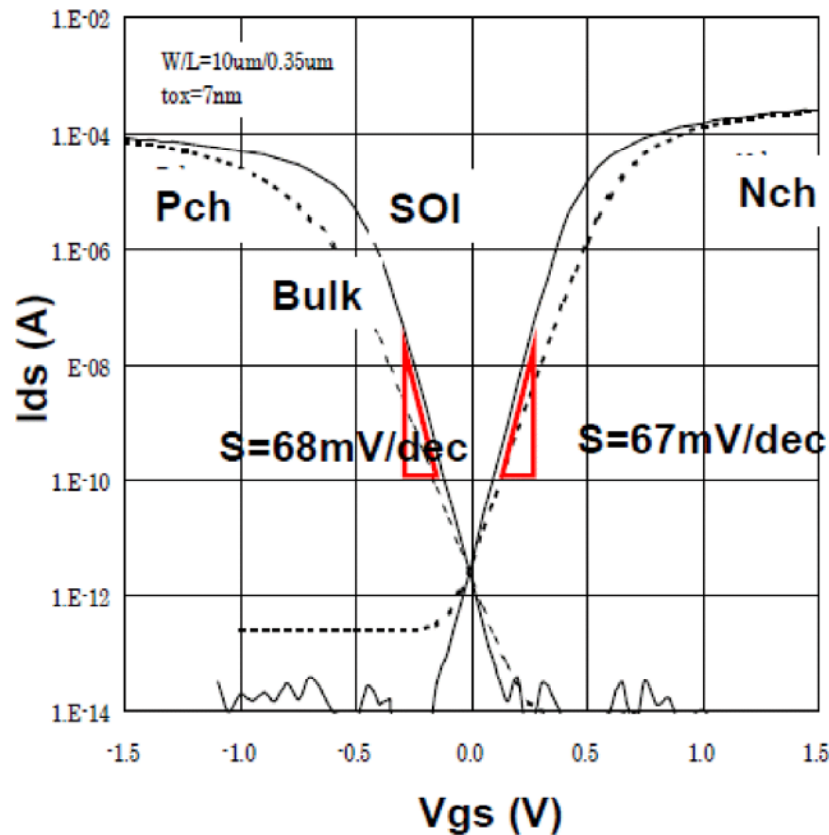
In SOI, Each Device is completely isolated by Oxide.

Aluminum Interconnect | Si-Gate

P+ | N | P+ | N+ | P | N+

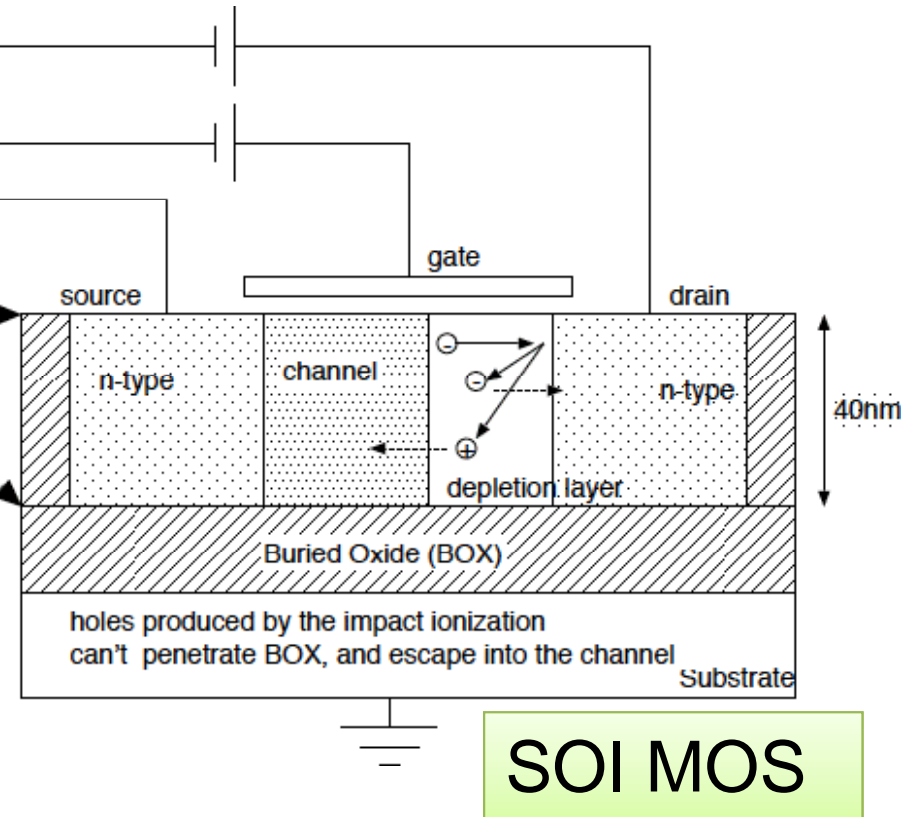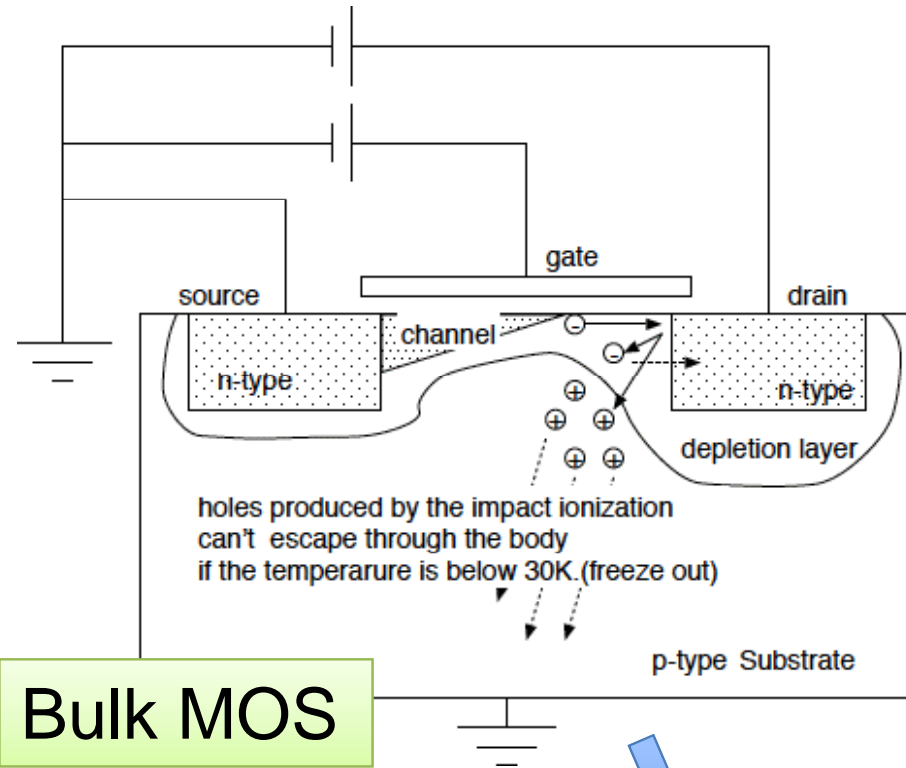Channel Oxide | Insulator

Steep Sub Threshold Slope

F.Ichikawa et al., SSDM, 2004

Gate voltage is not wasted to deplete the bulk.

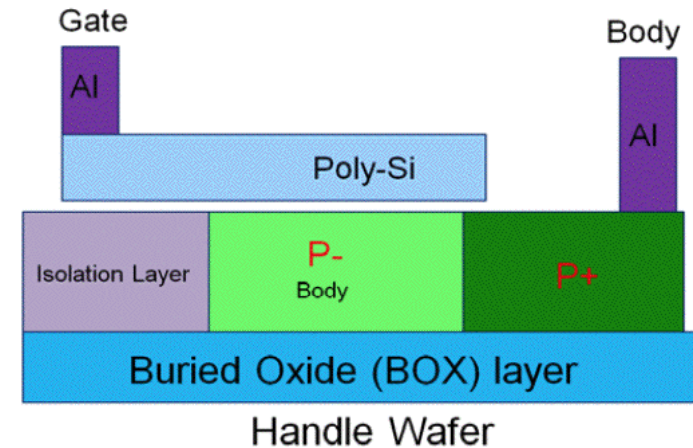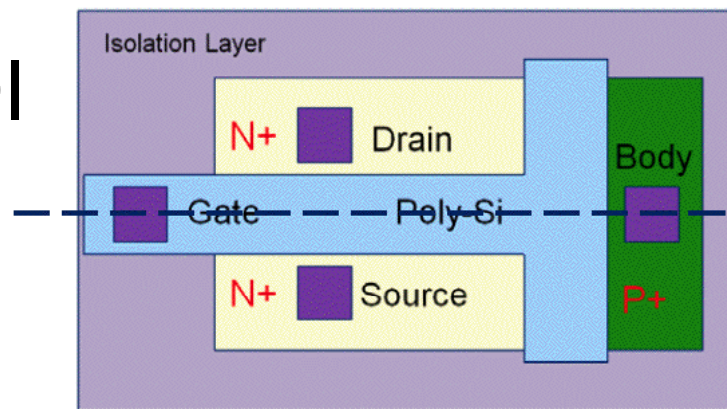Lower Threshold (Leakage Current) is possible without increasing Leakage Current (Vth).
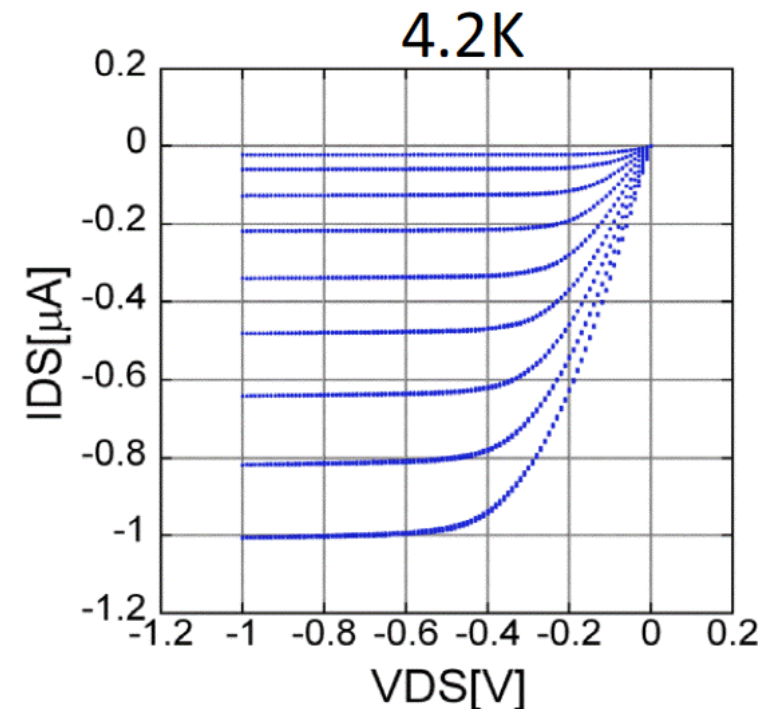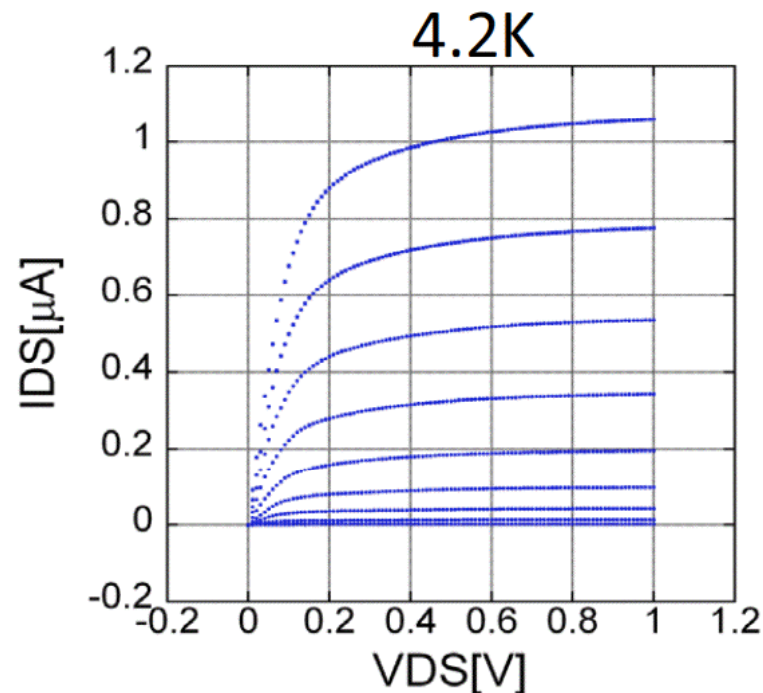
Operation at Cryogenic Temperature

Bulk MOS

holes produced by the impact ionization
can't escape through the body
if the temperarure is below 30K.(freeze out)

p-type Substrate

SOI MOS

holes produced by the impact ionization
can't penetrate BOX, and escape into the channel

Buried Oxide (BOX)

40nm

KINK

Hysterisis

4.2K

4.2K
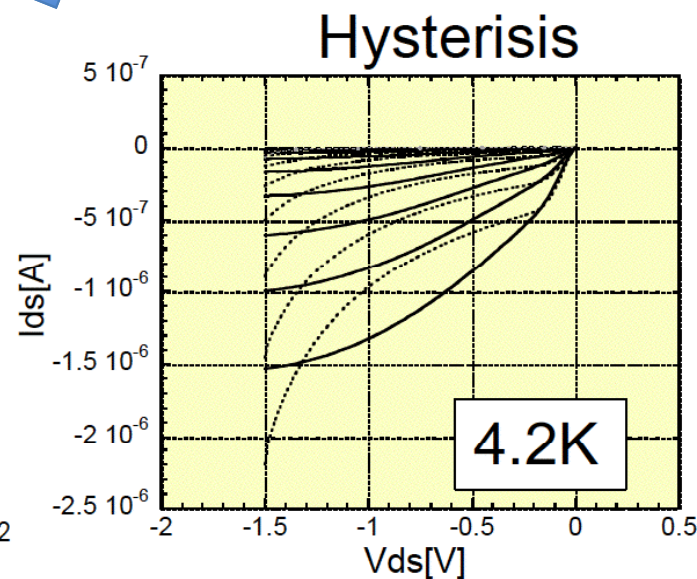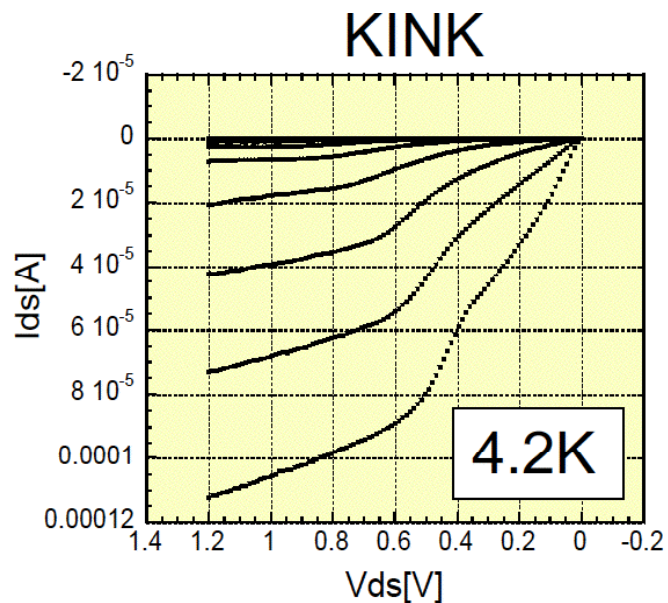
IV characteristics at cryogenic temperature
Body tie type

SOI

Body-tied W(μm)/L(μm)=0.5/10

The kink effects do not occur for |VDS|≤1.0V (L=10 μm)

SOI Pixel Project Brief History

'05. 4 : Proposed to KEK Detector Technology Project.
   (Generic R&D)

'05. 7 : Start Collaboration with OKI Semiconductor.

'05.10 : 1st Submission in VDEC 0.15 um MPW.

'06.12 : 1st (and last) 0.15 um KEK MPW run.
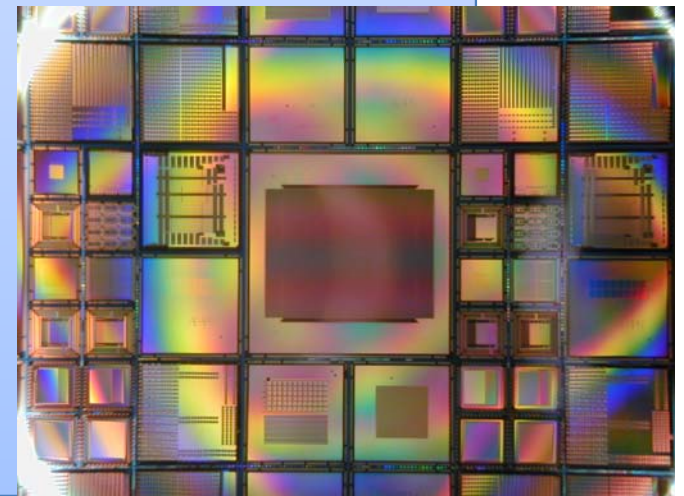
'07.3 : 0.15 um lab. process line was closed.

   → move to 0.2 um mass production line at Miyagi.
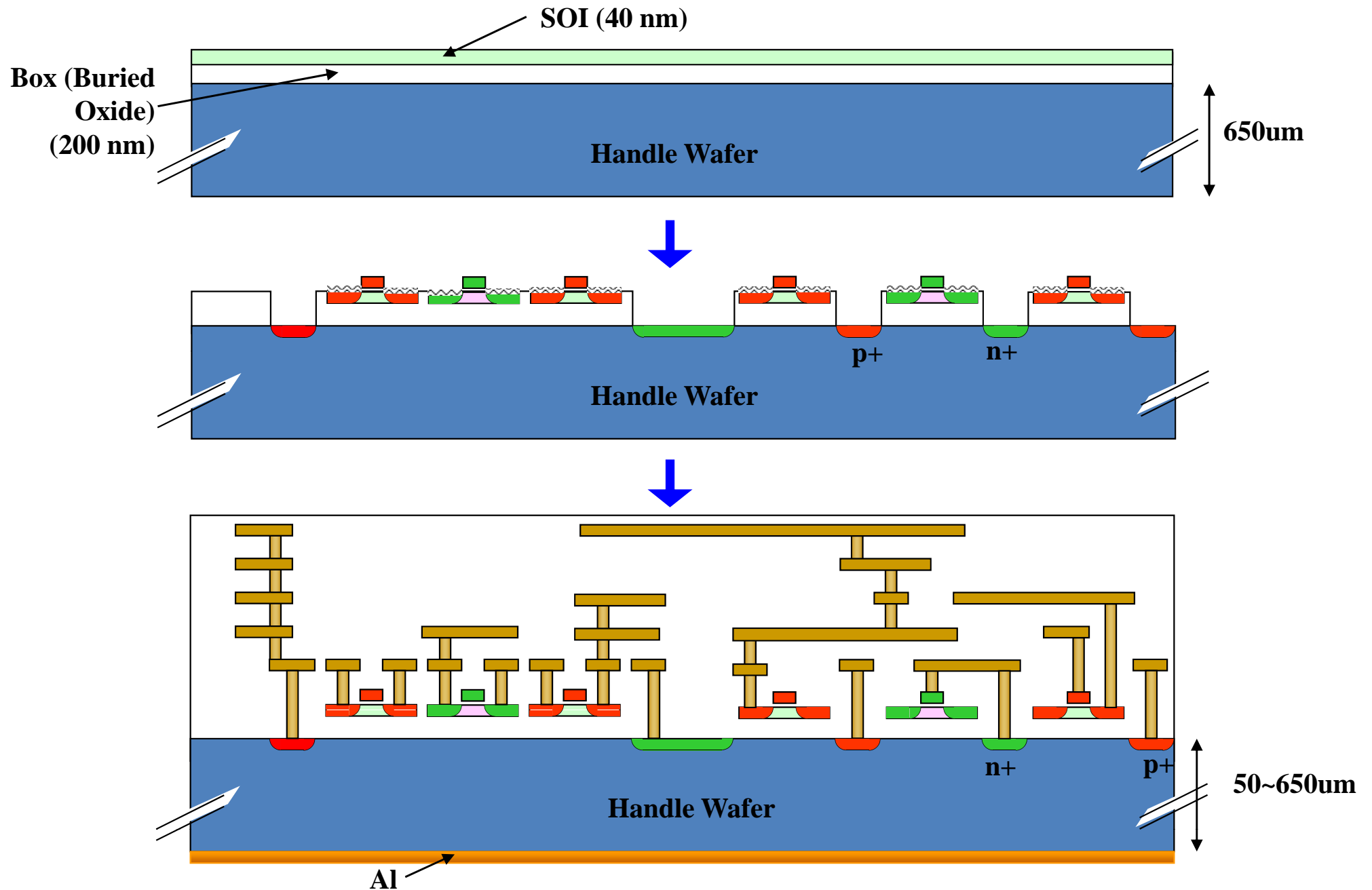
'08.1 : 1st 0.2 um KEK SOI-MPW run.

'08.10 : OKI is owned by ROHM Co. Ltd.
   (Lehman Shock)

      :

'11.1: 6th KEK SOI-MPW run

SOI Pixel Process Flow

SOI (40 nm)

Box (Buried Oxide) (200 nm)

Handle Wafer

650um

p+   n+

Handle Wafer

n+   p+

Handle Wafer

50~650um

Al

OKI semi/ROHM 0.2 μm FD-SOI Pixel Process

Process	0.2μm Low-Leakage Fully-Depleted SOI CMOS 1 Poly, 5 Metal layers. MIM Capacitor (1.5 fF/um^2), DMOS Core (I/O) Voltage = 1.8 (3.3) V
SOI wafer	Diameter: 200 mmϕ, 720 μm thick Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz (n) ~700 Ω-cm, FZ(n) ~7k Ω-cm, FZ(p) ~40 k Ω-cm
Backside process	Mechanical Grind, Chemical Etching, Back side Implant, Laser Annealing and Al plating

MPW (Multi Project Wafer) run

We are operating MPW runs Twice / year.
(Next MPW run is Oct. 3rd.)

Louvain-la-Neuve Univ.

U. of Hawaii

Riken

INP Krakow

FNAL

FNAL

IHEP China

LBNL

LBNL

U. Heidelberg

INTPIX 3C

CNTPIX5

U. Tohoku

CNTPIX4

Kyoto Univ.

JAXA/ISAS

INTPIX4

3D_L

KEK KEK MPI

3D_U

Krakow

Tsukuba Univ.

AIST

KEK JAXA

KEK KEK

SOI Pixel Detectors
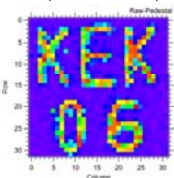
2006 — 0.64 mm — 32x32 — Vbias~10V
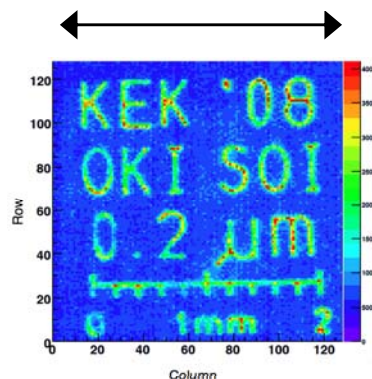
2008~9 — 2.56 mm — 128x128 — Vbias~100V

2010 — 13.8 mm — 832x512 — Vbias~250V
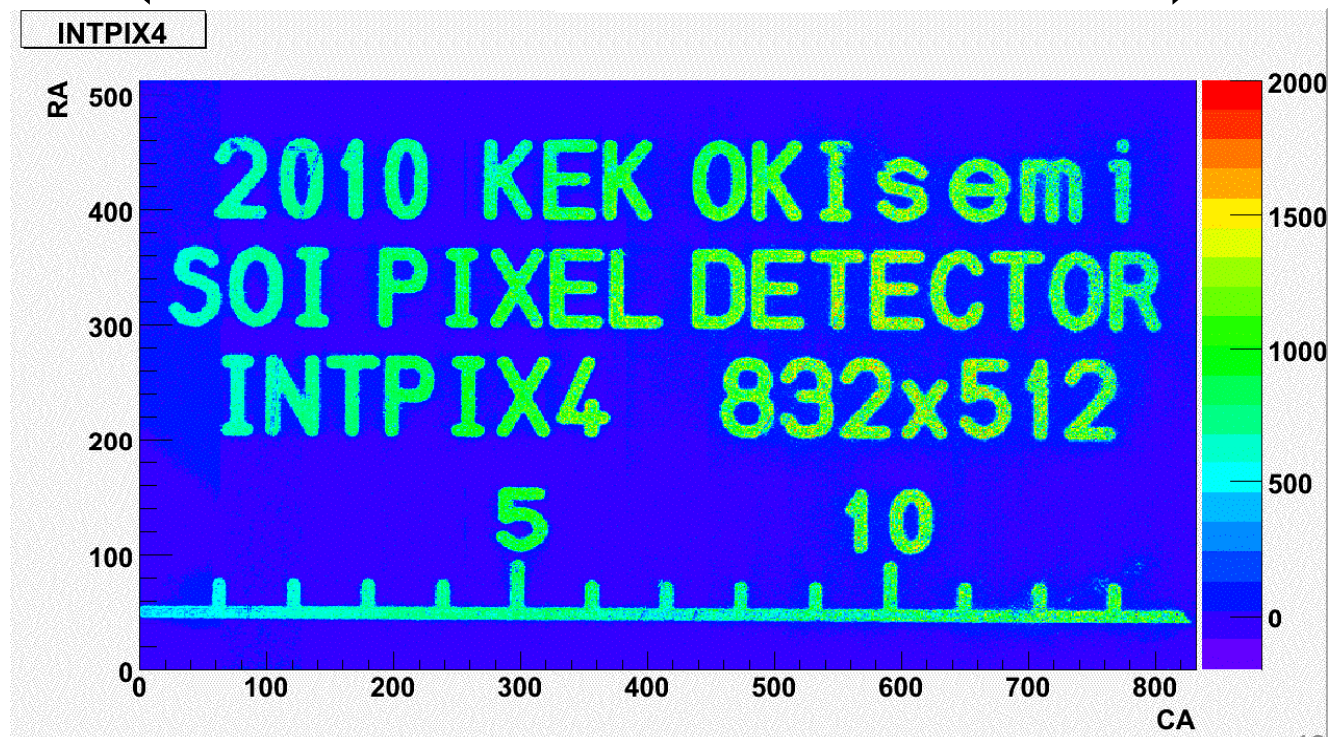
By the Way,
OKI Semi fab is located very near
to the Center of the Earthquake.

OKI Semiconductor
MIYAGI Co. Ltd.
&Tohoku Univ.

× 38° 6'12" N
142°51'36" E

T-Micro

KEK

JMA Seismic
Intensity

震度
(JMA Seismic Intensity)

7	
6+	
6-	
5+	
5-	
4	
3	
2	
1	

2011-03-11 14:46 (2011-03-11 05:46 UTC)
マグニチュード(Magnitude) 9.0
震源の深さ(Depth of hypocenter) 24km
出典(Source) : 気象庁(Japan Meteorological Agency)
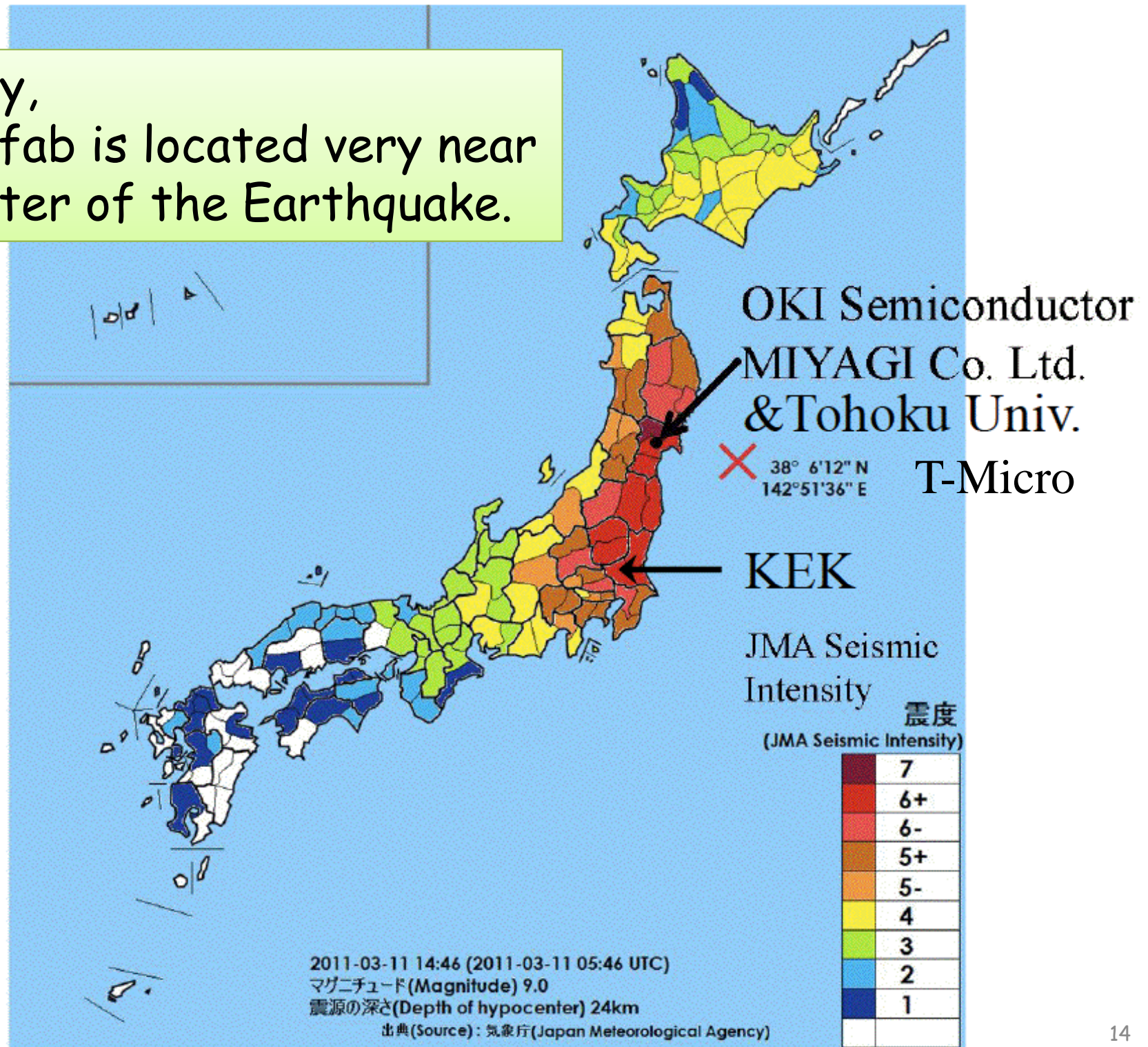
SOI Detectors

Integration Type Pixel (INTPIX)

$$V_{sense} = \frac{Q}{C} \approx \frac{0.6\,fC}{8\,fF} = 70mV$$

β線
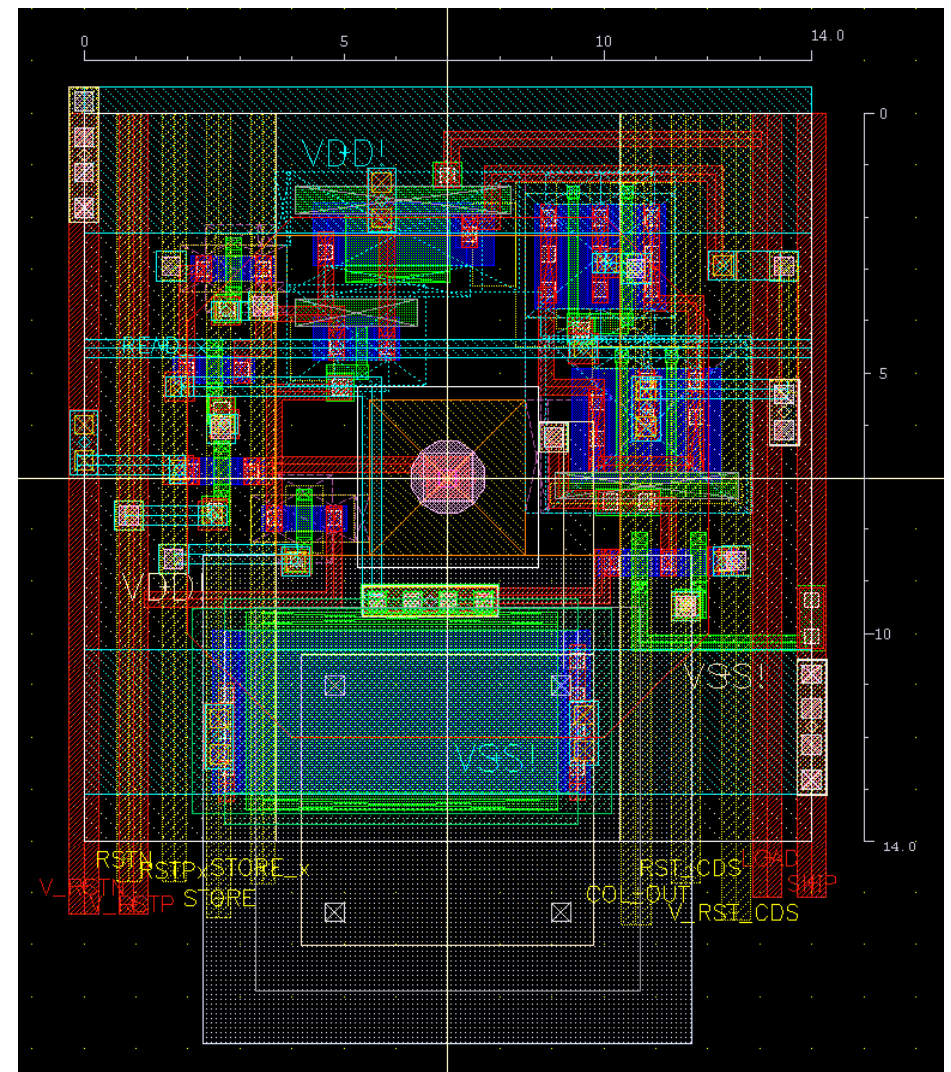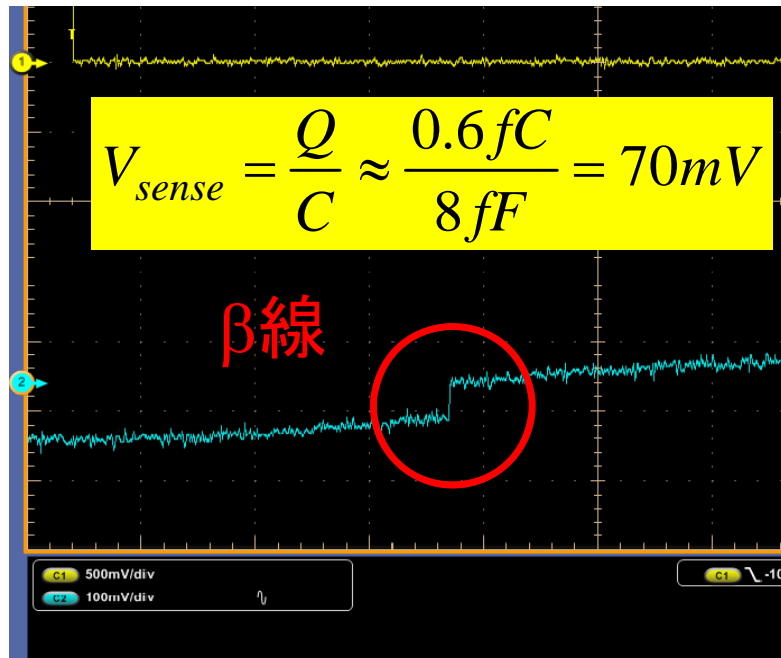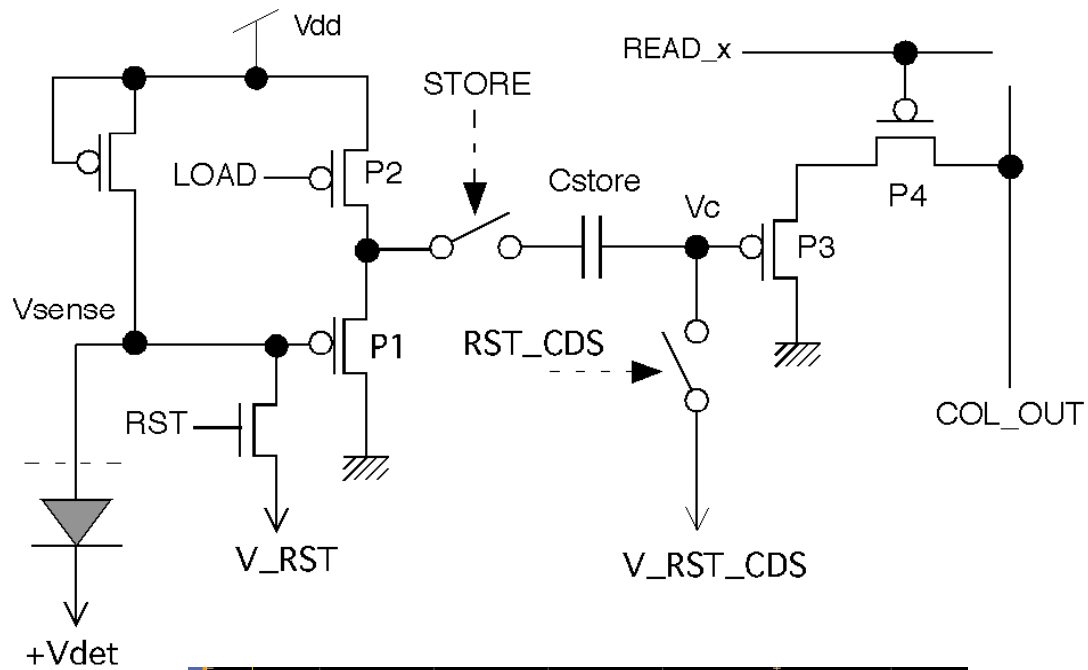
Size : 14 μm x 14 μm
with CDS circuit

Integration Type Pixel (INTPIX4)

15 mm

10 mm
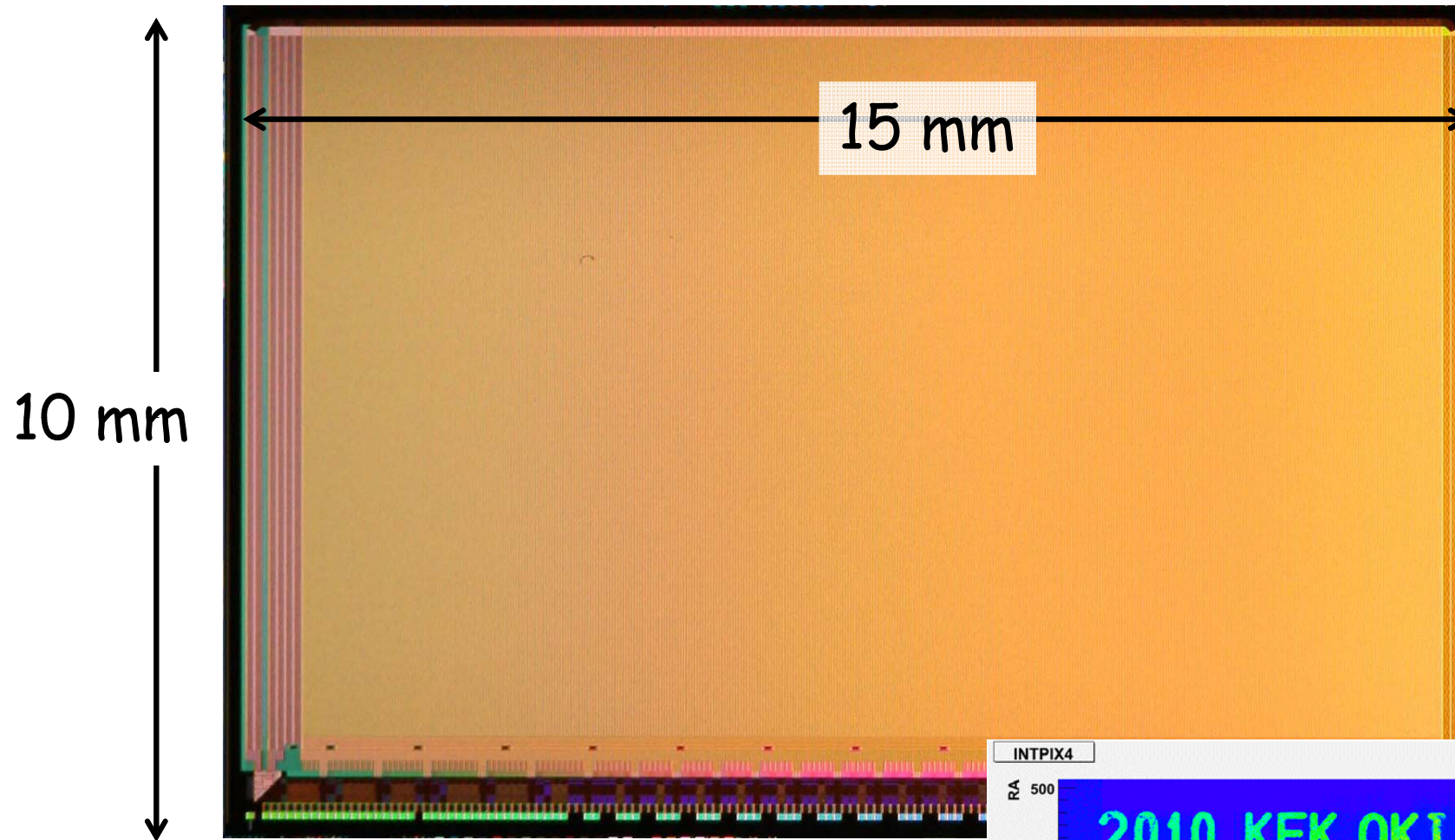
17x17 μm, 512x832 (~430k）
pixels、13 Analog Out、CDS
circuit in each pixel.

INTPIX4

2010 KEK OKIsemi
SOI PIXEL DETECTOR
INTPIX4   832x512

5   10
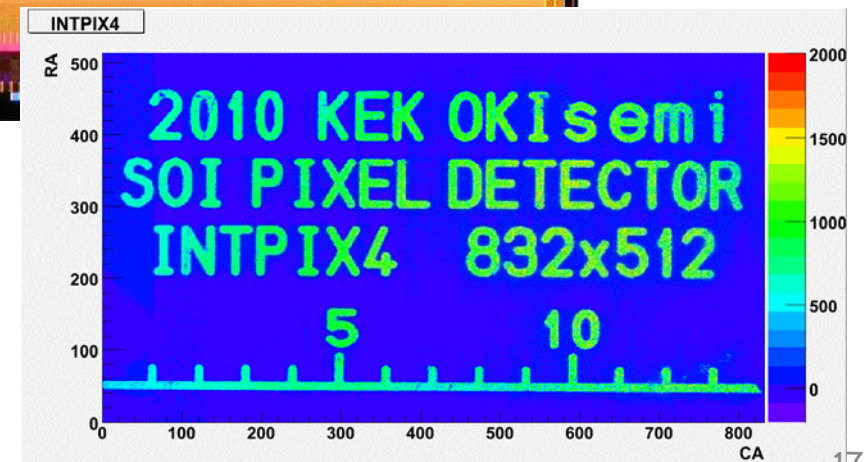
Data Acquisition Board

- Soi EvAluation BoArd with Sitcp(SEABAS)
- A FPGA controls the SOI Pixel chip
- Directly transferred to Ethernet

SEABAS

INTPIX4

USER FPGA

Data Transfer via Ethernet

ADC & DAC

300mm
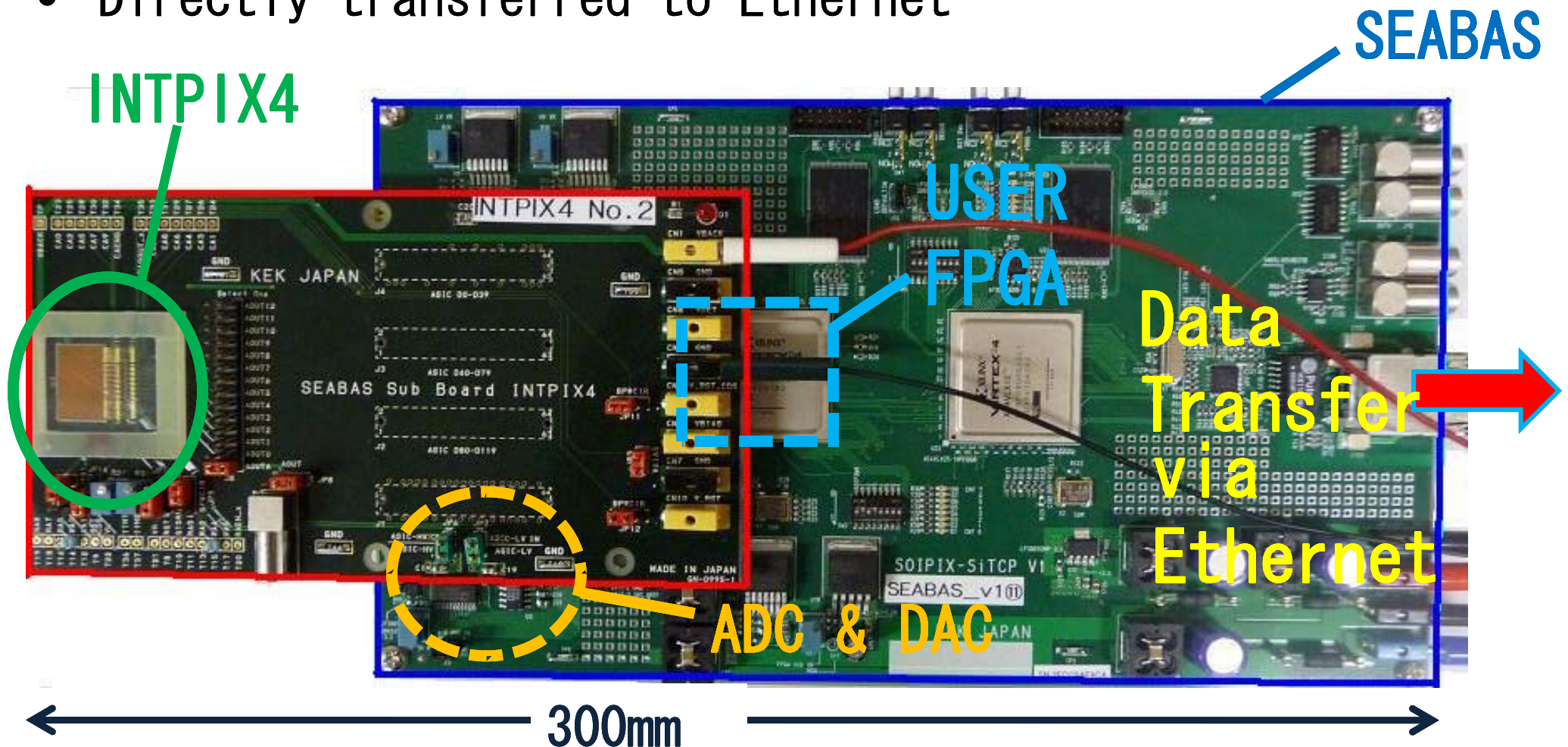
Spatial Resolution (Contrast Transfer Function)

- Comparison of contrasts with commercial X-ray devices.
  - SOI Pixel : INTPIX4, **F**lat **P**anel **S**ensor (FPS), CCD, and **I**maging **P**late (IP)

CTF [%] = B / A
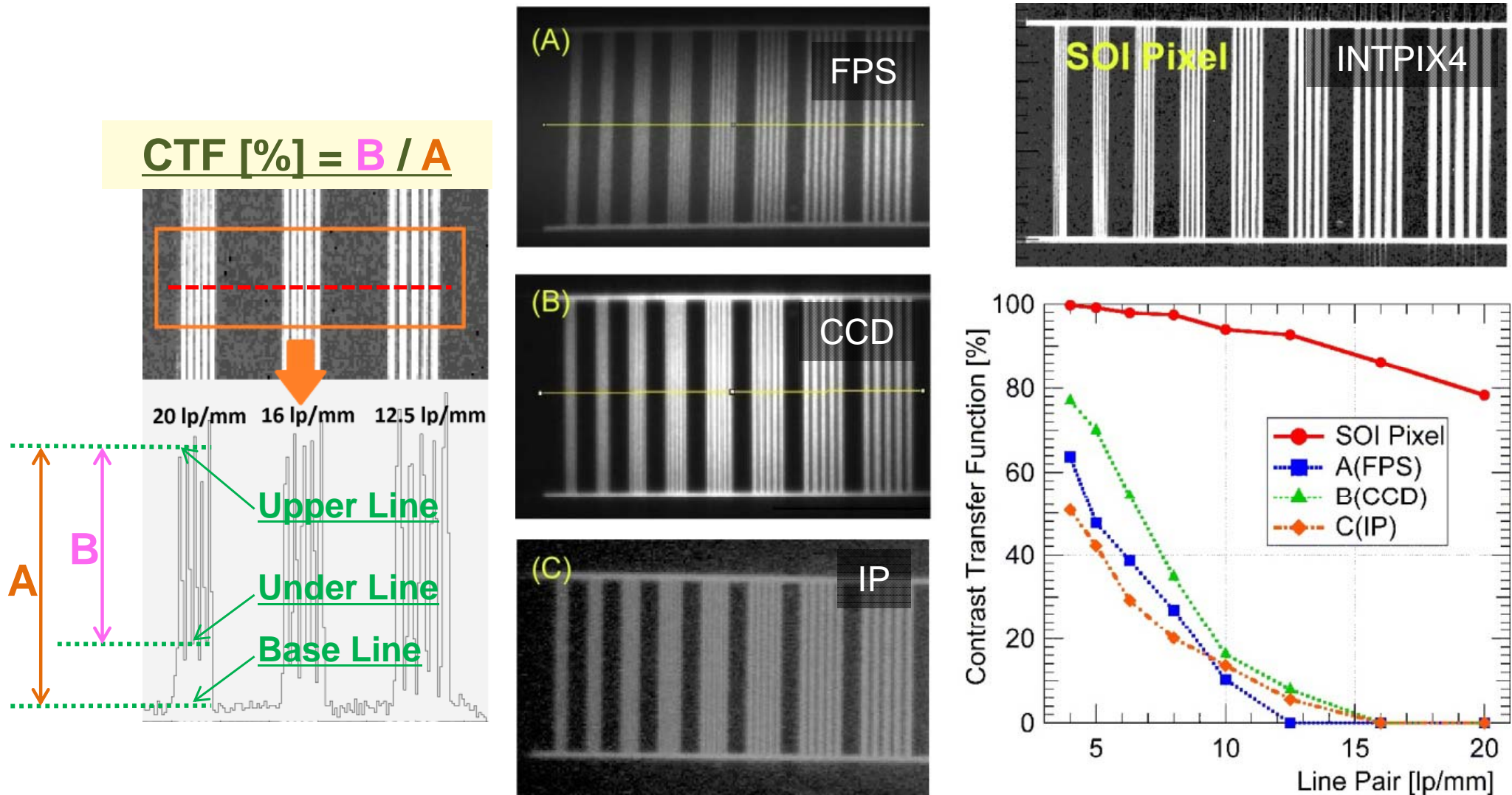
INTPIX4
Pixel Size : 17 um x 17 um
No. of Pixel : 512 x 832 (= 425,984)
Chip Size : 10.3 mm x 15.5 mm
Vsensor=200V, 250us Int. x 500
X-ray Tube : Mo, 20kV, 5mA

Fine resolution & High Contrast

5mm
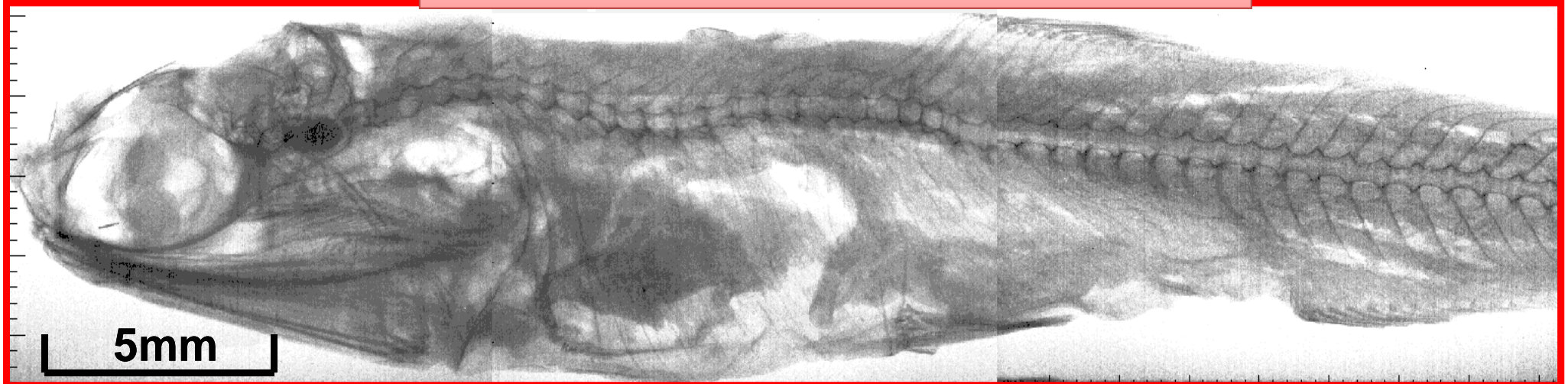
X-ray Image of a small dried sardine taken by
a INTPIX4 sensor (3 images are combined).

(A. Takeda)

CERN SPS
200GeV/C π^- beam

Second Plane
Vbias=70V

$\sigma \sim 1.2 \ \mu m$

LBNL & Padove

NIM A, M. Battaglia et al.,
http://dx.doi.org/10.1016/j.nima.2011.05.081

22
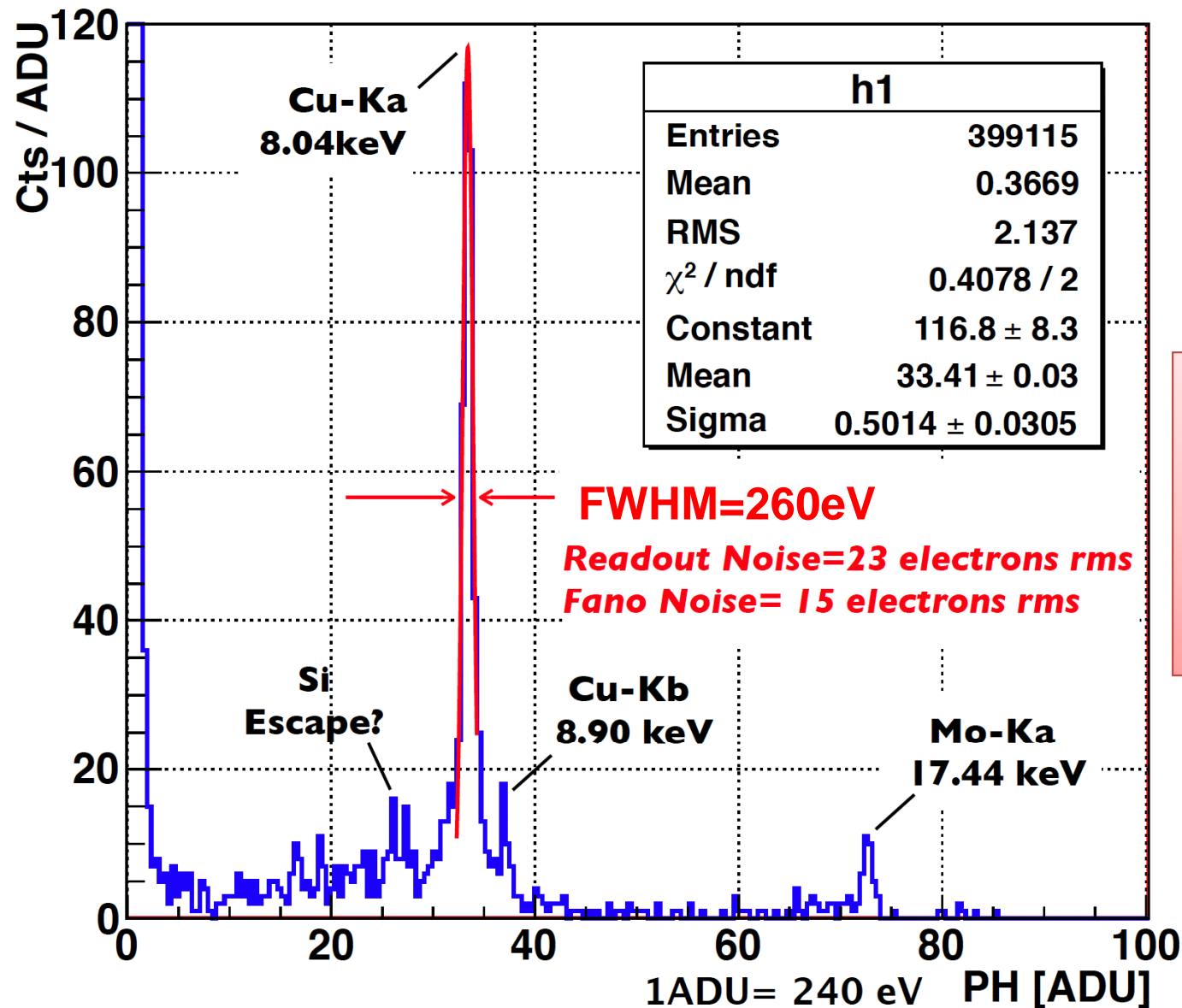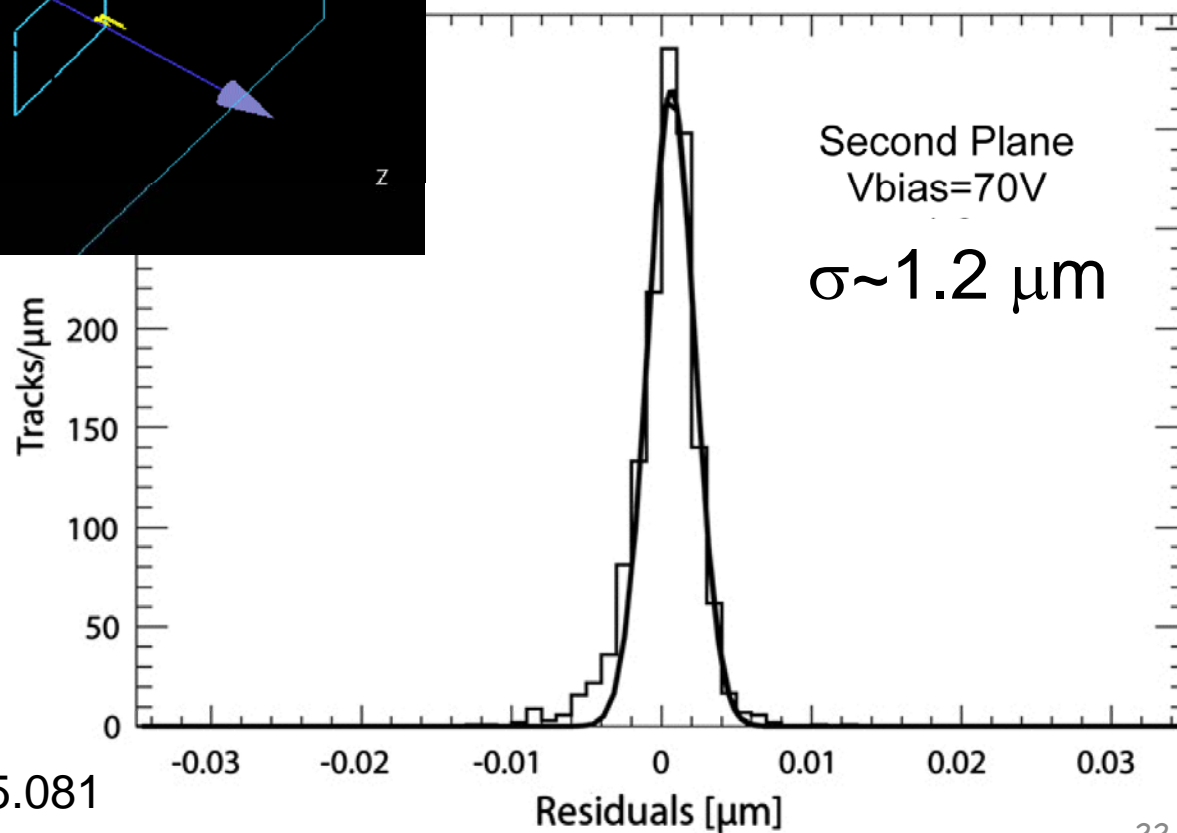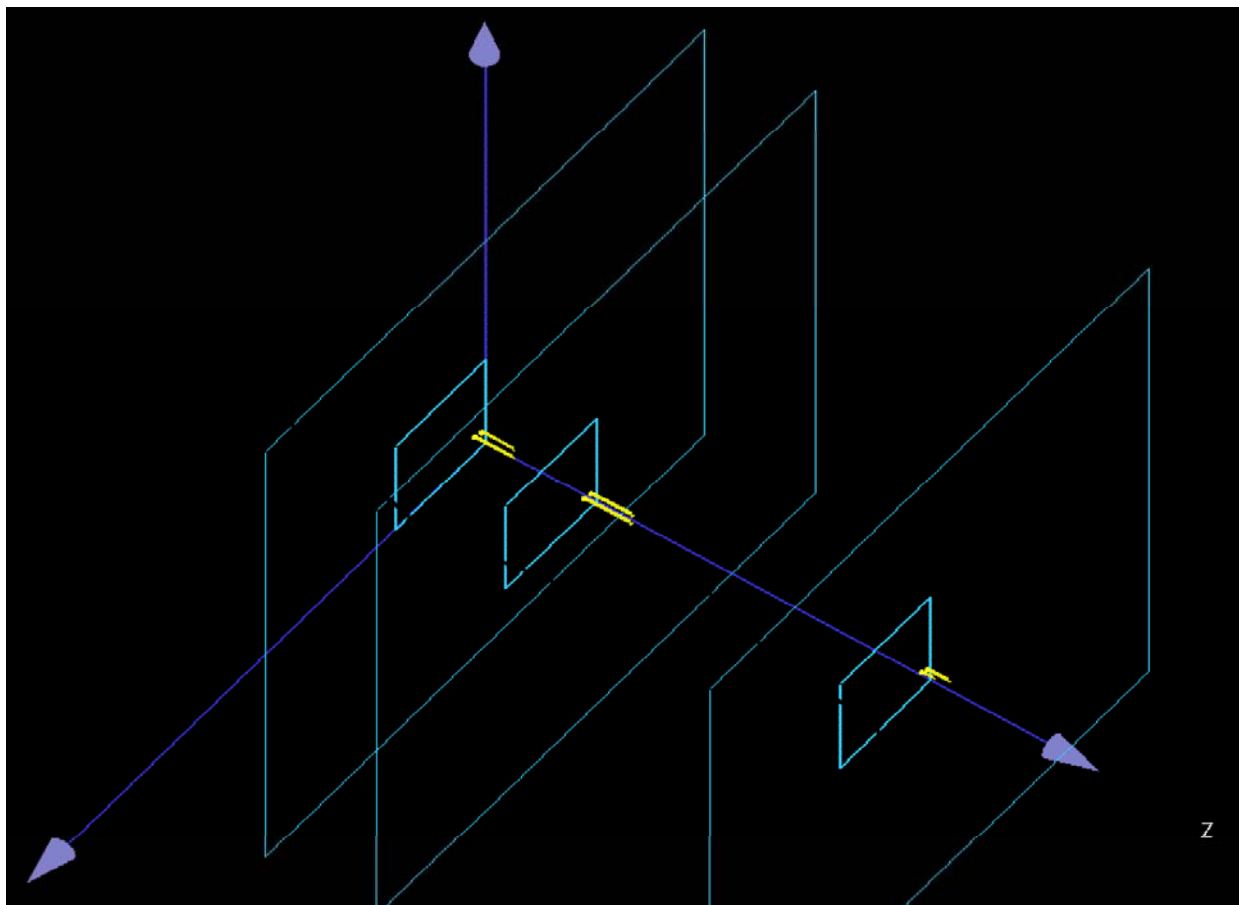
e+ Beam Test at Tohoku Univ.

SOI beam test 2010 collaboration

e+ Beam ~673MeV/c

L3 y residual distribution

3rd layer y	
Entries	5473
Mean	0.0002858
RMS	0.007503
Prob	0
Constant	1293 ± 28.2
Mean	0.000395 ± 0.000045
Sigma	0.002921 ± 0.000047

$\sigma \sim 2.9\ \mu m$
(incl. multiple scattering)

XY-stage

photomultiplier tube for timing trigger

SEABAS(R/O) board

CNTPIX sub board

INTPIX sub board

Beam (positron)
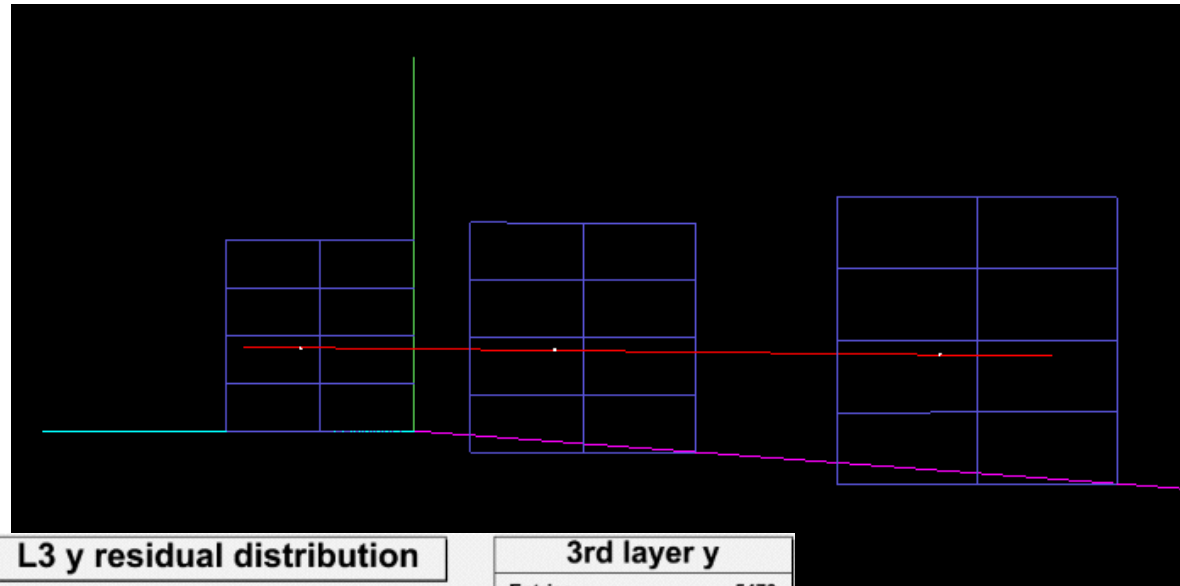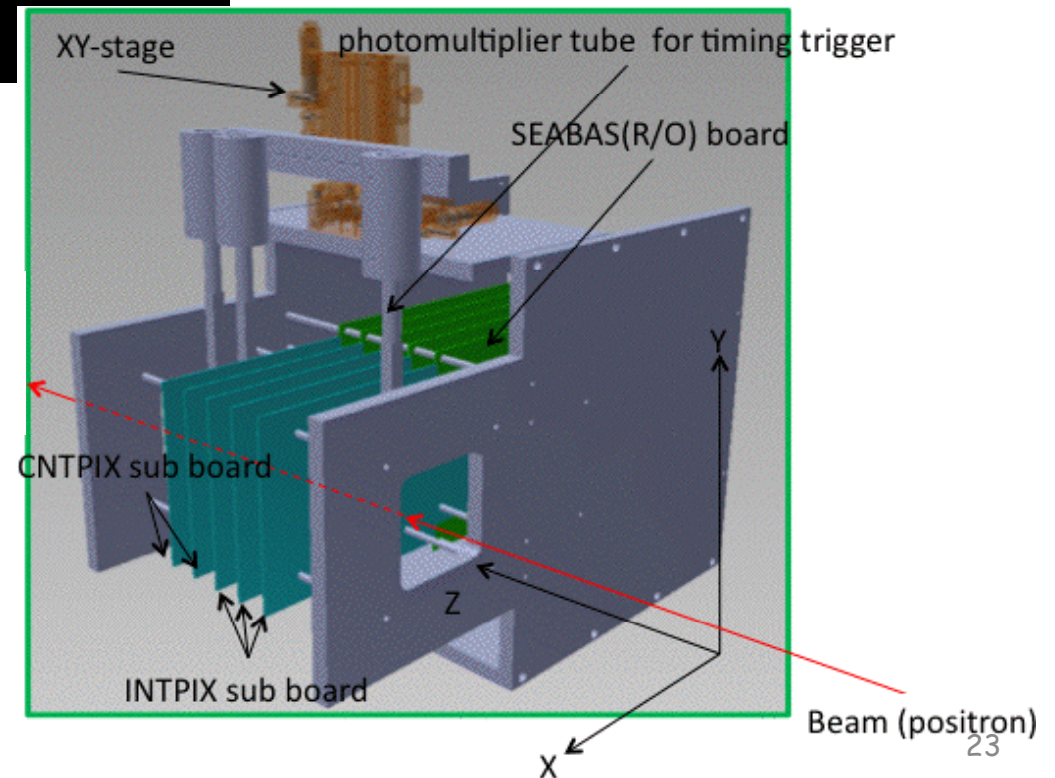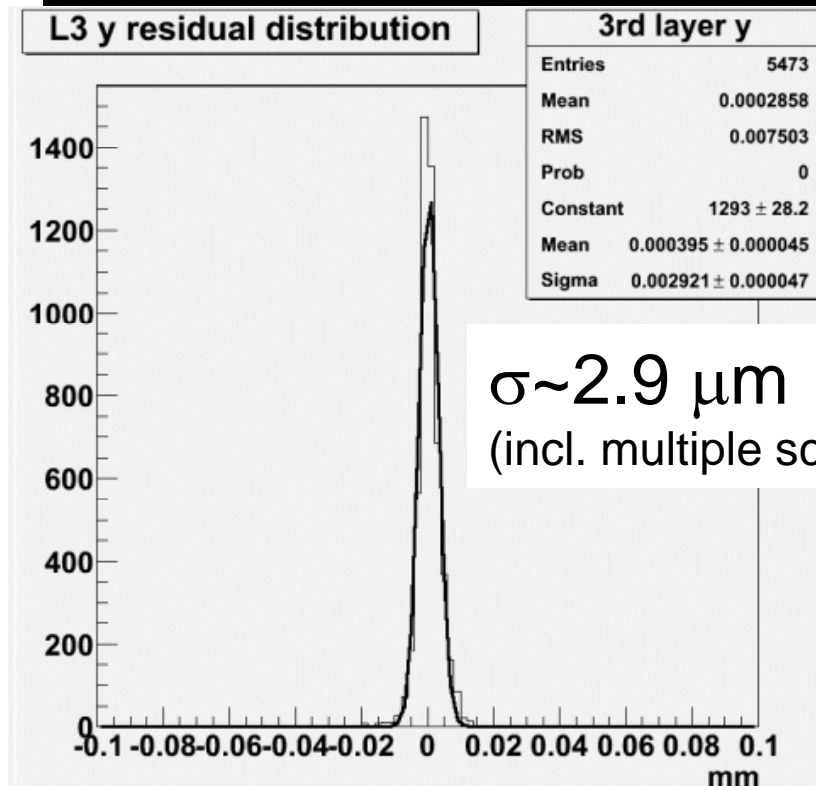
Counting Type Pixel (CNTPIX)

CNTPIX5 Pixel

Dual Discri

Vfb

Charge Amp

Shaper

VthH

VthL

Window

from/to other 3 pix

Counter Control Logic

Programable Counter

9 bit   9 bit

fine DAC_H 3bit

fine DAC_L 3bit

Control Registers

18

+Vdet
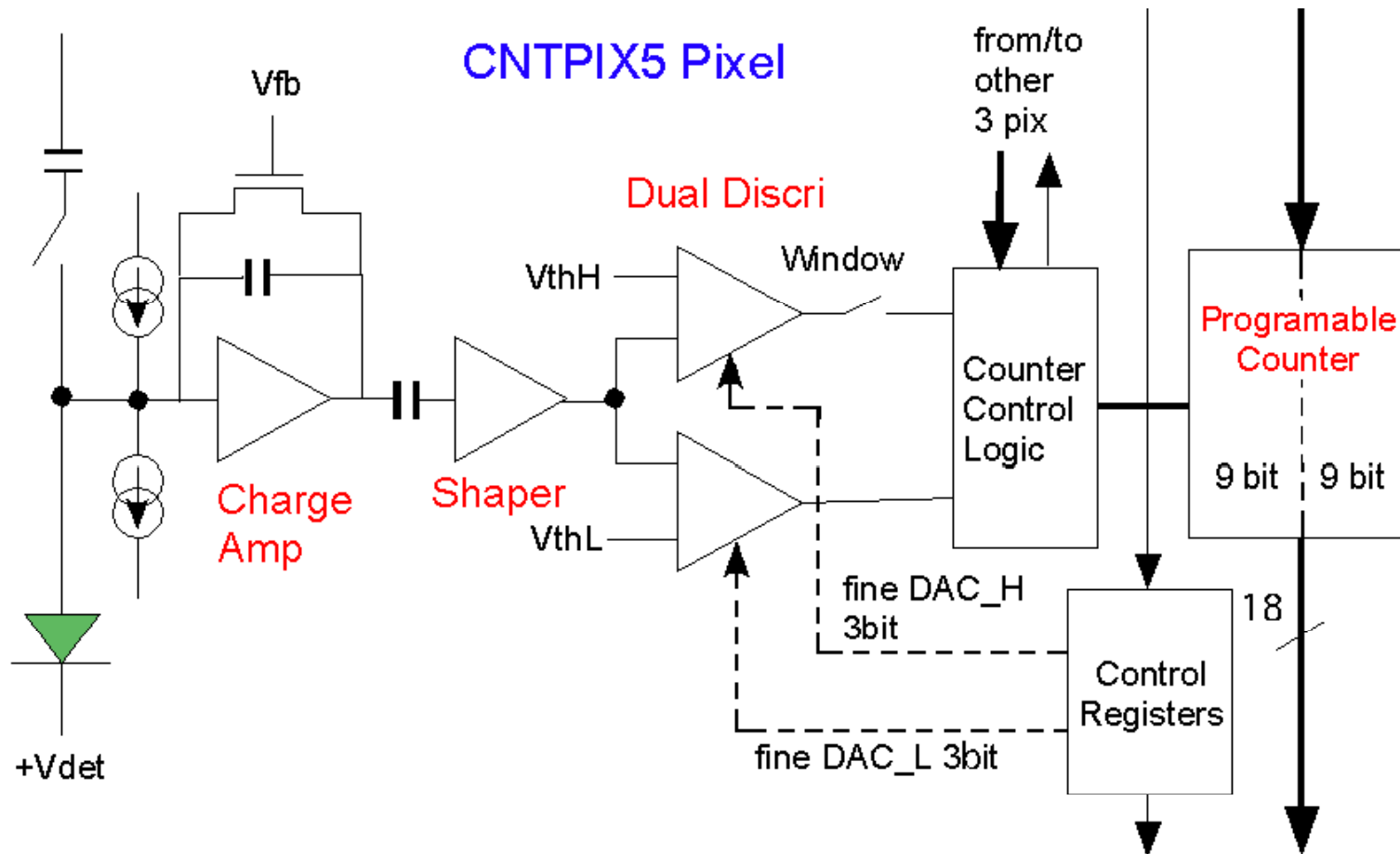
Energy selection and Counting in each pixel. 4 pixels can be combined.

5 x15.4 mm^2
72 x 272 pixels
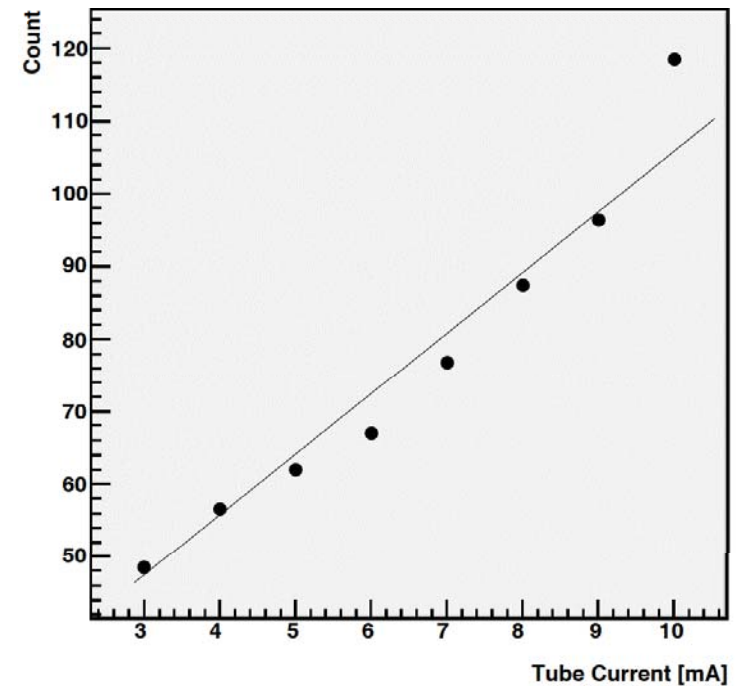64um x 64 um pixel
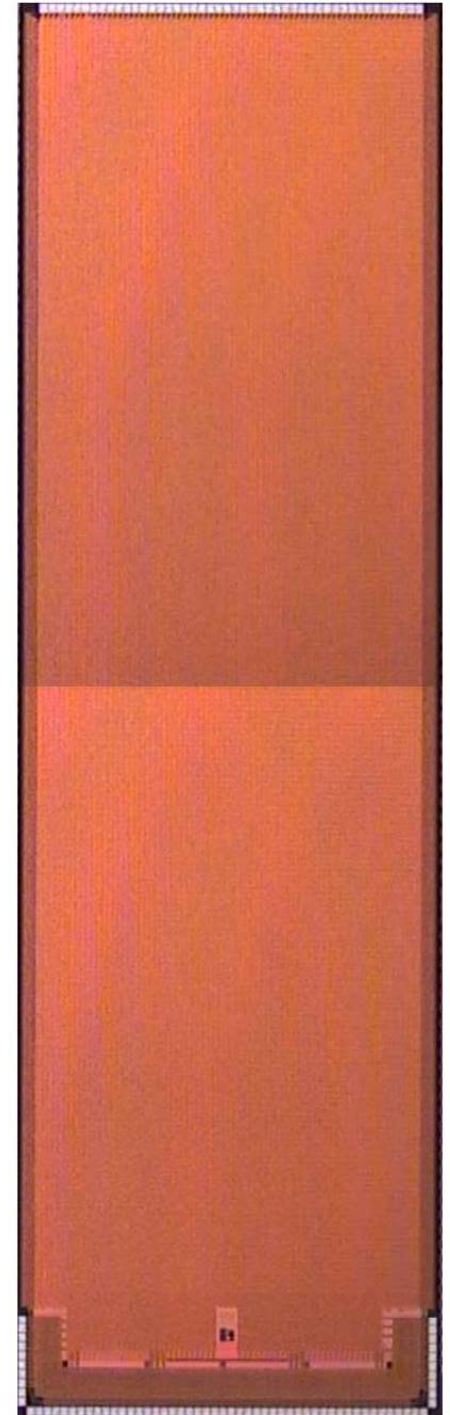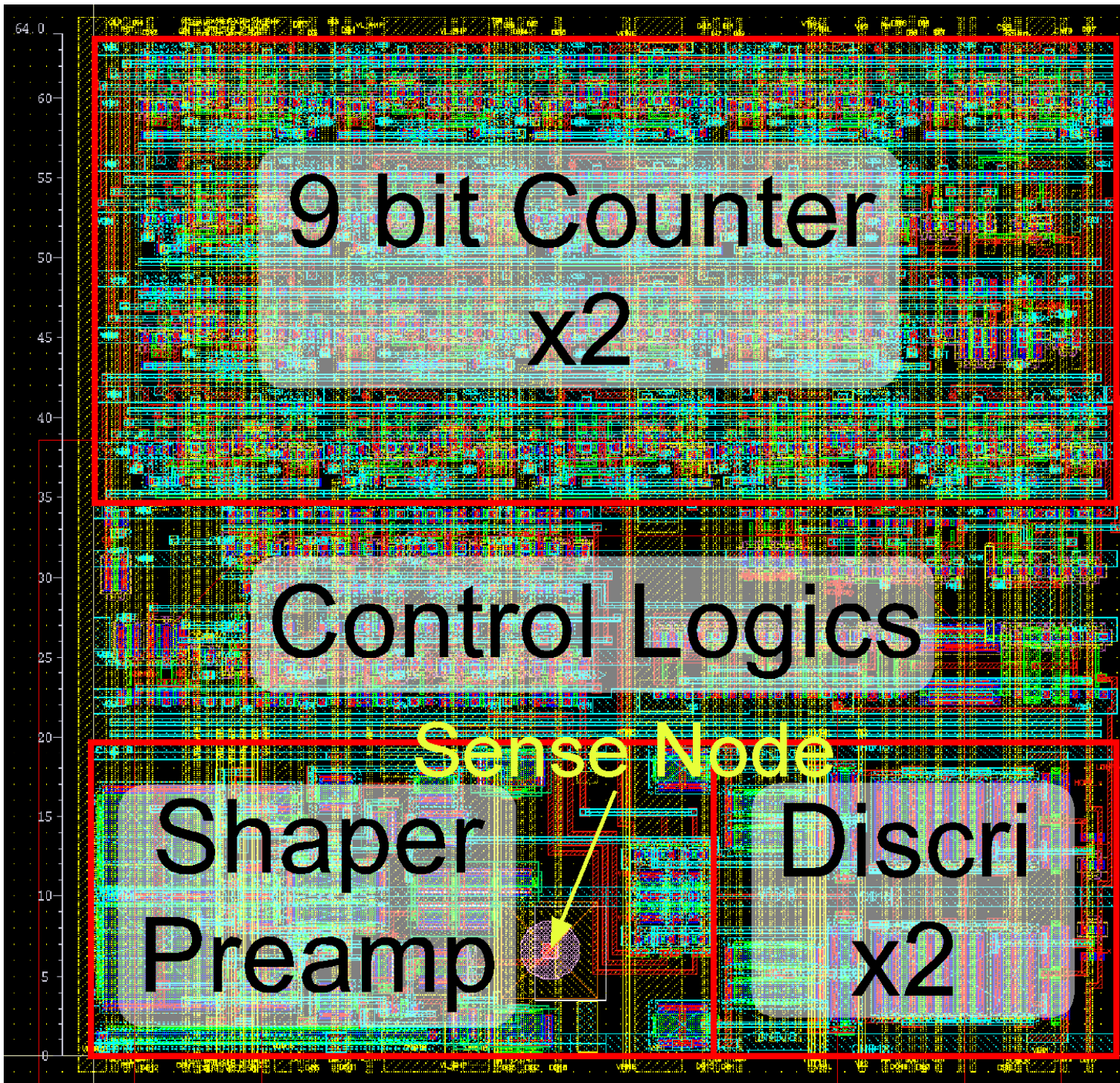
CNTPIX5
Pixel Layout

64x64 um^2

~600 Tr/pix
x 72 x 212
= 10 M Trs

9 bit Counter x2

Control Logics

Sense Node

Shaper Preamp

Discri x2

CNTPIX X-ray Test

Pixels are working but some crosstalks are observed.
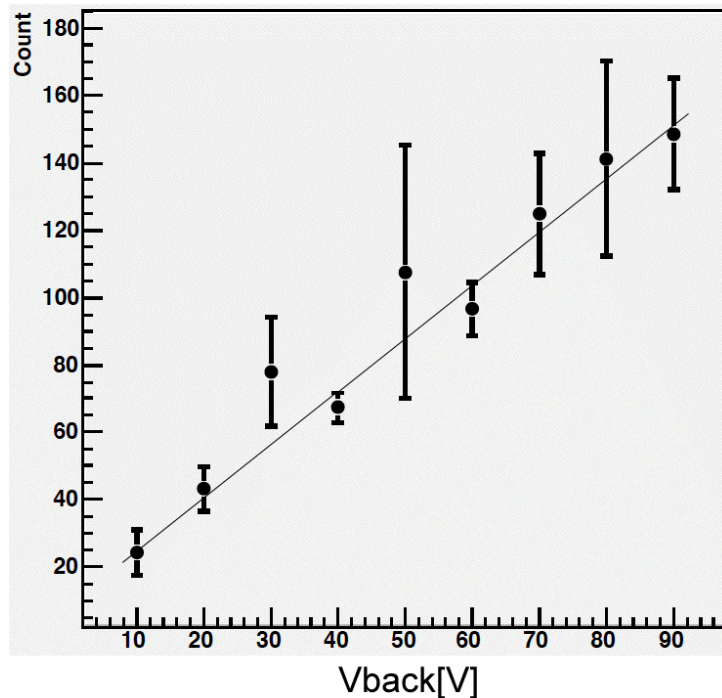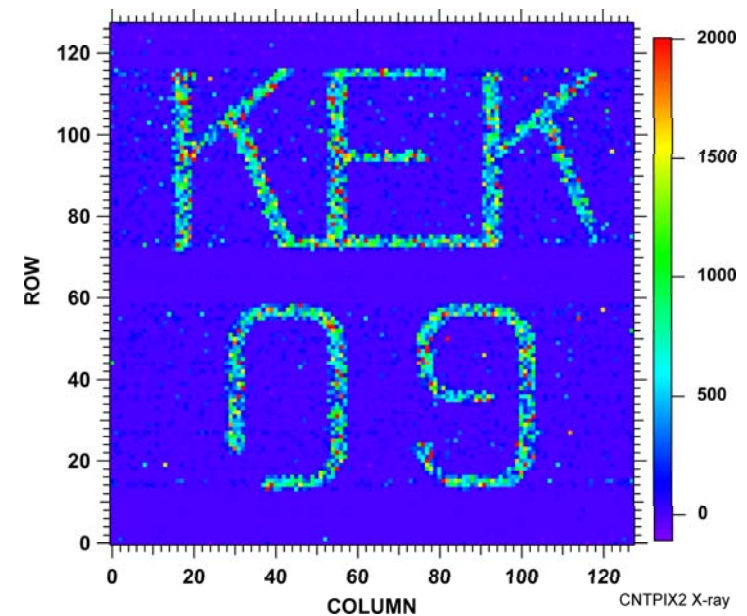
Count v.s. sensor bias.

Count v.s. X-ray Tube Current

Developing Techniques
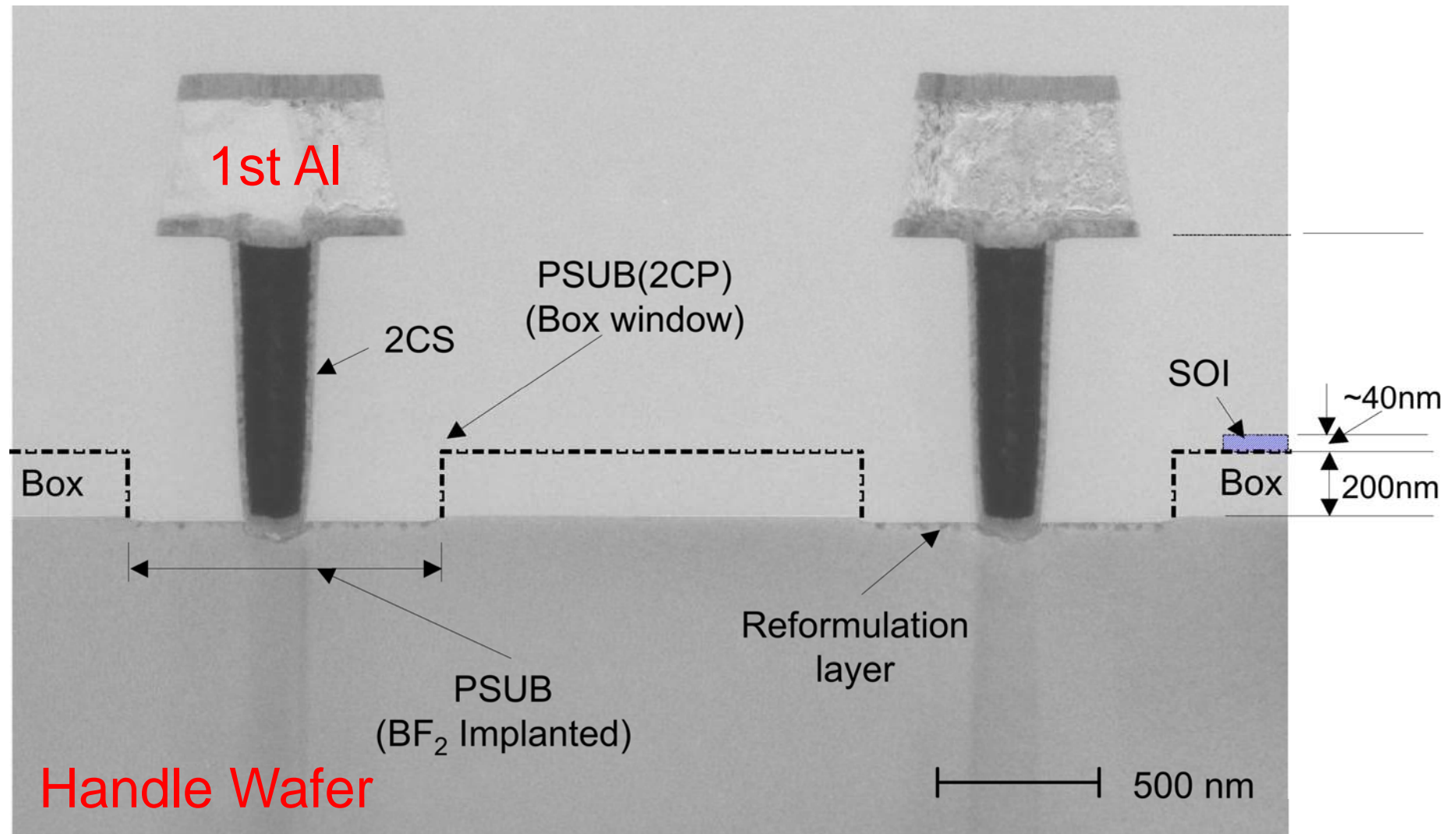
Buried p-Well (BPW)

Substrate Implantation

BPW Implantation

Buried
Oxide
(BOX)

SOI Si

Pixel   Peripheral

P+

BPW
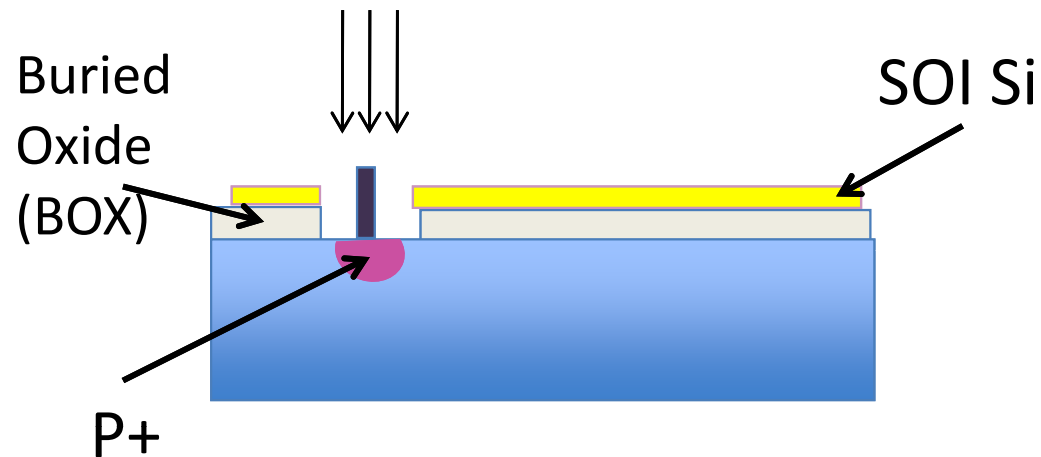
- Cut Top Si and BOX
- High Dose
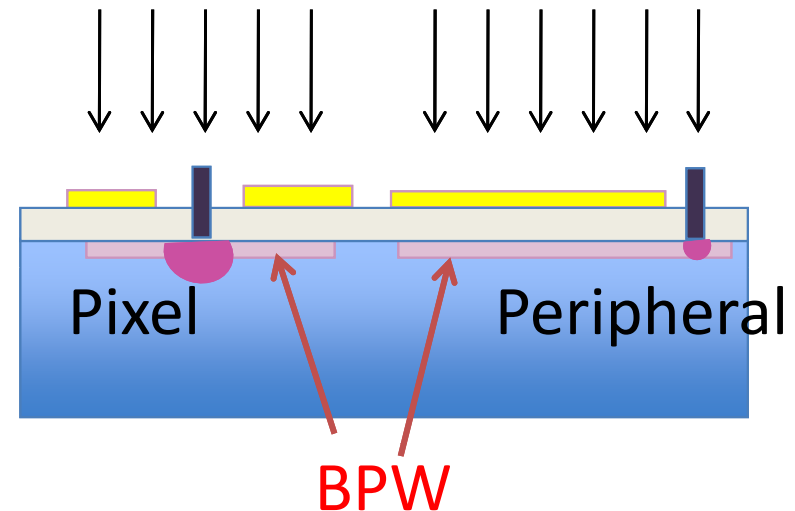
- Keep Top Si not affected
- Low Dose

- Suppress the Back Gate Effect.
- Shrink pixel size without loosing sensitive area.
- Increase break down voltage with low dose region.
- Less electric field in the BOX which improve radiation hardness.

$\underline{I_d}$-V_g and BPW
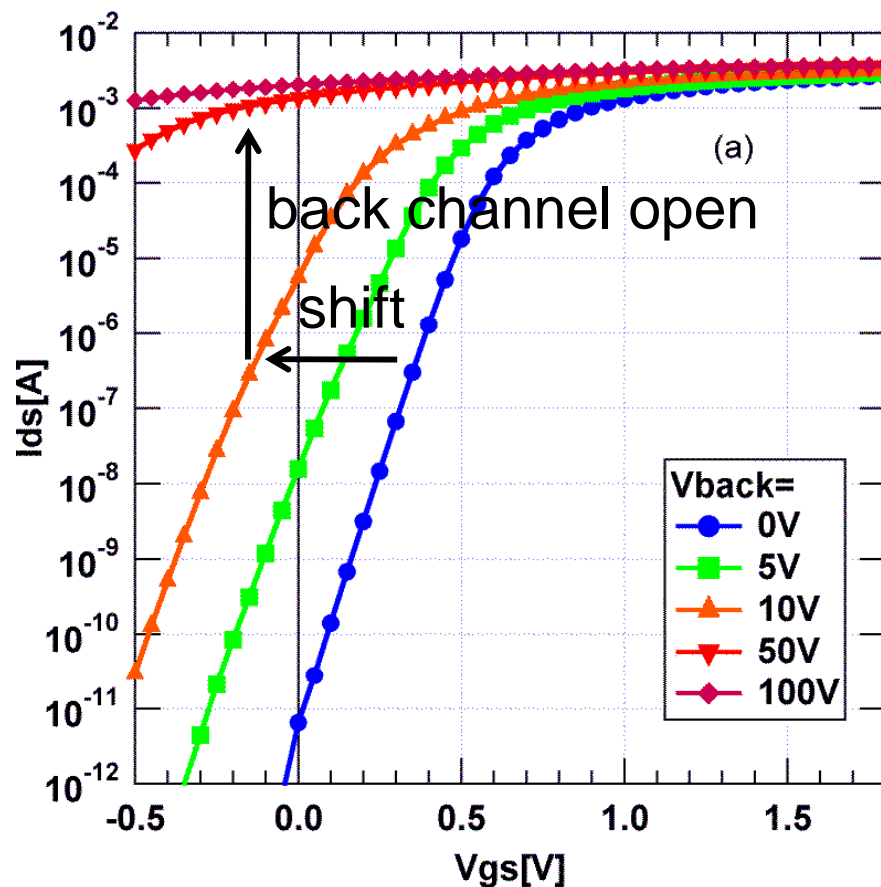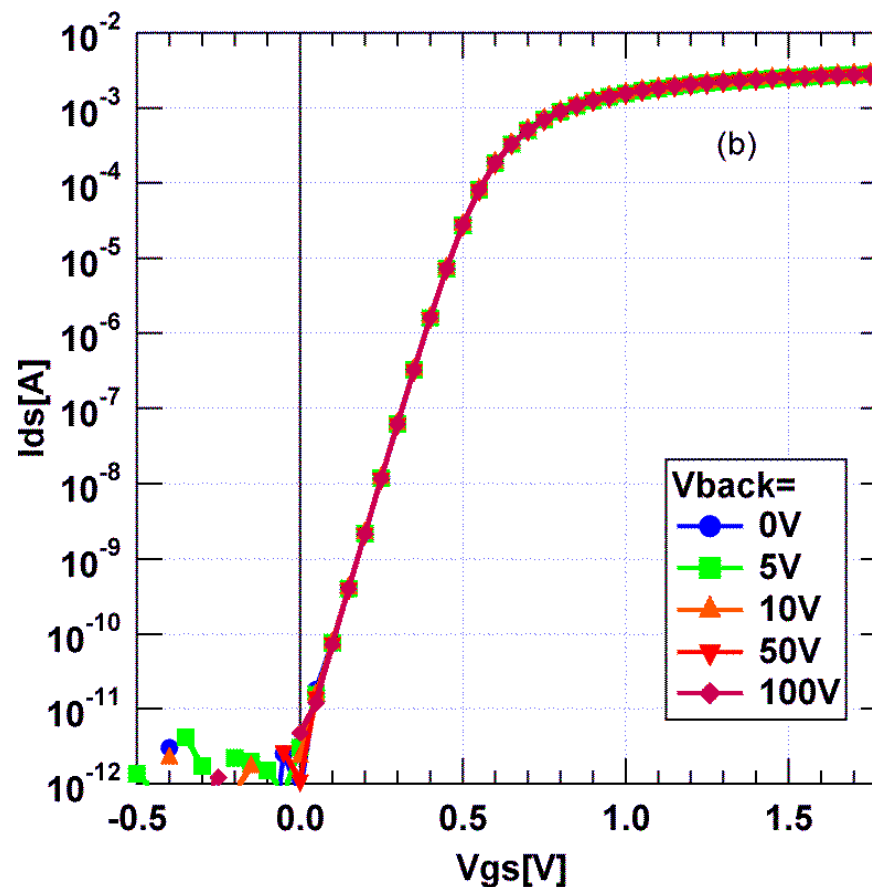
Back gate effect is suppressed by the BPW.

Radiation Tolerance

SOI is Immune to Single Event Effect

Gate Oxide

Gate

Gate

Si

Si

Buried Oxide

Depletion Layer

Bulk Device

SOI Device
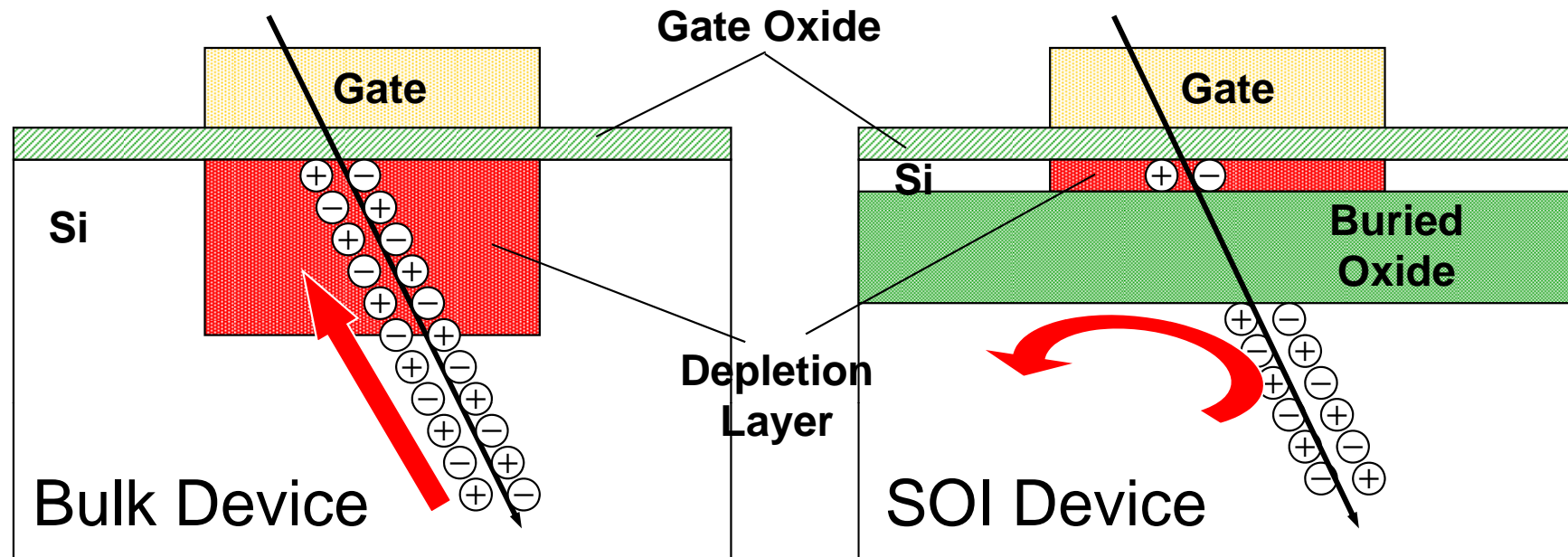
But not necessary strong to Total Ionization Dose due to thick BOX layer

Gate

Si

Buried Oxide

Trapped Holes
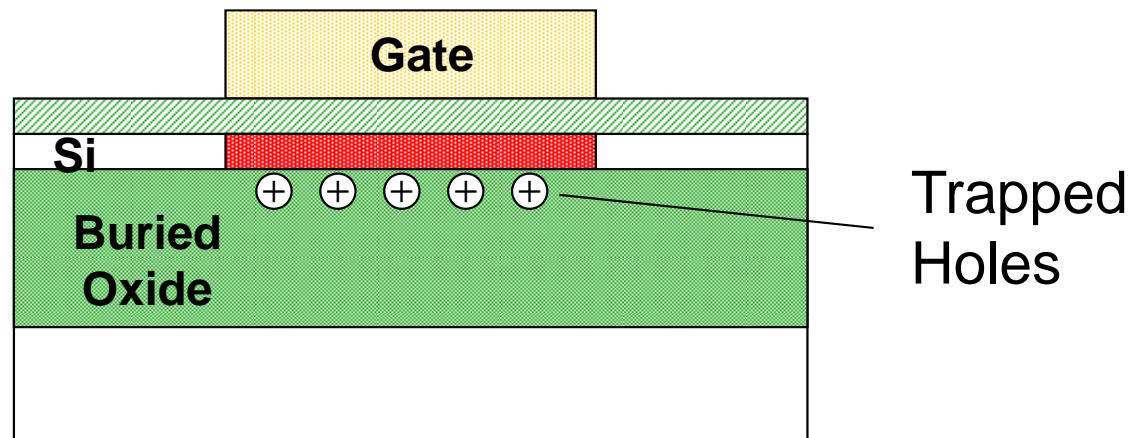
Radiation Tolerance and BPW

By adding the BPW layer, Electric field in the BOX is reduced and possibility of charge recombination will increase. Thus increase radiation tolerance.

X-ray Irradiation
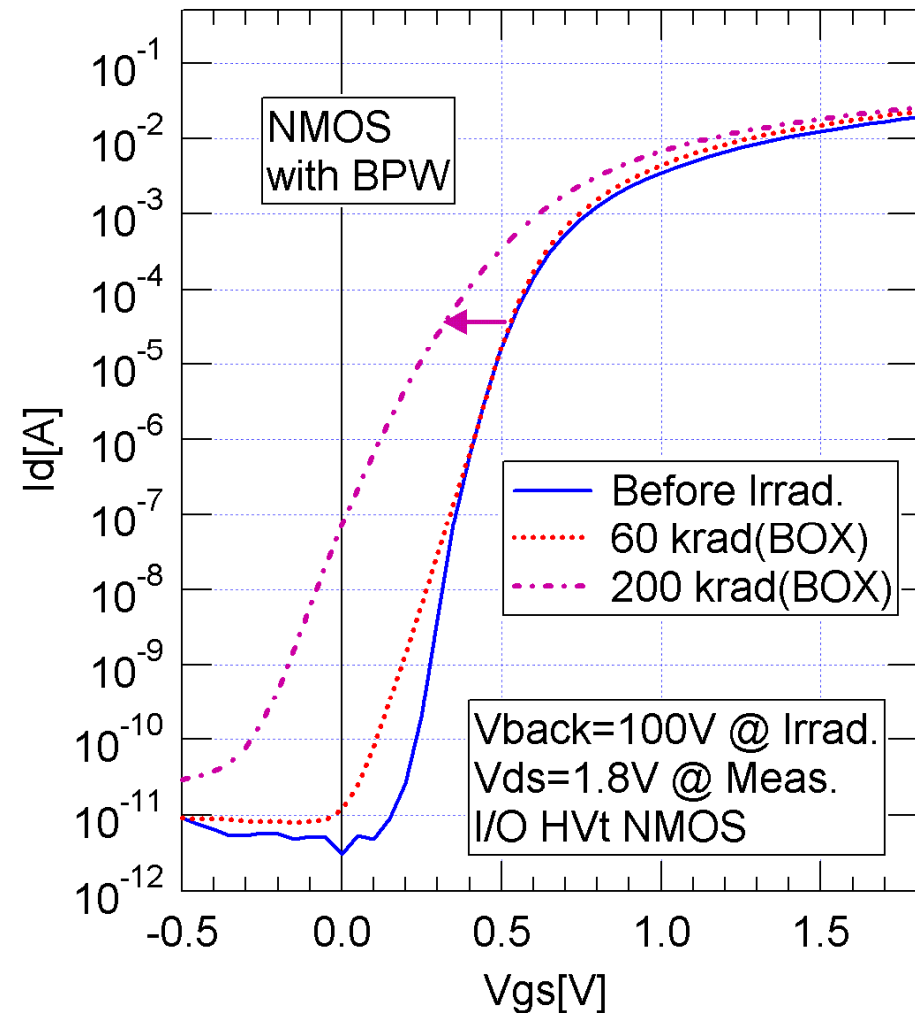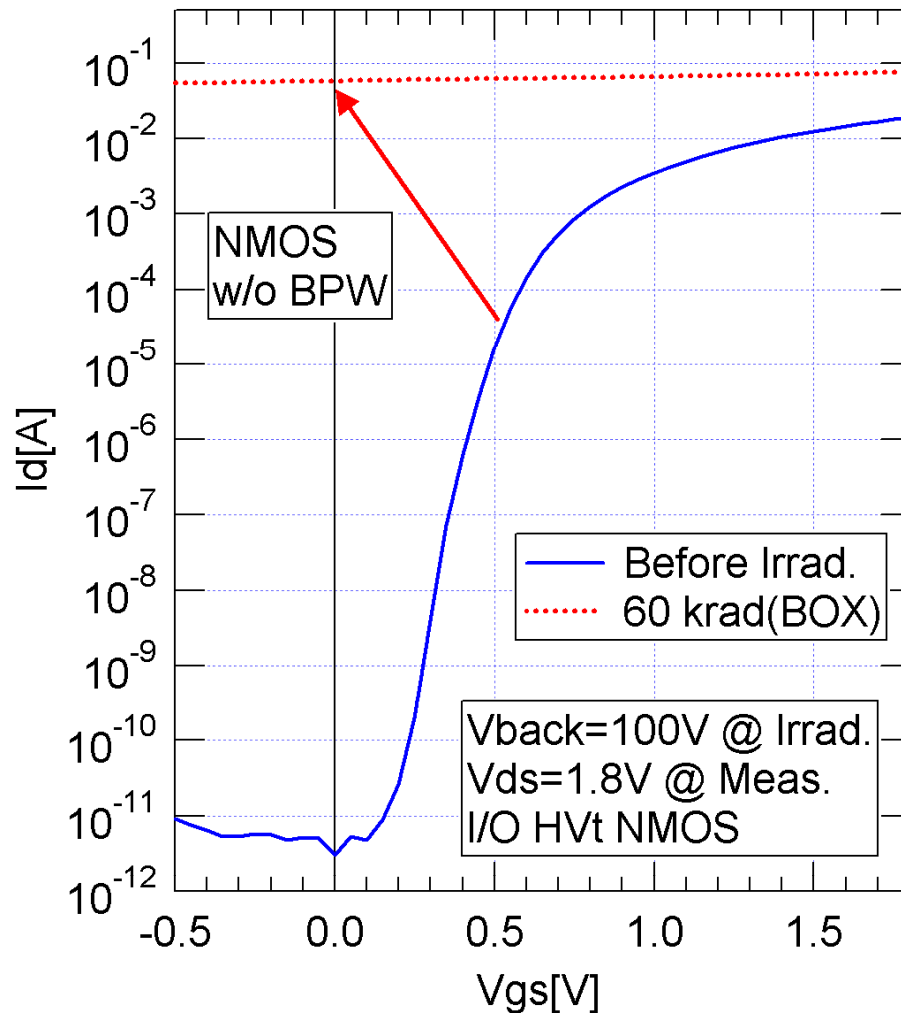
TID(Total Ionization Doze) Damage Compensation

Leak Current and V_{Th} resumes to nearly original value by biasing back side even at 100Mrad.

Vback= 0 -10 -20 -30V

10^{15} p/cm^2
(~100 Mrad)

before
irradiation

pre_
BG_0
BG10
BG20
BG30

Id[A]

Vgs[V]

10^{15} p/cm^2
(~100 Mrad)

△Vt[V]

Backgate Bias[V]
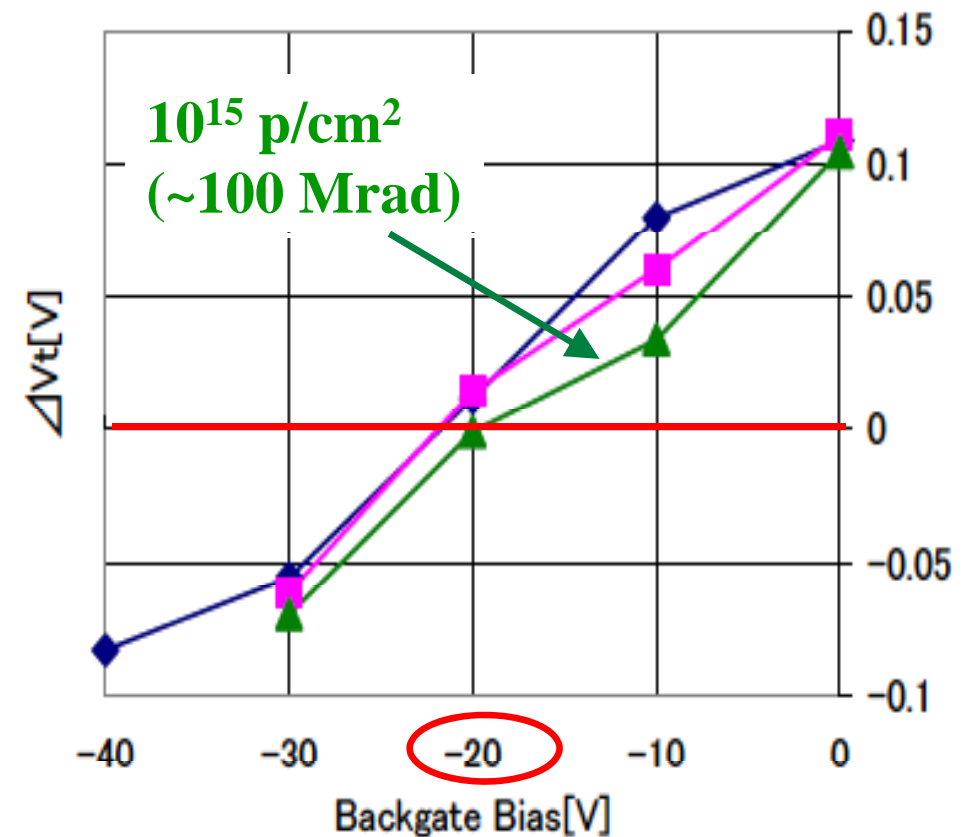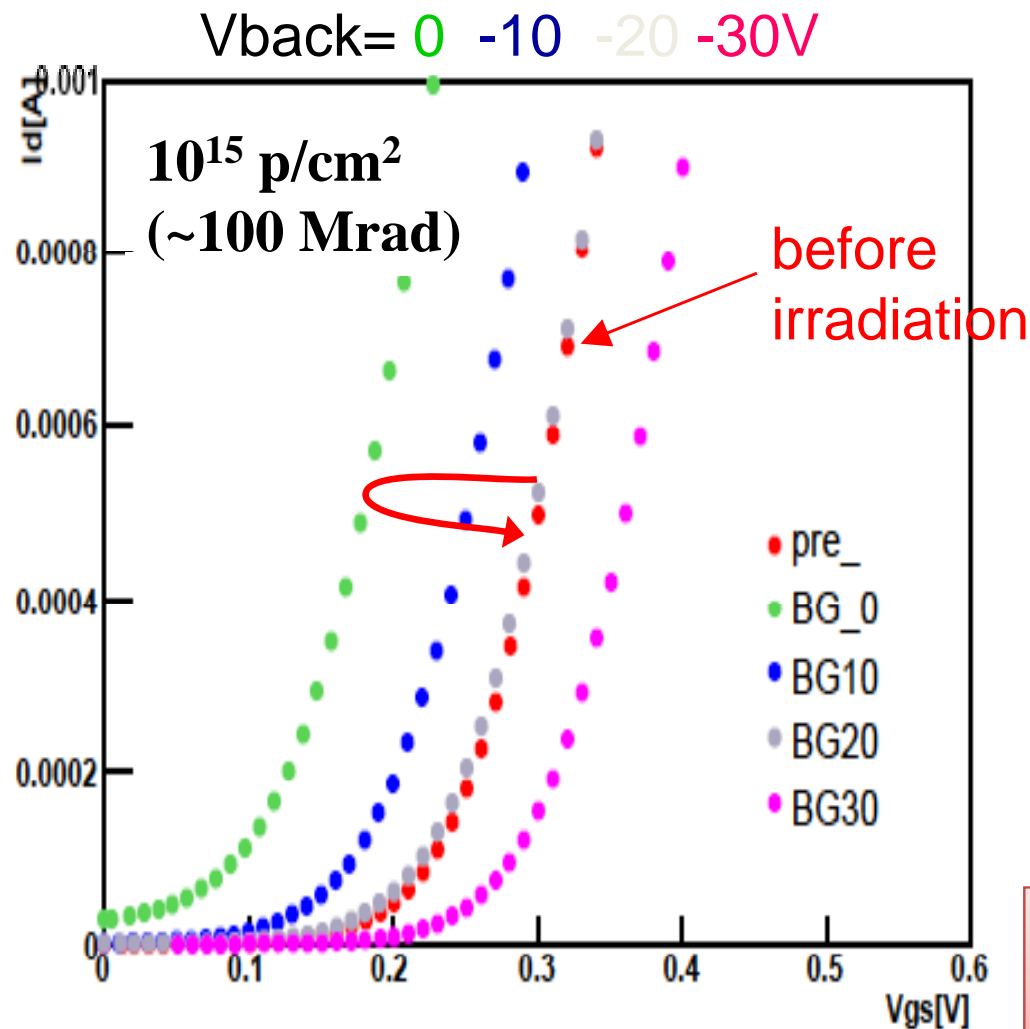
This can be done with nested well or double SOI wafer

FZ(p and n) SOI Wafer

It was difficult to process 8" FZ-SOI wafer in CMOS process.

Before Oxidation	Conventional SOI Process	Improved SOI Process
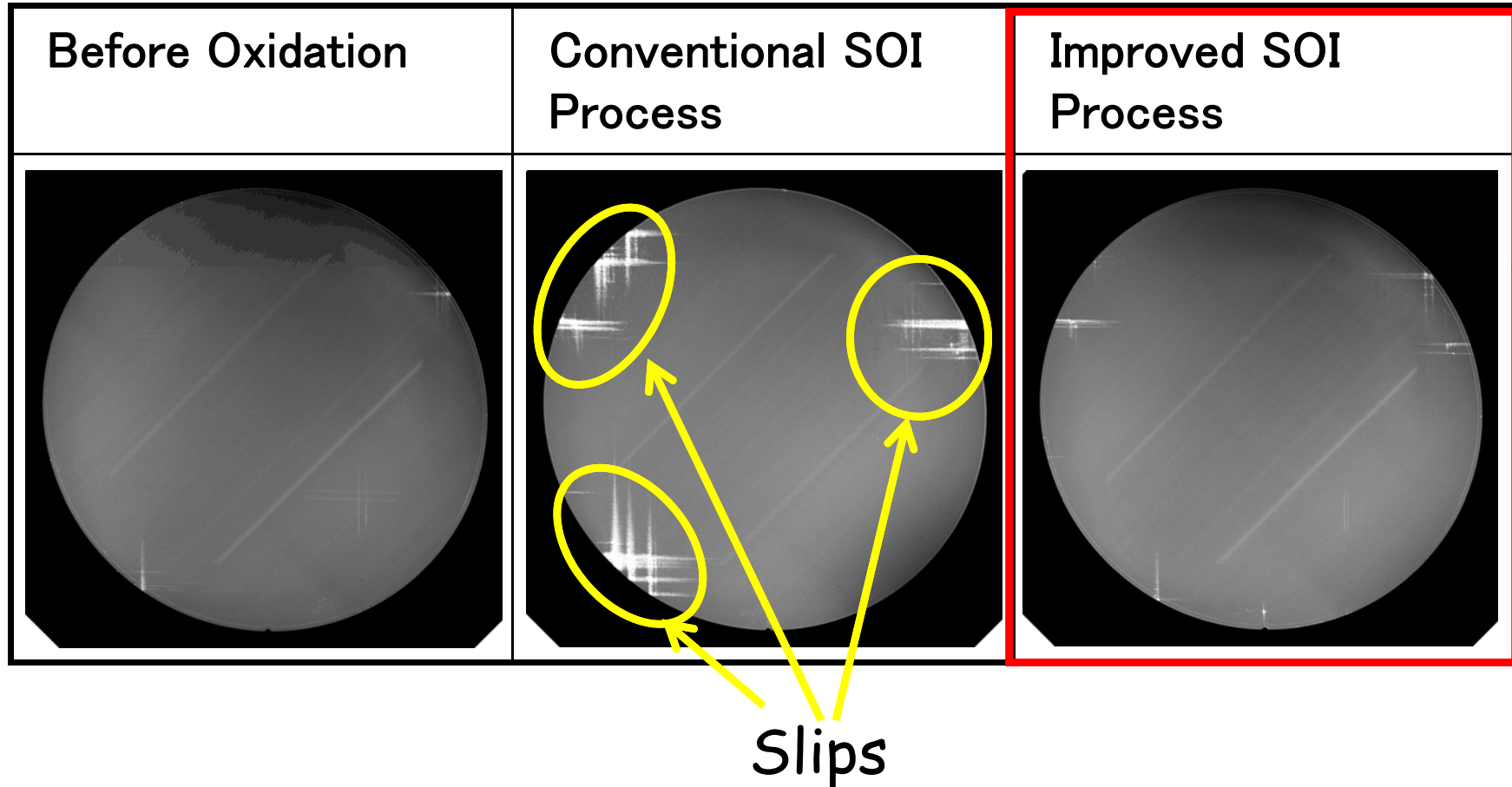
Slips

We optimized the process parameters, and succeeded to perform the process without creating many slips.

Wafer type and Leakage Current
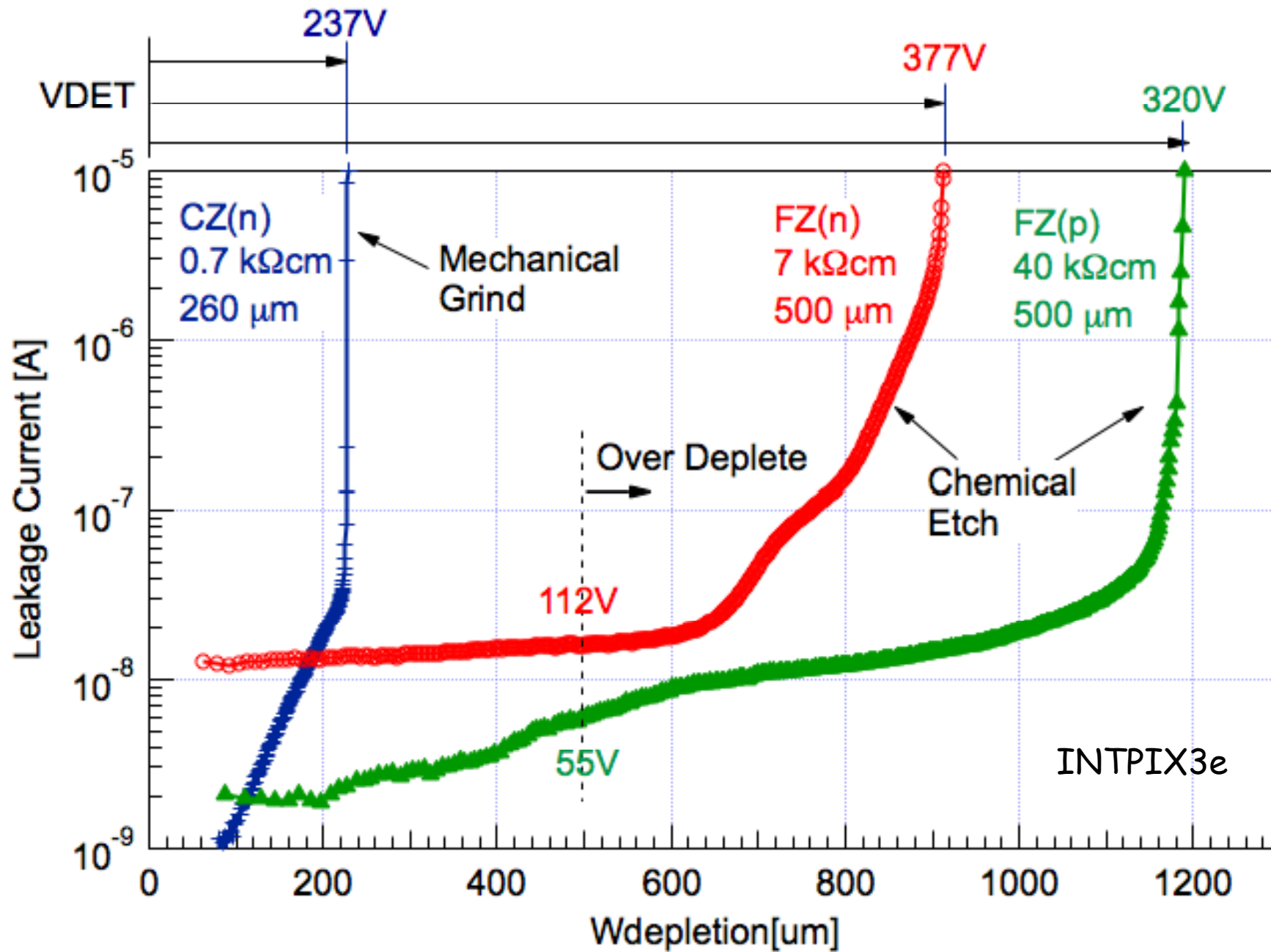
Nested BNW/BPW Structure
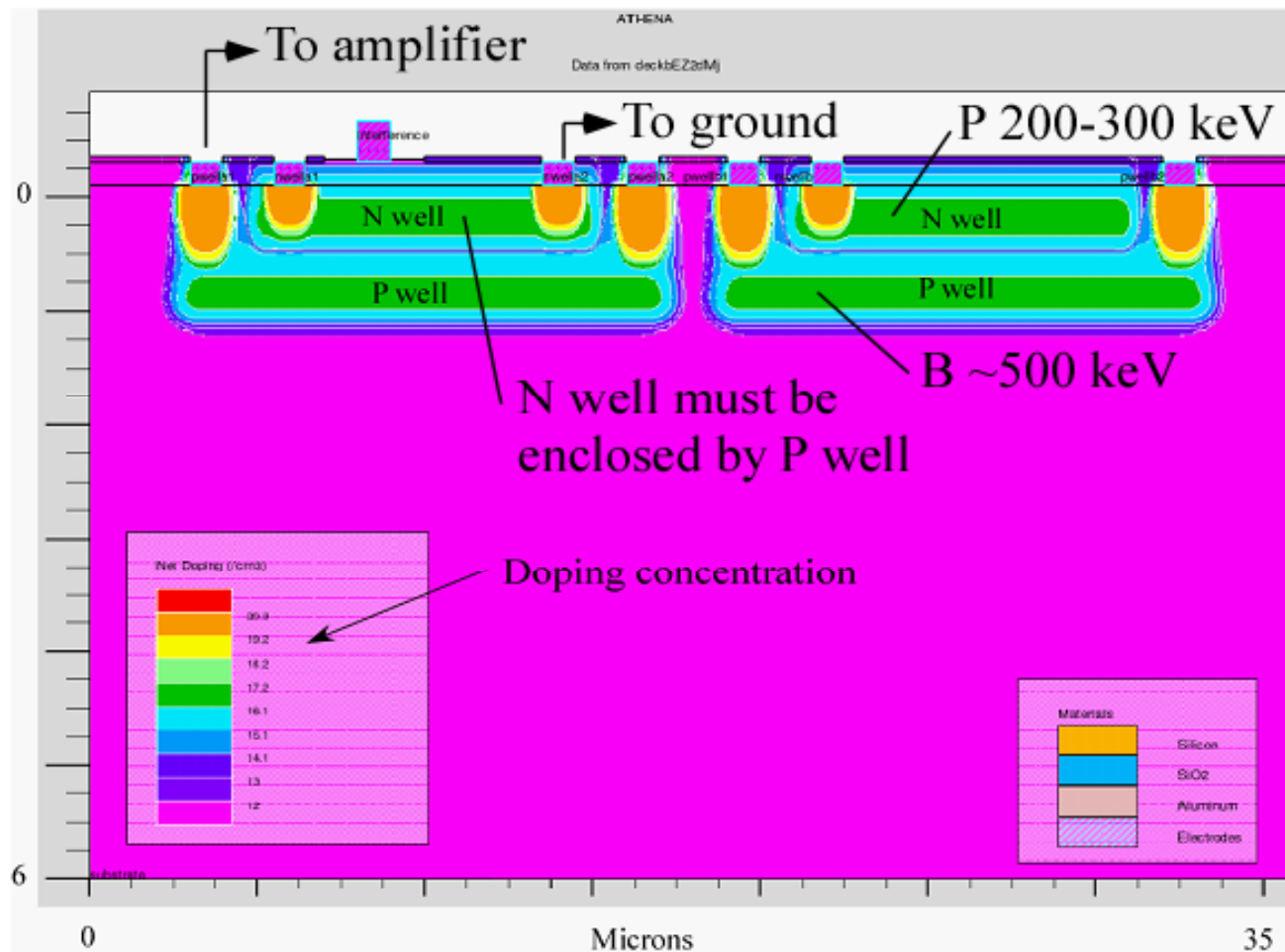
- Signal is collected with the deep Buried P-well.
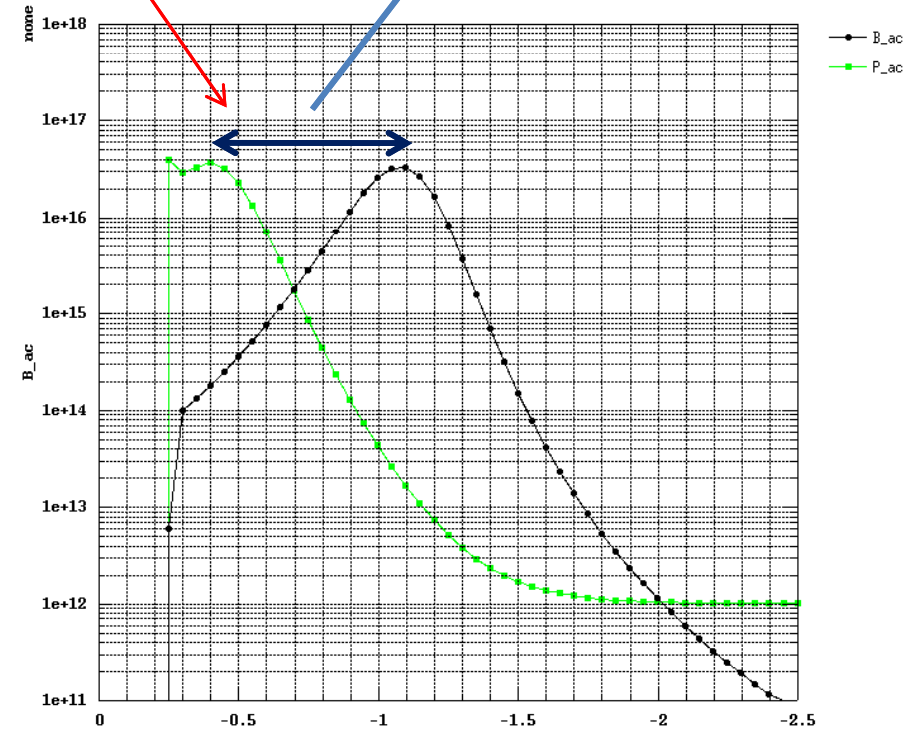- Back gate and Cross Talk are shielded with the Buried N-well.

FEE2011 G. Deptuch (Fermilab)

Impurity Concentration
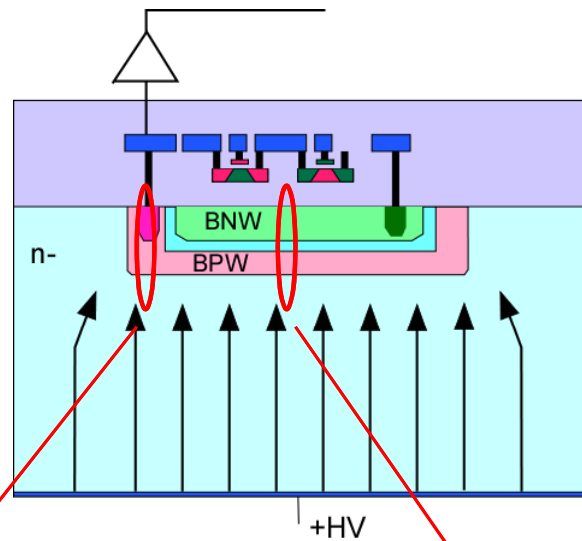
Peaks of BNW and BPW are separated ~0.7 μm to reduce capacitance
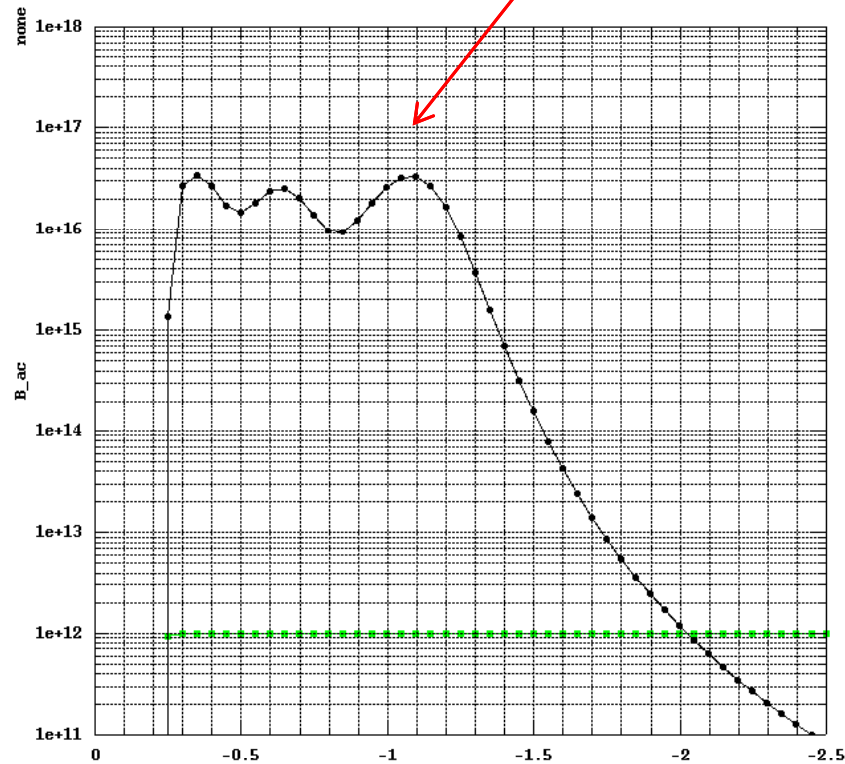
Double SOI Layer wafer
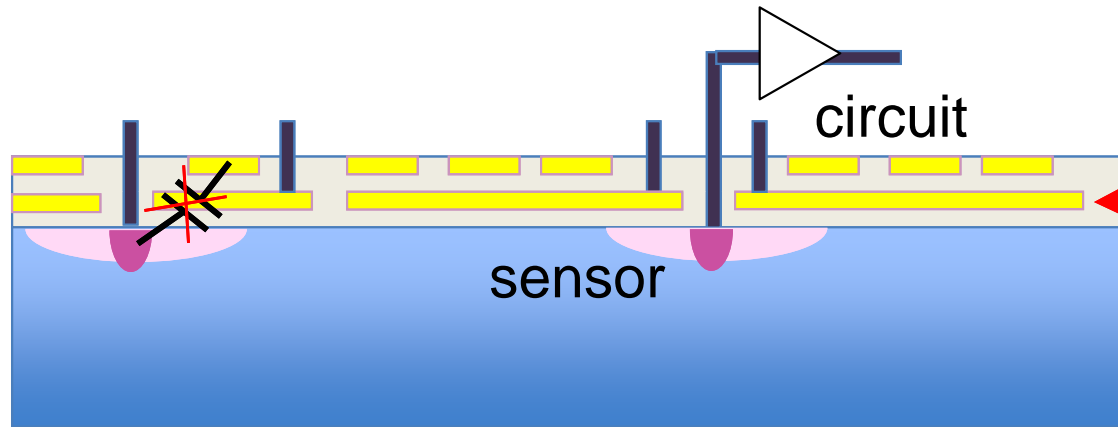
circuit

sensor

additional conduction layer

Shield sensors from circuit

In addition to the shielding between sensor and electronics,

* oxide trapped hole can be compensated

* able to control Tr threshold voltage block by block

* additional components such as diode, resistors can be implemented.

Wafer is ready.
Process study is in progress.

断面TEM写真（CMP）

130nm	Surface
	Si
150nm	BOX
96nm	Si
150nm	BOX
	BASE
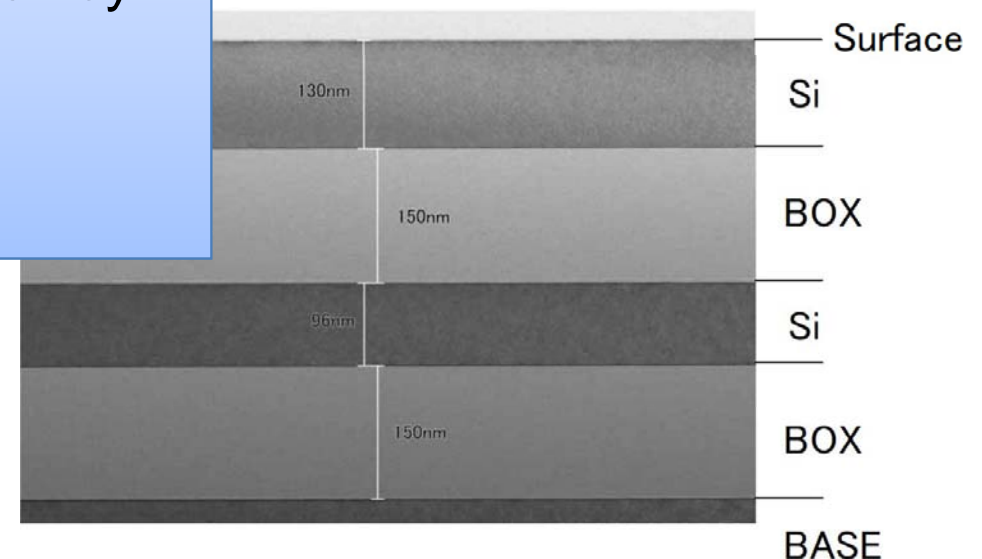
Larger Mask

Present Mask

20.8 mm
x
20.8 mm
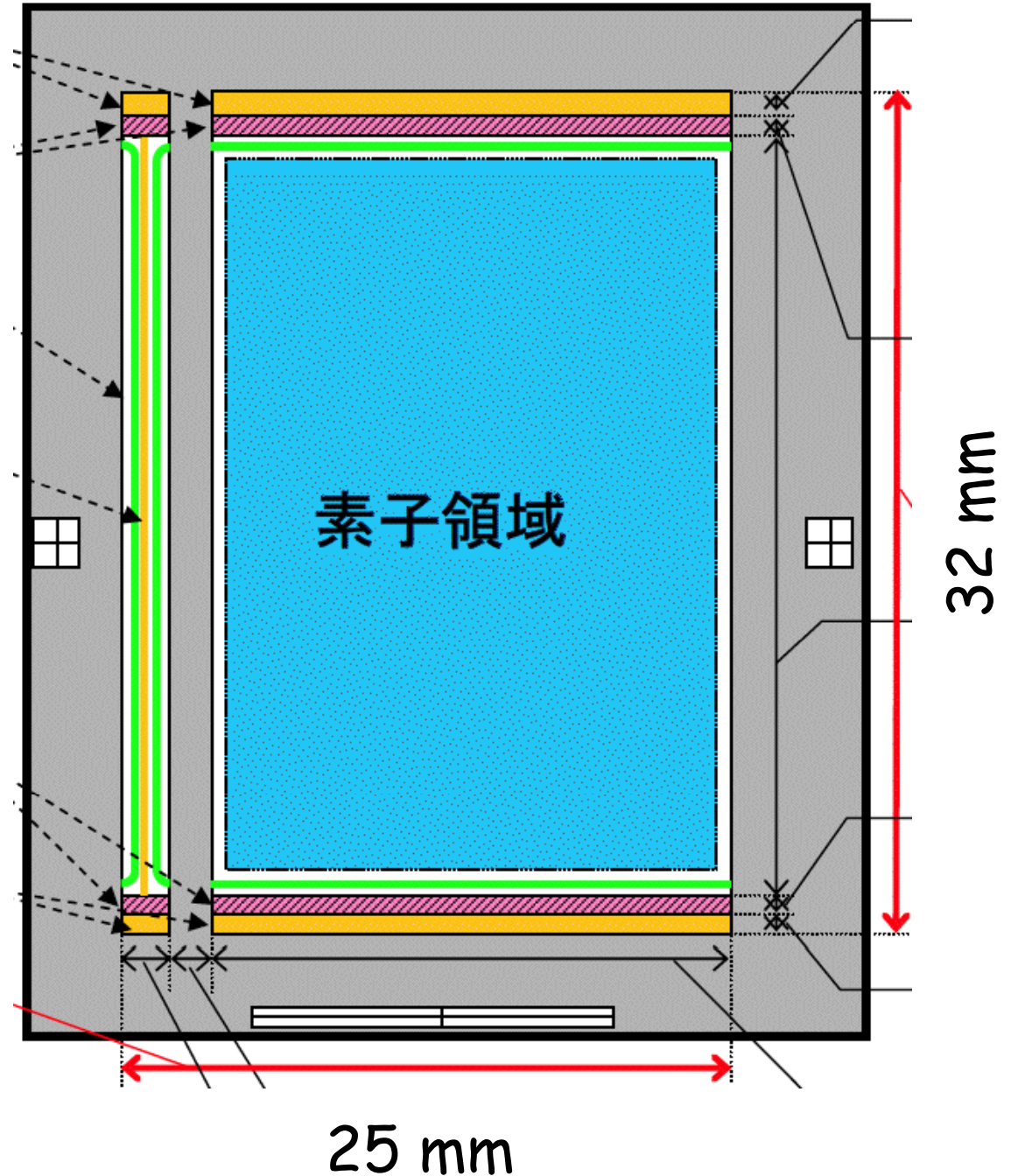
Larger mask will be used from next MPW run.
→ Larger Sensor & Reduced cost per area.

New Mask

素子領域

32 mm

25 mm

Stitching

Stitching test is in preparation.

~30 mm

~66 mm
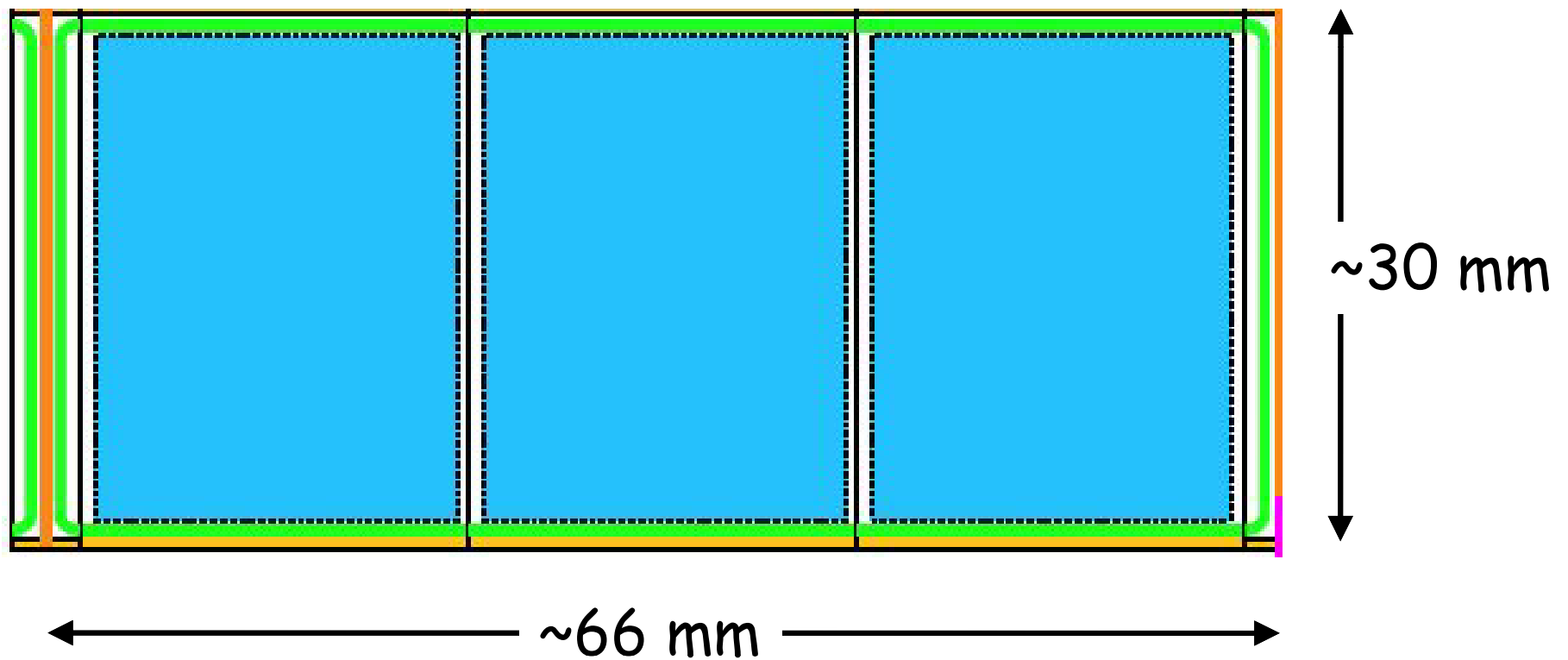
Vertical (3D) Integration

We have submitted 3D test chips on Feb. 2009 and Feb. 2010 to the SOI process. These chips are being bonded with μ-bump technology (~5 um pitch) of T-micro Co (ZyCube).
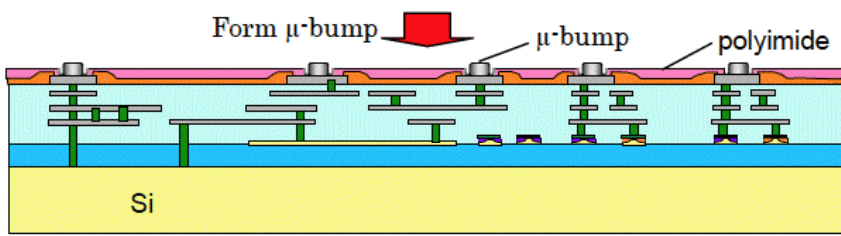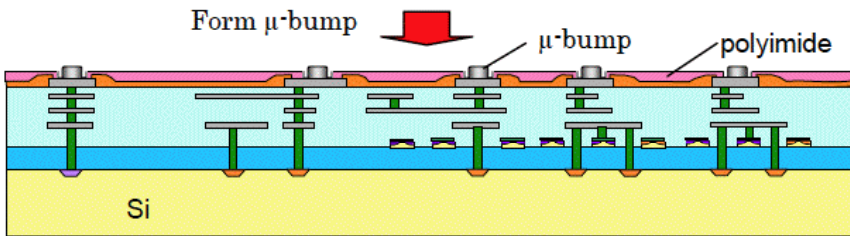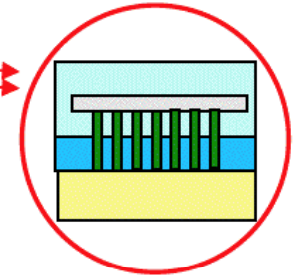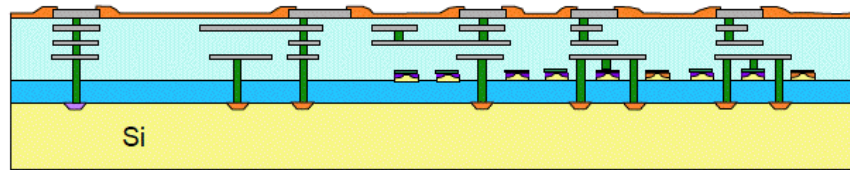We had a few technical problems and non-technical issues.
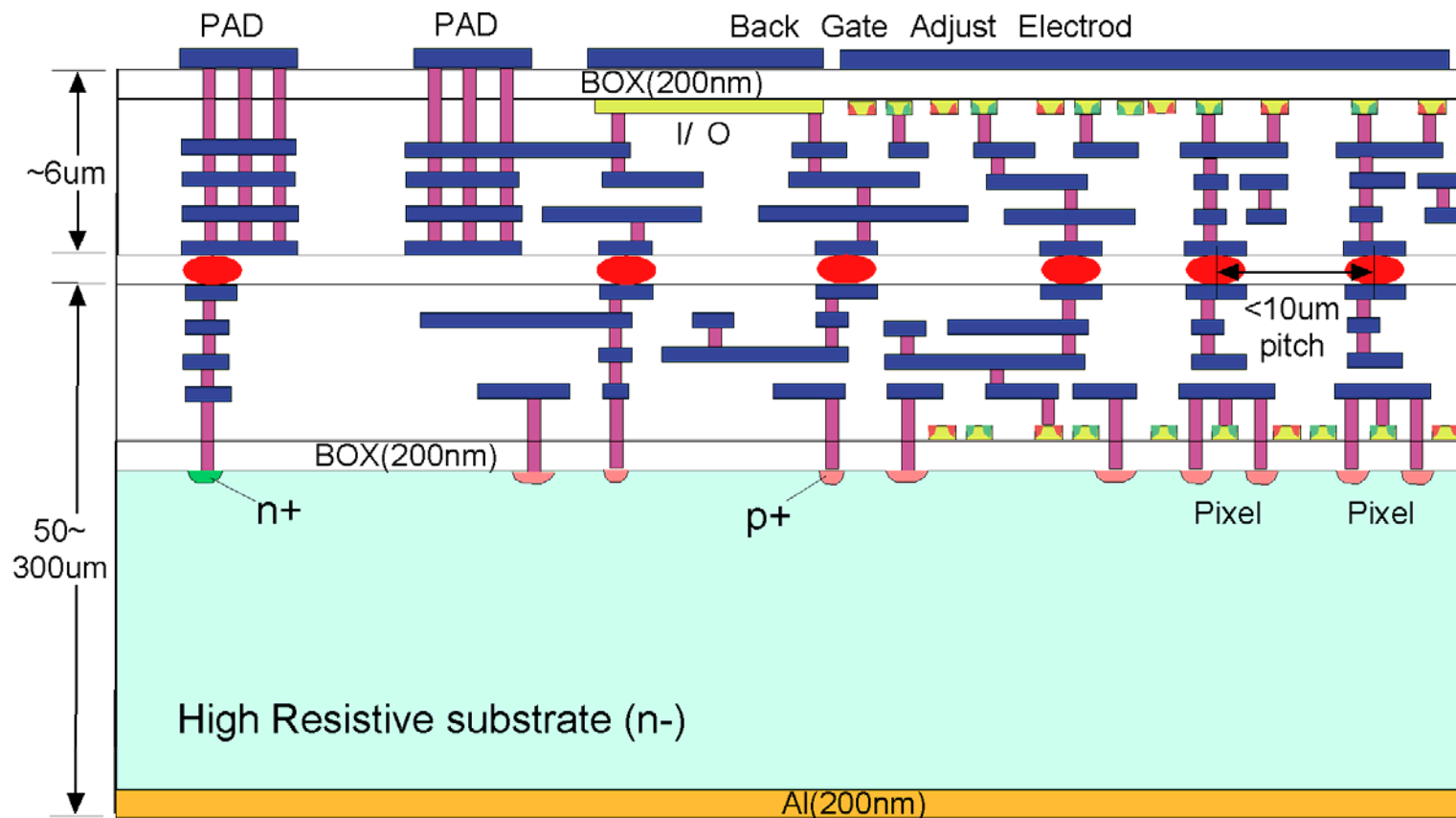
(1) Stack Process Flow (after finishing wafer process)

Lower Chip

Upper Chip
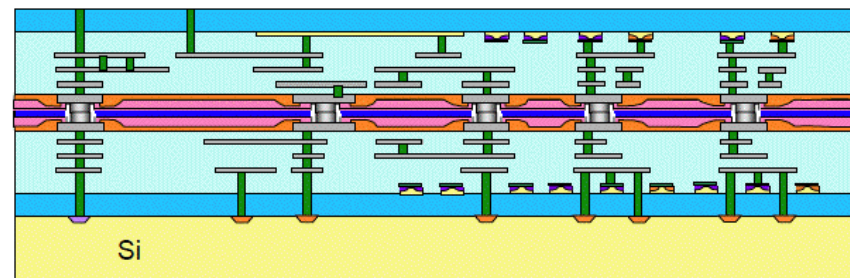(Layout must be done with mirror inverted)

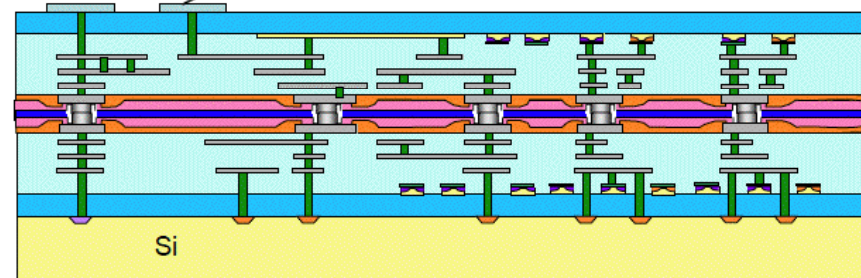Form μ-bump   μ-bump   polyimide

Form μ-bump   μ-bump   polyimide

-Stack wafer with
  μ-bump and adhesive
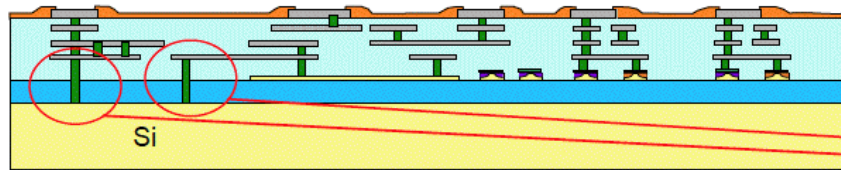
adhesive

-Ti/TiN/Al sputter
-Metal Pad Litho.

Al-pad

-Si etch
-SiO2 slight etch

-P-SiNd deposition
-Pad Litho.

P-SiN

T-Micro
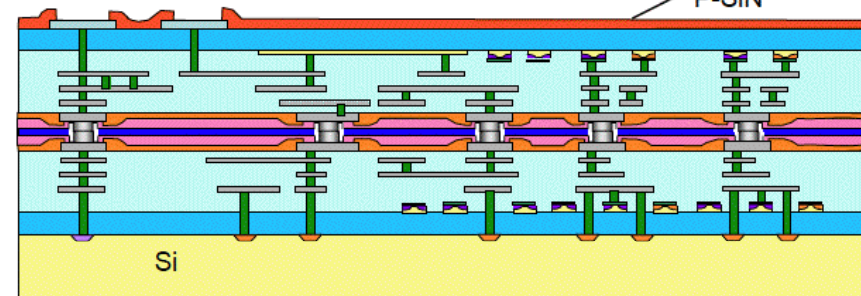
μ-bumps fabrication

10 um
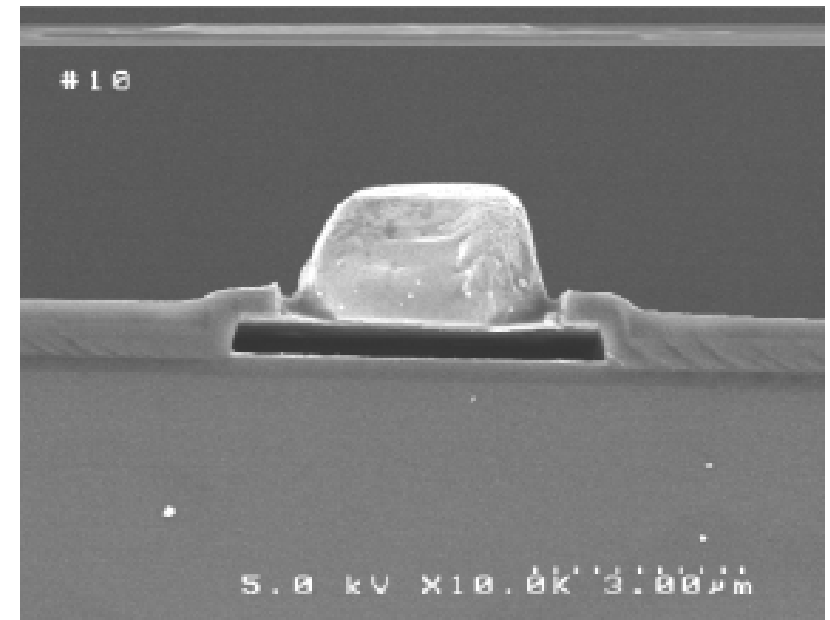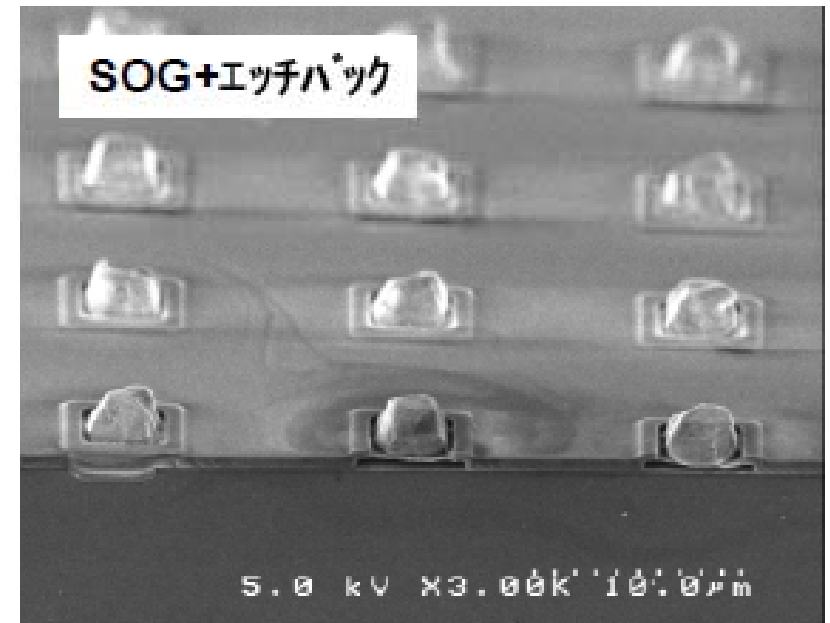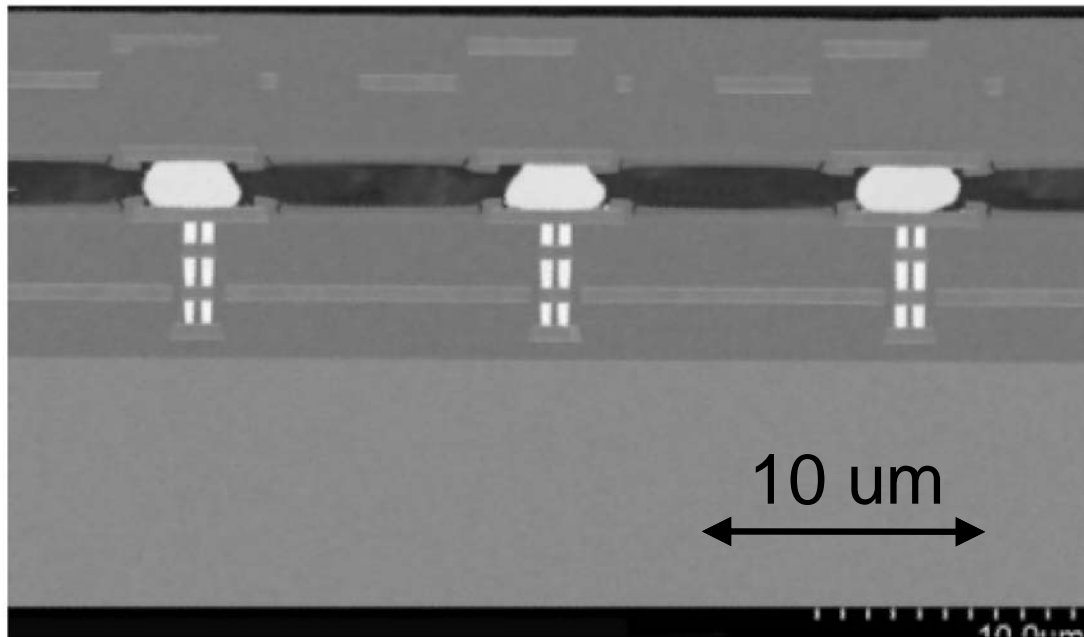
Difficult to Etching

Also Etched from side

Si   **Hi-R**   adhesive

Hi-R

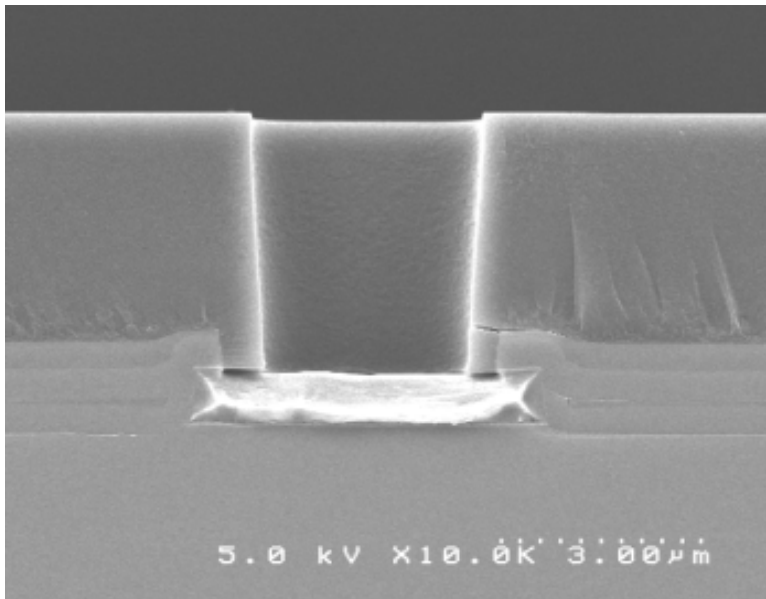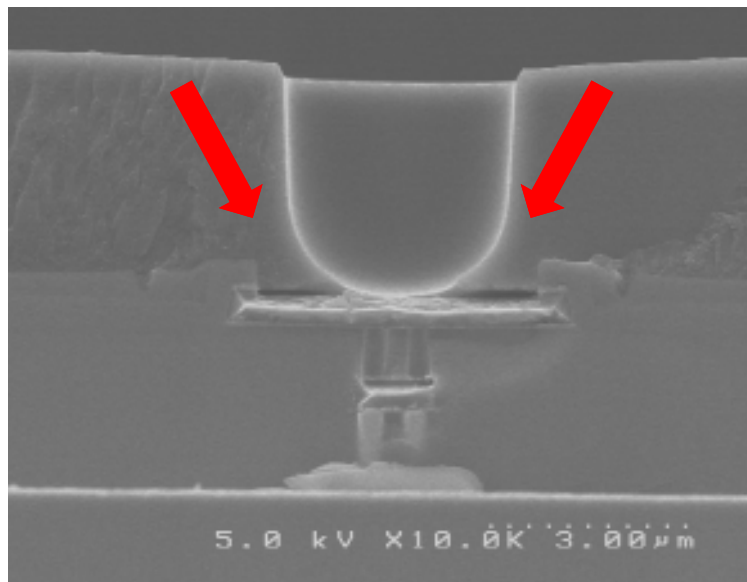**Easy to Etching**

Si   **Lo-R**   adhesive

Hi-R
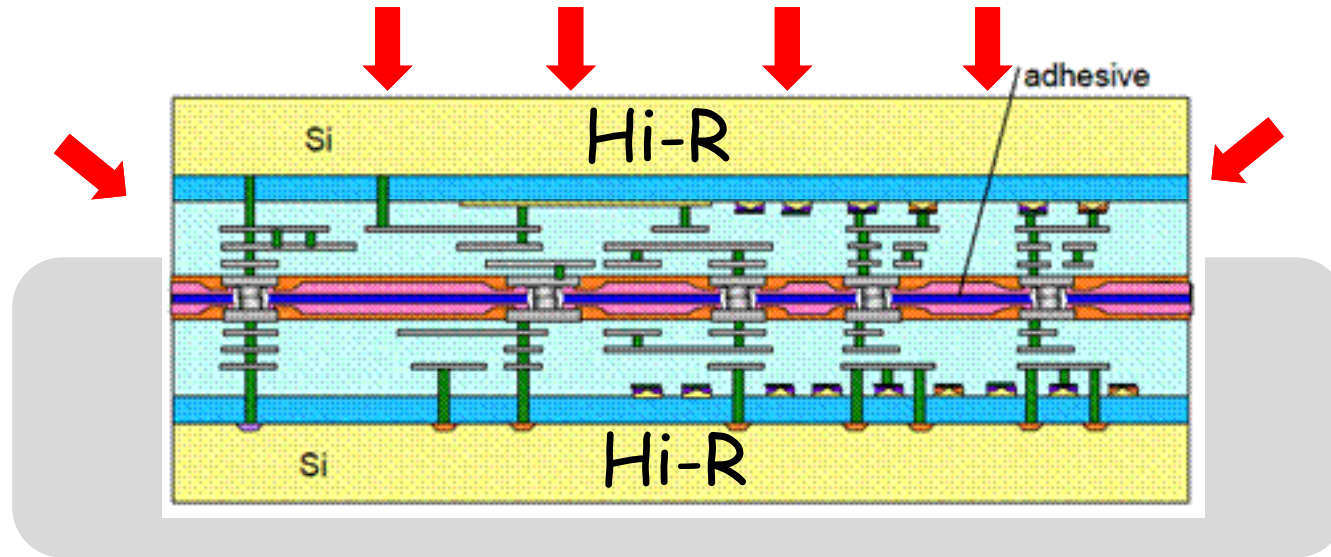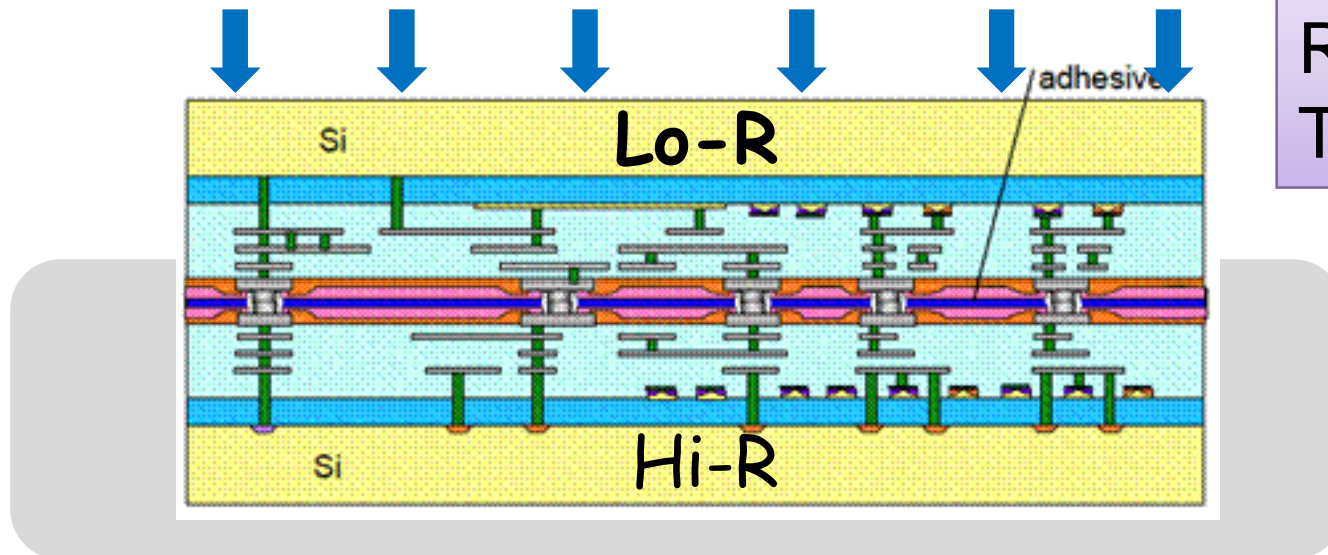
Change Low Resistive Wafer for Top Chip

We observed Resist is melting into the μ-bump hole after back grinding.
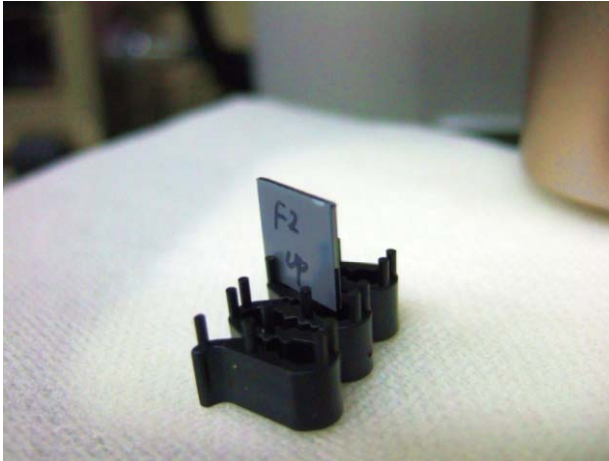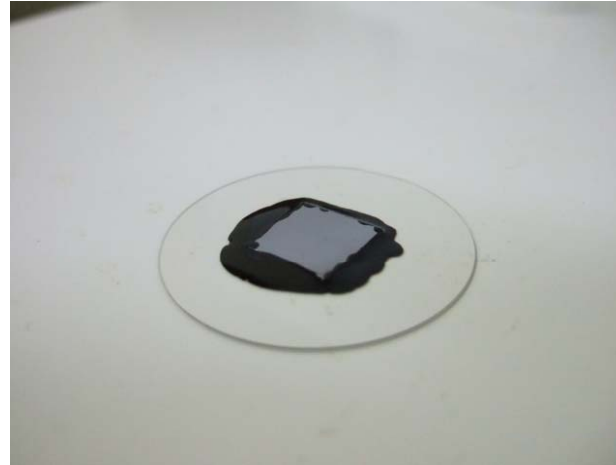
Back Grinding

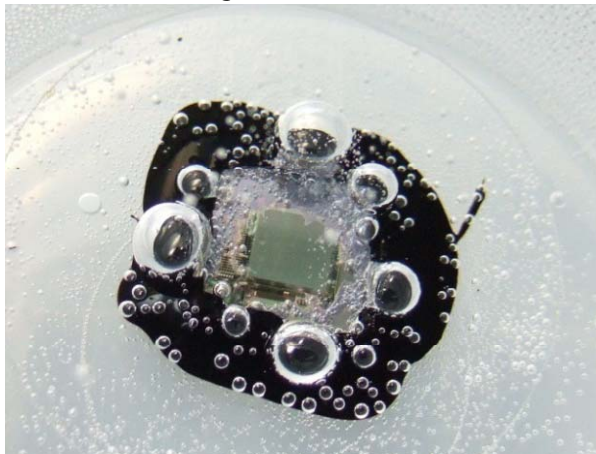We changed the order, so the back side is grinded before the μ-bump hole formation.

T-Micro

Before adhesive injection

Before Si etching

Si etching

Si etching

After Si etching

Now Back side Al plating is being done

4. Summary

- SOI technology has many good features; low power, large range of operating temperature, low single event effect, vertical integration, ...

- SOI Pixel process becomes more stable and practical to use. Most of the technical problems are solved.

- We have ~twice/year regular MPW runs with increasing no. of users (Next MPW run is Oct. 3rd).

- Many pixel sensors are working and showing good performance.

- The process is still progressing; Higher resistivity, Nested well structure, Double SOI, Larger mask size, Stitching, …

- We welcome new users to the SOI pixel process.