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Part I

SOI

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SOI PROJECT

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Contents:

1. Introduction 3
2. SOI Pixel Process 4
2.1 Wafer Process 4
2.2 Back Gate Effect & BPW 5
2.3 Sensor Layers 6
2.4 High Resistive Wafer 7
2.5 Leakage current 9
2.6 Multi Project Wafer Run 10
2.7 Stitching 11
3. Detector Developments 12
3.1 SEABAS Readout Board 12
3.2 Integration Type Pixel Detector (INTPIX) 13
3.3 X-ray Detector for Astrophysics (XRPIX) 15
3.4 XFEL Detector (SOPHIAS) 17
3.5 Vertex Detector (PIXOR) 18
3.6 Low Temperature Applications 19
3.7 Other Detector R&Ds 21
4. Advanced R&Ds 23
4.1 Double SOI 23
4.2 3D Vertical Integration 26
5. Data Base 29
5.1 Development History 29
5.2 Collaboration Members 29
5.3 Master Thesis 32
5.4 Publications 33
5.5 External Fundings 37
5.6 Patents 37
6. References 37

1. INTRODUCTION

The Silicon-On-Insulator (SOI) pixel R&D [i] is targeting to develop monolithic pixel detectors for future high-energy physics experiments, X-ray experiments, and other applications. It integrates both radiation sensors and LSI circuits in one chip, and achieve high-resolution and intelligent detectors.

Fig. 1 shows the schematic view of the SOI pixel detector (SOIPIX). The SOI wafer is composed of a thick, high-resistivity substrate (sensor part) and a thin low-resistivity Si layer (CMOS circuitry) sandwiching a buried oxide (BOX) layer. After removing the top Si and the BOX layer in the region of the sensing node contacts, p or n dopant is implanted to the substrate. Then contact vias and metal connections from the p-n junction to the transistors are created. The main advantages of the SOI detectors are;

- There is no mechanical bump bonding, so obstacles, which will cause multiple scattering, are eliminated and smaller pixel size is possible.
- Parasitic capacitances of sensing nodes are very small (~10fF), so large conversion gain and low noise operation are possible.
- Full CMOS circuitry can be implemented in the pixel.
- The cross section of single event effects caused by radiation is very small. A latch-up mechanism, which destroys conventional bulk CMOS LSI, is absent.
- Unlike conventional CMOS process, there is no leakage path to bulk. Thus SOI transistors are shown to work over a very large temperature range from 4K to 600K.
- The technology is based on industry standards, and one of most promising technology for future LSIs. Thus further progress and lower cost are foreseeable.
- Emerging vertical (3D) integration techniques are a natural extension of the SOI technology, so a much higher integration density is possible.

We have started this R&D in 2005 by collaborating with Lapis Semiconductor Co. Ltd (see 5.1 Development History). Our process is developed based on their 0.2 μm CMOS fully-depleted (FD-) SOI process [ii].

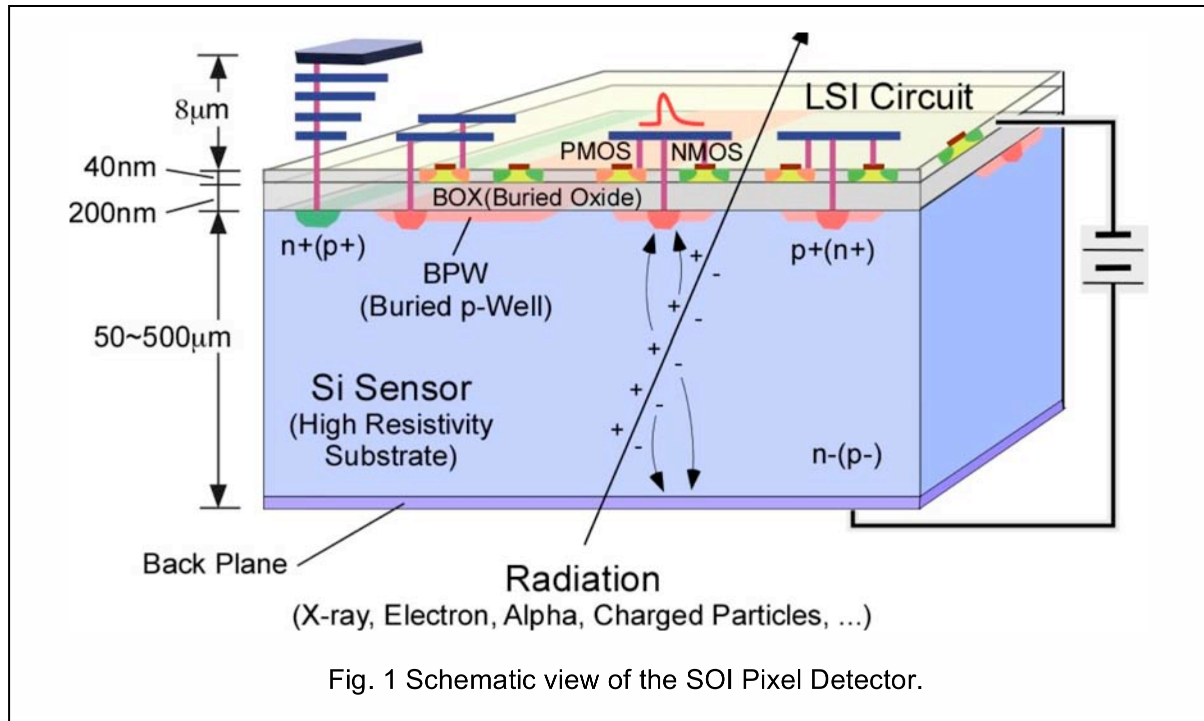


Fig. 1 Schematic view of the SOI Pixel Detector.

2. SOI PIXEL PROCESS

2.1 Wafer Process

Main specifications of the process are summarized in Table 1. We have been trying several kinds of high-resistivity wafers (CZ and FZ) for both n- and p-type wafers (see 2.4 High Resistive Wafer). To reduce development cost, we called academic sectors to join our MPW runs (see 2.6 Multi Project Wafer Run). The process has 5 layers of metal and can be implement MIM capacitor located on 3rd metal (Fig. 2) [iii].

Table 1. SOI pixel process specifications.

Process	0.2μm Low-Leakage Fully-Depleted SOI CMOS, 1 Poly, 5 Metal layers, MIM capacitor (1.5 fF/um2), DMOS option. Core (I/O) Voltage = 1.8 (3.3) V
SOI wafer	Diameter: 200 mmϕ, Top Si: Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: 720 μm thick. Cz(n) ~ 700 Ω-cm, FZ(n) ~ 7kΩ-cm, FZ(p) ~ 25 kΩ-cm, etc.
Backside	Thinned to 100 ~ 500 μm by mechanical grind, and chemical etching. Then adequate impurity is implant, laser Annealed, and Al is plated (200 nm).
Transistors	Normal and low threshold transistors are available for both core and IO transistors. Three types of structures (body-floating, source-tie and body-tie) are available.
Optional process	Buried p-well formation Vertical integration with μ-bumps.

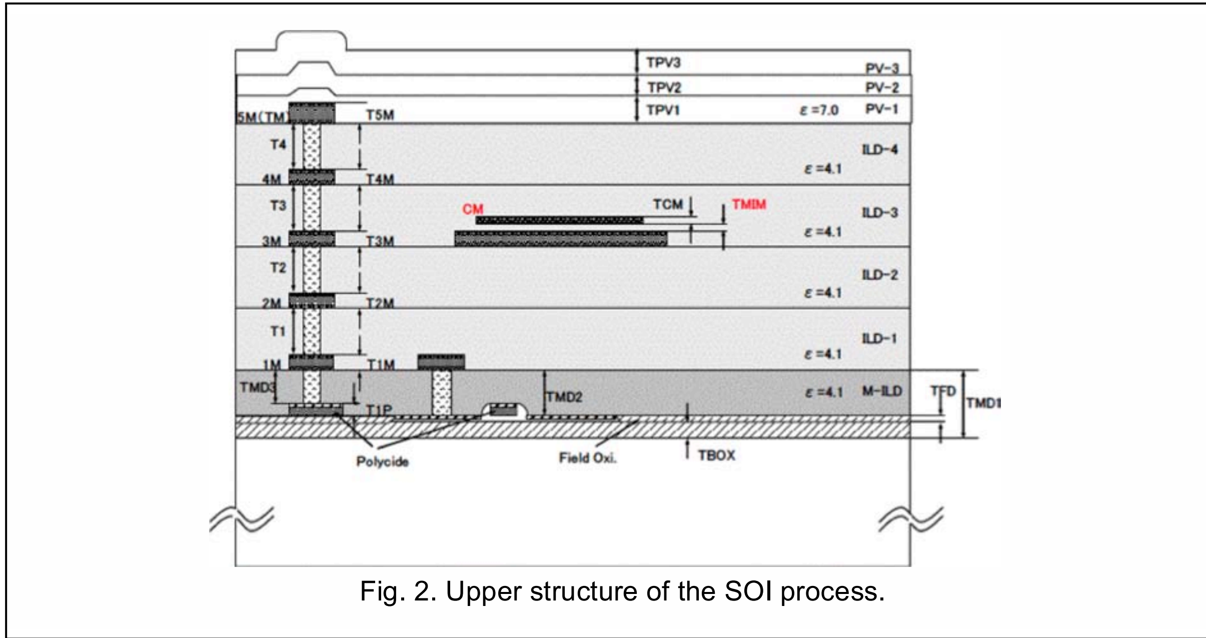


Fig. 2. Upper structure of the SOI process.

2.2 Back Gate Effect & BPW

One of the major difficulties to build a radiation sensor in SOI wafer is the back gate effect. Since the sensor and the transistors are located very near (~200 nm), transistors become ON when high voltage is applied to the sensor (Fig. 4-a). To shield the electric field of the transistors from the sensor voltage, we developed Buried Well (BW) process. We implant p(n)-type dopant without removing the top Si layer to create a buried p(n)-well region (BPW(BNW)) under the BOX. As shown in Fig. 4, leakage current of transistors becomes very high at the back side voltage of above 10V if there is no BPW layer. However, the transistor characteristic does not change at 100V by introducing the BPW layer. (Actually there is no back gate effect seen even more than 200V).

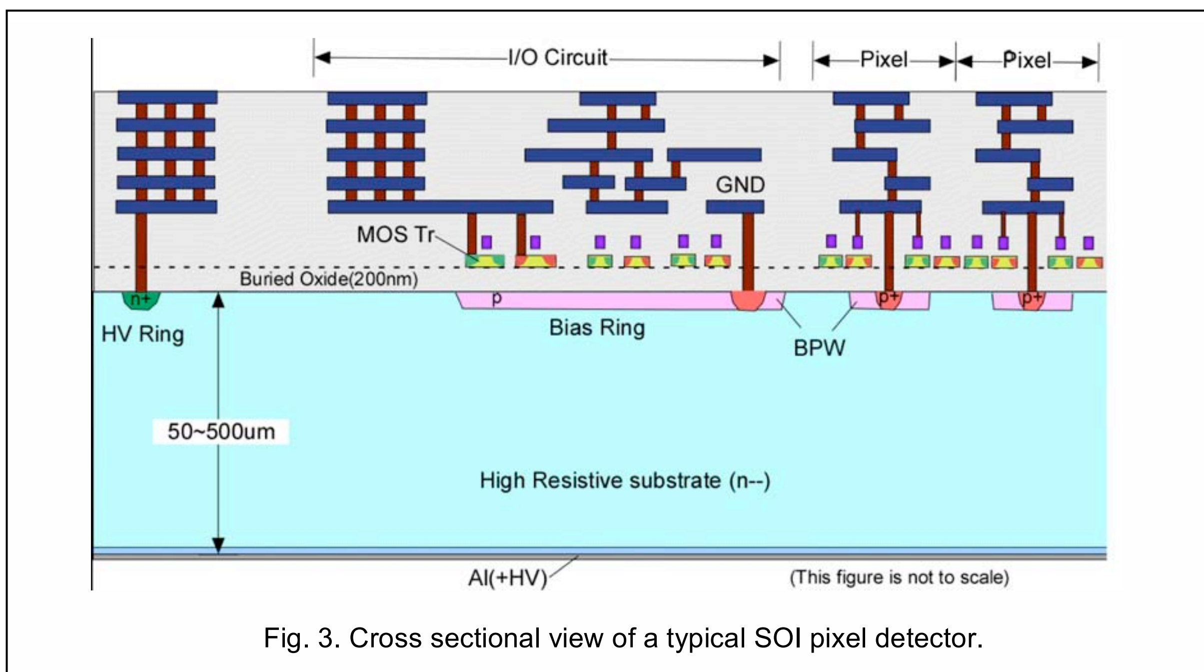


Fig. 3. Cross sectional view of a typical SOI pixel detector.

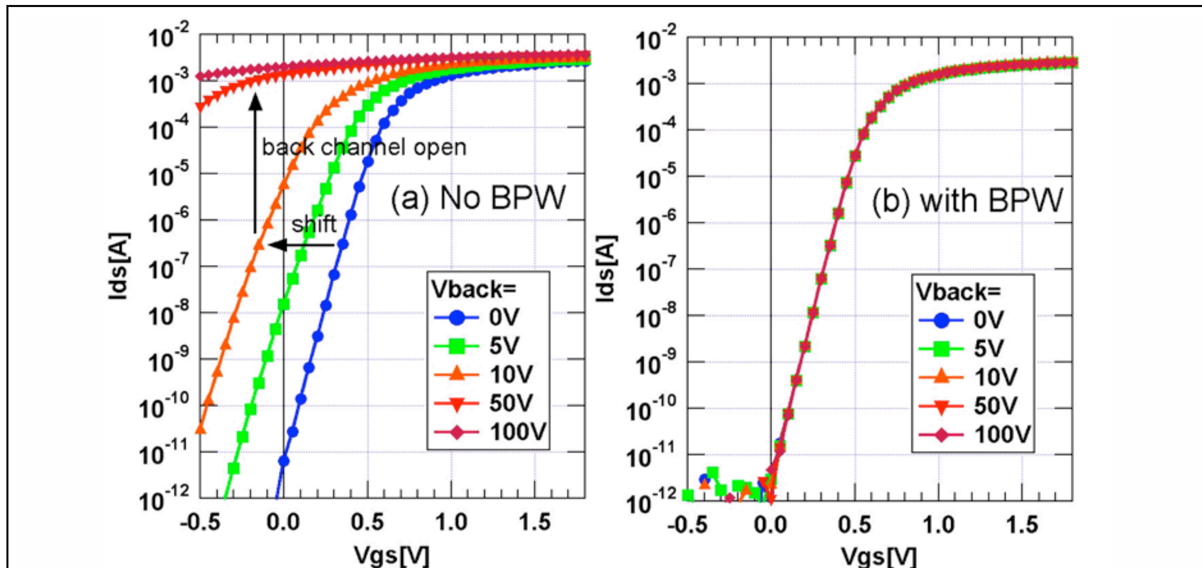


Fig. 4. NMOS transistor Ids-Vds curve and back side voltage. (a) Without BPW layer, (b) with BPW layer connected to ground. By introducing the BPW layer, the back gate effect is fully suppressed.

2.3 Sensor Layers

After introducing the BPW/BNW layers successfully, several structures that require additional layers were proposed and introduced. Fig. 5 shows present possible layers under the BOX. PS and NS layers are high-density implant region to create p+ and n+ region and contact to metal layer. These implant will be done after removing top Si and SiO2 layers.

BP3 is same mask layer used in the BPW, and is used when deeper implant is required. BP2 is deepest buried layer to create nested structure with the BNW.

We are using same layout both for n-type and p-type substrate. Therefore, when we process p-type substrate p-implant and n-implant are reversed. Thus, in p-type substrate, BPW mask is used for buried n-well, and BNW mask is used for buried p-well and so on.

As for the backside of the wafer, following processes are done normally.

i) Mechanical grind to desired thickness,

ii) Wet etching by 40um,

iii) Implant of n (p) dopant to n(p)-substrate (depth ~ 0.5um),

iv) Aluminum plating (~200 nm).

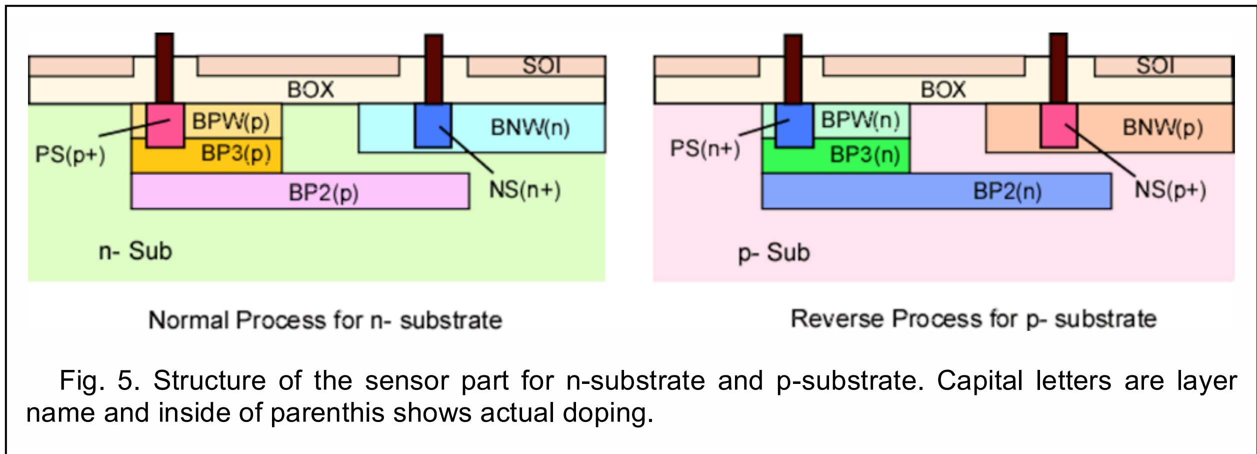


Fig. 5. Structure of the sensor part for n-substrate and p-substrate. Capital letters are layer name and inside of parenthis shows actual doping.

2.4 High Resistive Wafer

We have been mainly using high resistive SOI wafer from standard products of SOITEC Co. The handle wafer is made in Czochralski (Cz) method (called HR1 wafer), which is n-type and has about 700 Ohm•cm resistivity. However, it is desirable to get much higher resistivity to create thicker depletion depth with lower voltage. We asked SOITEC to make special SOI wafer by bonding with Floating Zone (FZ) wafer. That FZ wafers was supplied from us since it is not easy to get 8" FZ wafer.

To do CMOS process on FZ wafer is not easy task since CMOS high temperature process will cause slips in the wafer (Fig. 6 center). After careful tuning of the high temperature process, we succeeded to process FZ-SOI wafer without major slips (Fig. 6 right).

Fig. 7 shows leakage current vs. depletion depth for different wafers. FZ(n) and FZ(p) wafers of 500um thick become full depletion with 112V and 55V respectively, while Cz(n) wafer needs 237V to deplete 260um thick wafer.

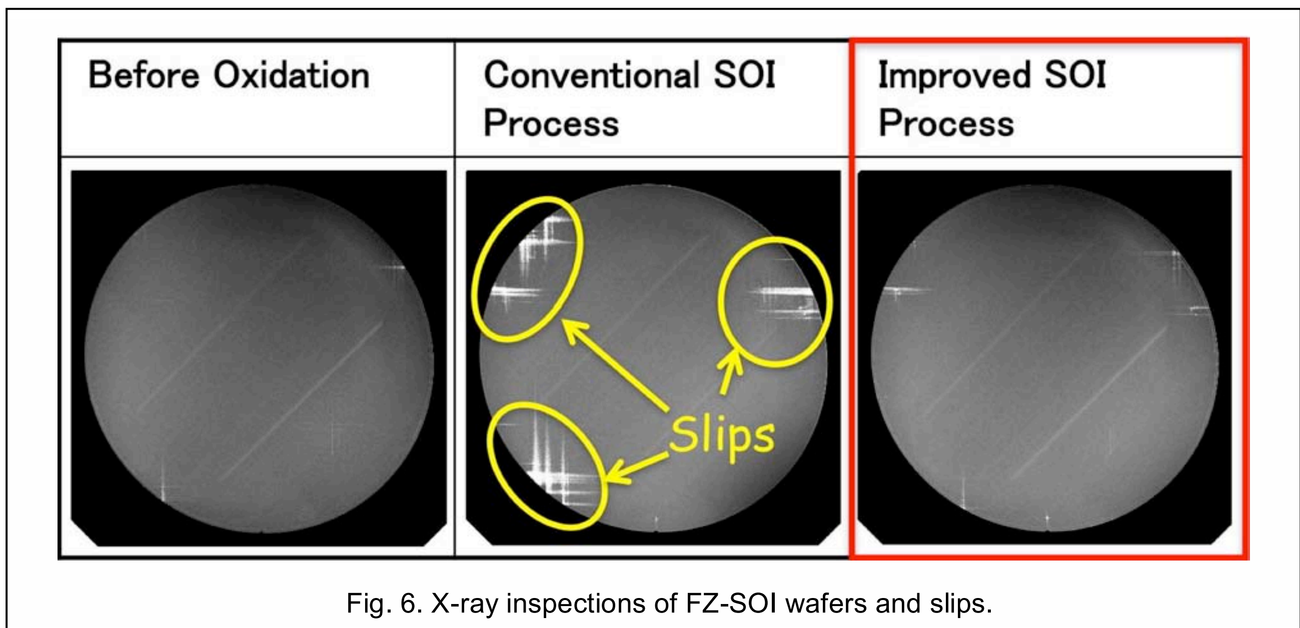


Fig. 6. X-ray inspections of FZ-SOI wafers and slips.

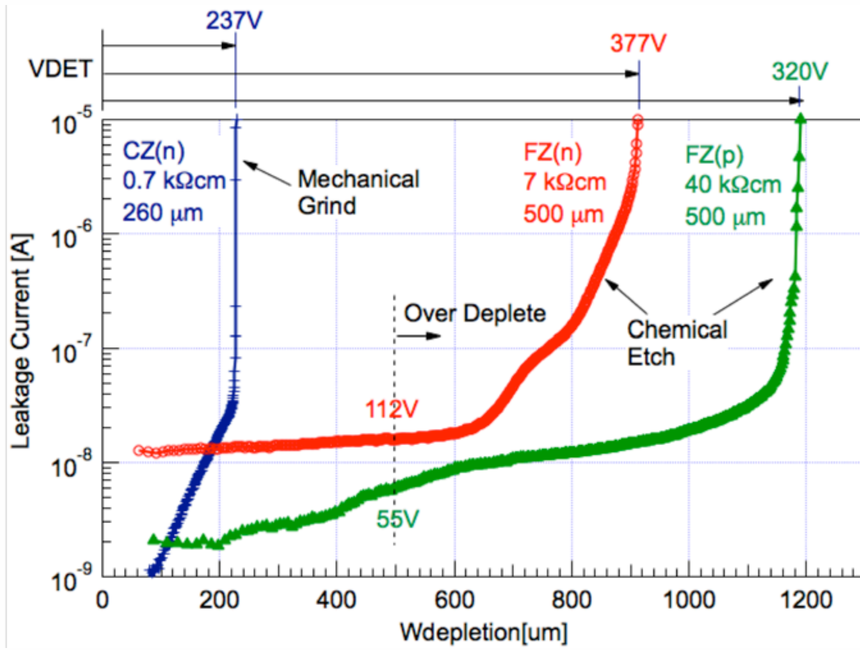


Fig. 7. Leakage current and depletion width of INTPIX3e chip for different kinds of wafers. Backside of the Cz(n) wafer is mechanical grind only, while the FZ(n) and FZ(p) wafers are chemical etching is

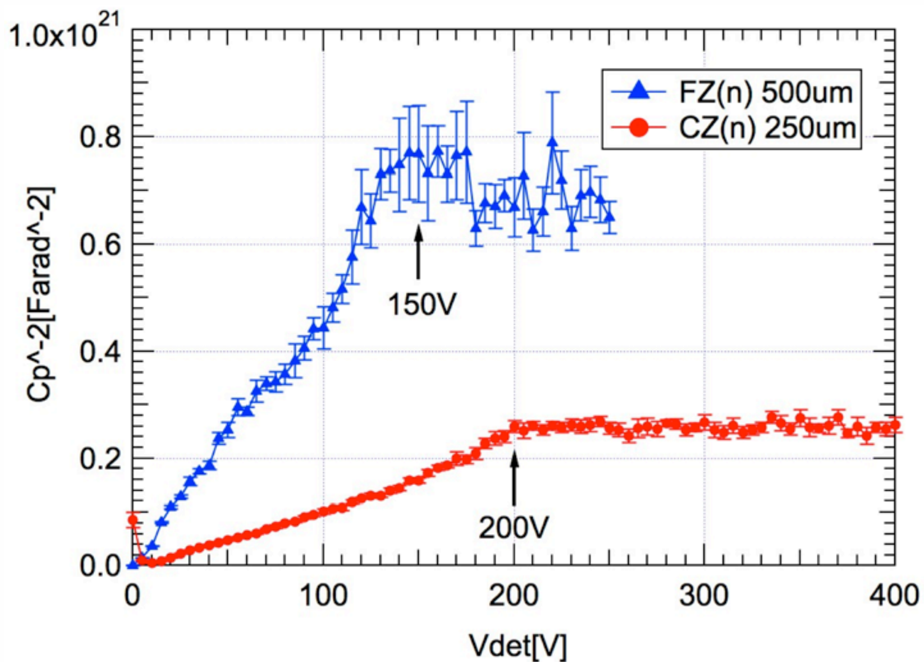


Fig. 8. $1/C^2$ plot of the INTPIX4 detector measured at 1kHz. Calculated resistivity from the corner voltage is 6.0 kOhm•cm and 1.1

2.5 Leakage current

While leakage current of the sensor is not so important for short integration time applications, it is important for long integration time applications such as astronomical X-ray observation and measurements that require good energy resolution.

Table 2 shows leakage current of a few detectors. CZ(n)(=HR1) wafer shows relatively large leakage current (> 100nA/cm^2@Room Temp.), while FZ(n) wafer shows better leakage current (10nA/cm^2@20ºC). Fig. 9 shows temperature dependence of the XRPIX1 leakage current. By lowering temperature, leakage current will decrease but become constant below -20 ºC. We have not yet identified the source of the constant leak curent.

Table 2. Summary of leakage current @Vdet=10V.

Chip/TEG	Wafer	Temp.	Leakage current
XRPIX1	Cz(n)	25 ºC	440 nA/cm2
XRPIX1	Cz(n)	-50 ºC	0.3 nA/cm2
XRPIX1	FZ(n)	20 ºC	10 nA/cm2
XRPIX1	FZ(n)	-20 ºC	0.1 nA/cm2
MAMBO IV (nested well)	FZ(n)	Room T	<100 nA/cm2
INTPIX/CNTPIX	Cz(n)	Room T	100~300 nA/cm2

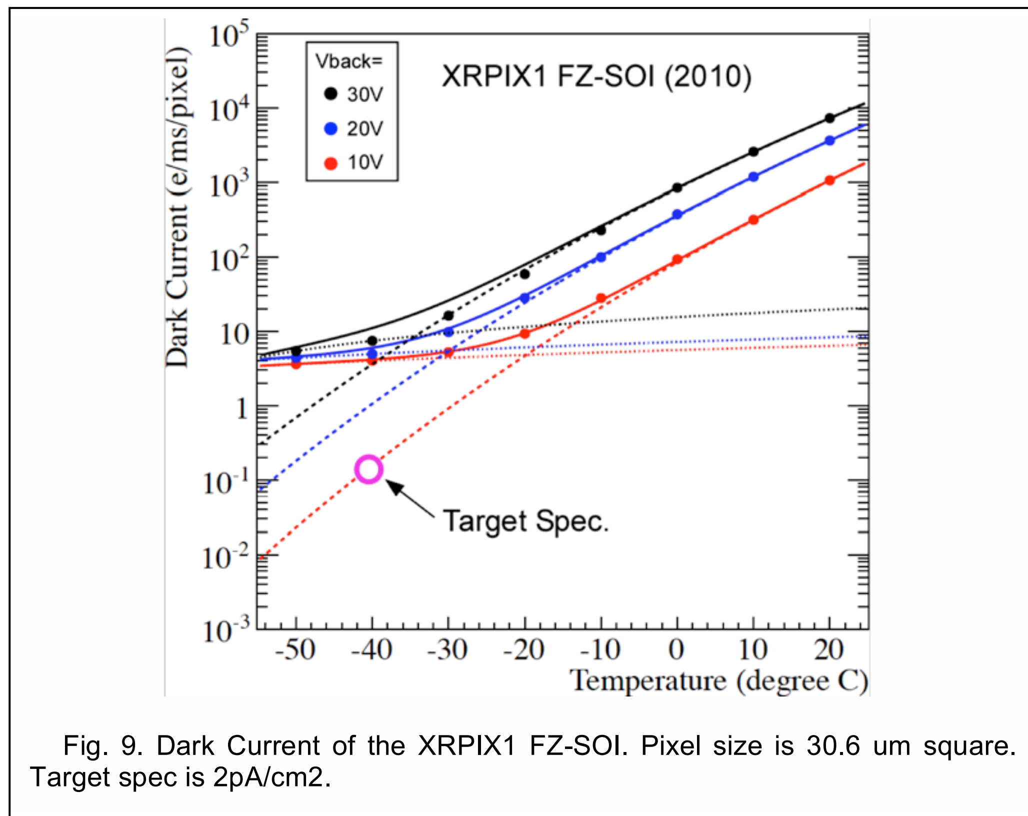


Fig. 9. Dark Current of the XRPIX1 FZ-SOI. Pixel size is 30.6 um square. Target spec is 2pA/cm2.

Fig. 10 shows Arrhenius plot of the XRPIX2b-Cz(n). Until full depletion occurs around 250V, the activation energy is about 0.55eV. This implies main source of the current comes from generation current in the depletion region. When full depletion achieved above 300V, activation energy decreases below 0.35eV. This implies back side surface is the source of the additional leakage current.

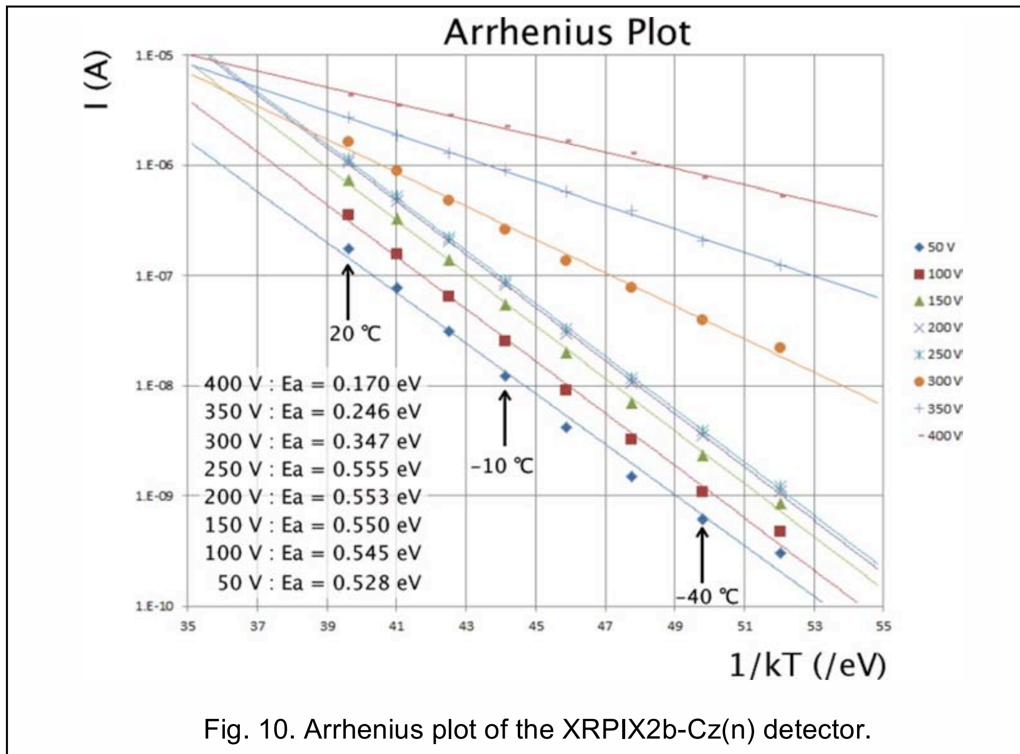


Fig. 10. Arrhenius plot of the XRPIX2b-Cz(n) detector.

2.6 Multi Project Wafer Run

The cost of semiconductor process is not cheap. Major part of the cost is mask set. To reduce development cost and have multiple chances for developments, we decided to operate this SOI pixel process as Multi Project Wafer (MPW) runs. In past a few years, we have been doing the MPW runs twice per year except year 2011 when large earthquake was occurred and Lapis semiconductor fab was damaged.

In addition to many Japanese institutes, we have been collaborating with US/Europe/Asian researchers through this MPW runs. Our present collaborator/user are listed in section 5.2 "Collaboration Member"

In 2011, we changed the mask size from 20.6mm x 20.6mm to 24.6mm x 30.8mm, so that we can accept more designs and build larger detector Fig. 11.

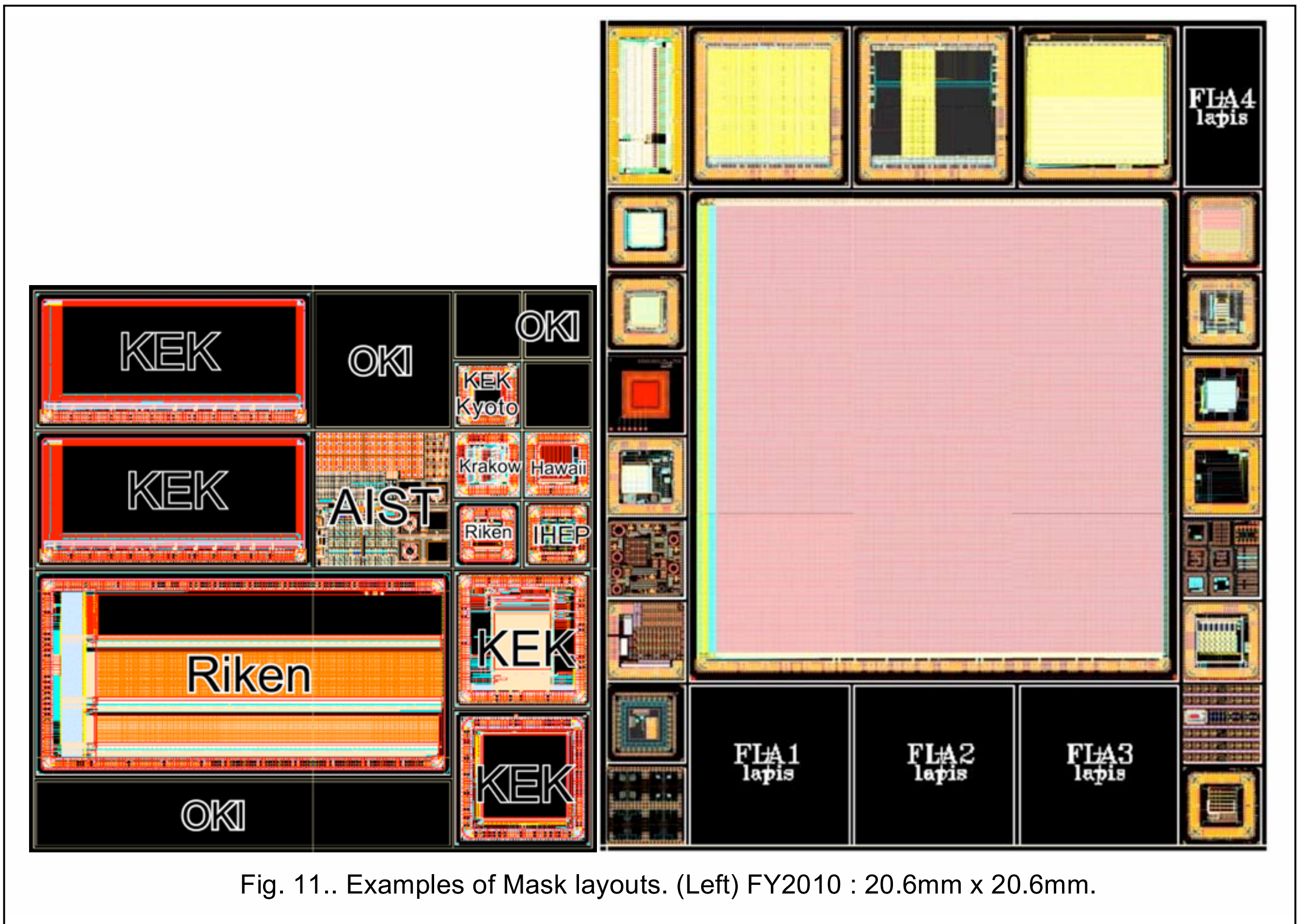


Fig. 11.. Examples of Mask layouts. (Left) FY2010 : 20.6mm x 20.6mm.

2.7 Stitching

Large area detectors are often required in some experiments, but the mask size is limited to 24.6mm x 30.8mm in size. Therefore, we have developed stitching technique to make large format detector by using only one mask set. Fig. 12 shows the stitching method and photographs of the processed wafer.

The development is mainly driven by Riken group for the SOPHIAS detector. Since this was our first trial, we took buffer region size of 10um and connect only minimum number of layers (PS, NS and metal 1). However, Lapis is confident to make buffer region shorter and connects all metals.

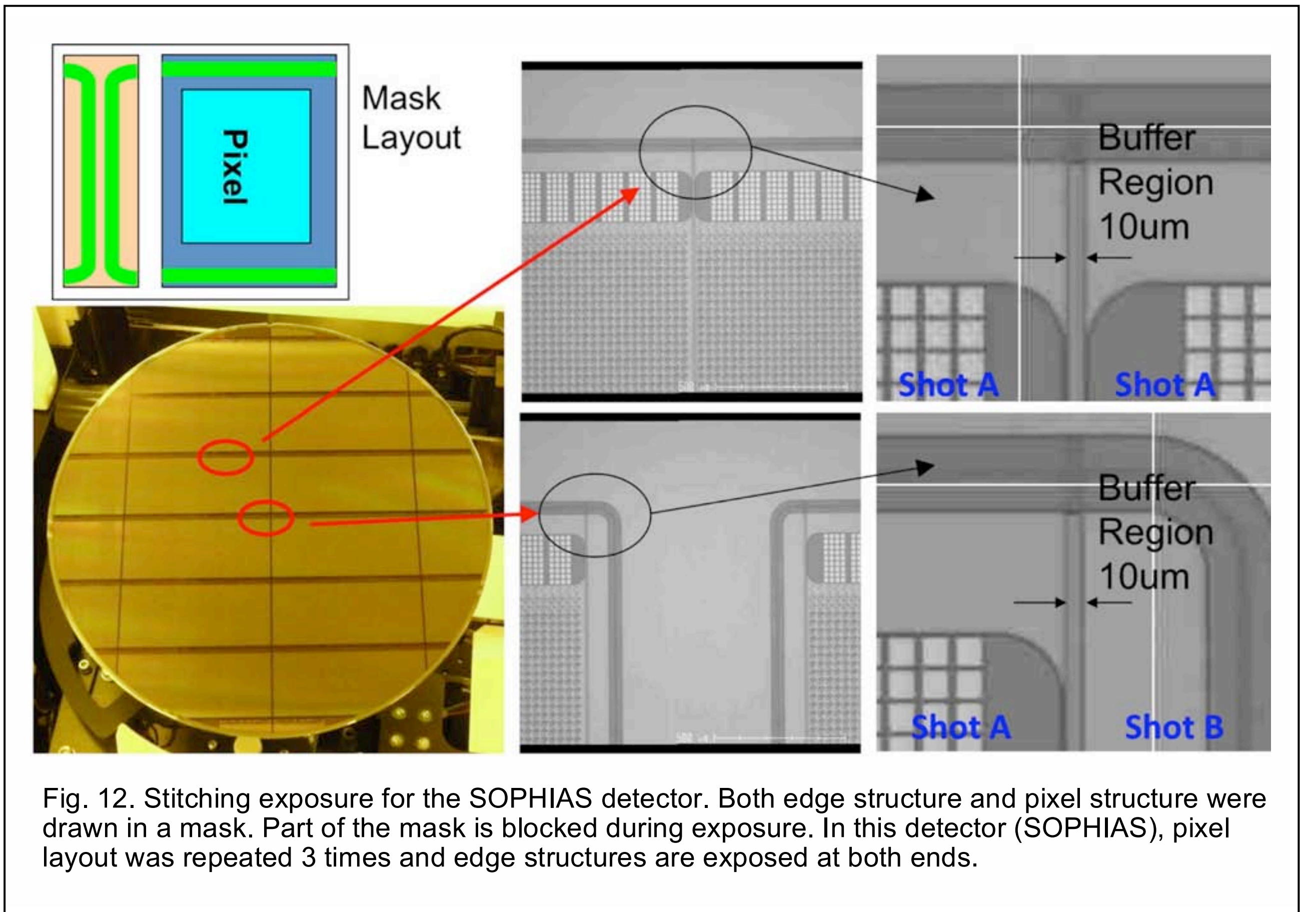


Fig. 12. Stitching exposure for the SOPHIAS detector. Both edge structure and pixel structure were drawn in a mask. Part of the mask is blocked during exposure. In this detector (SOPHIAS), pixel layout was repeated 3 times and edge structures are exposed at both ends.

3. DETECTOR DEVELOPMENTS

There are many activities of detector developments using the SOI pixel process. In this section, we flash major activities of the developments.

3.1 SEABAS Readout Board

To test manufactured chip quickly, we have developed SEABAS (SOI EvAluation BoArd with Sitcp) read out board. The board contains two FPGAs one for controlling the SOI pixel and the other is for transferring the data through Ethernet (called SiTCP).

Fig. 13 and Fig. 14 show block diagram and photograph of the SEABAS2 (2nd generation board) respectively. By using the SEABAS2 board, we could take ~70 frame/sec with INTPIX4 detector (425k pixels).

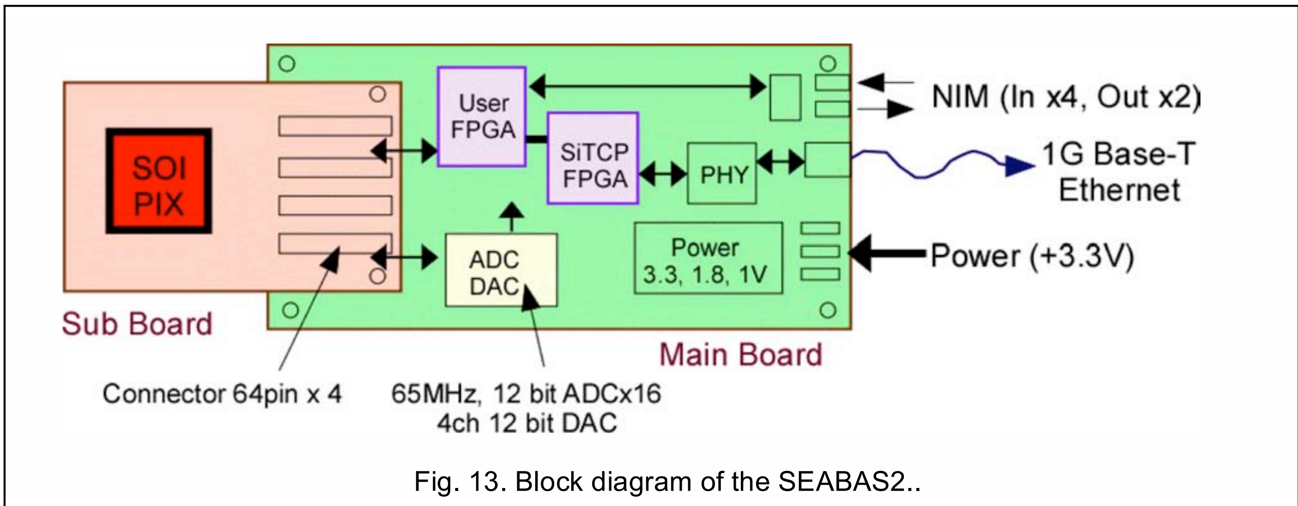


Fig. 13. Block diagram of the SEABAS2..

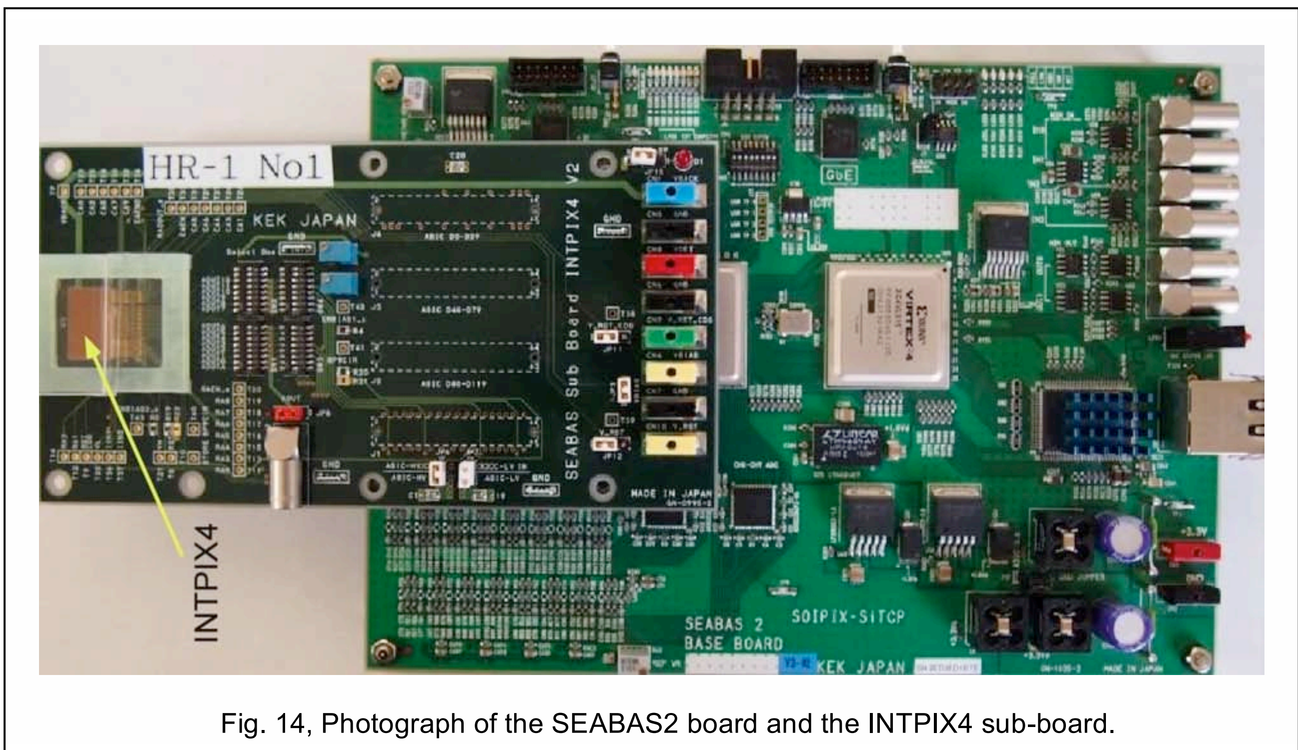


Fig. 14, Photograph of the SEABAS2 board and the INTPIX4 sub-board.

3.2 Integration Type Pixel Detector (INTPIX)

Main SOI detectors developed so far are integration-type pixel detectors. The basic schematic of the sensor and a layout are shown in Fig. 15. The circuit is similar to that of the CMOS optical imager. Smallest size of the pixel we have developed is 8 μm square. Many of the integration-type pixels have correlated double sampling (CDS) circuit in each pixel or in column circuit. Largest chip (INTPIX5/6) so far tested has 896 x 1408 (~1.3 M) pixels, and new chip (INTPIX7) under process has 1408 x 1408 (~2M) pixels. Specifications of major integration-type detector are summarized in Table 3.

An example of X-ray image taken by the INTPIX4 detector is shown in Fig. 16.

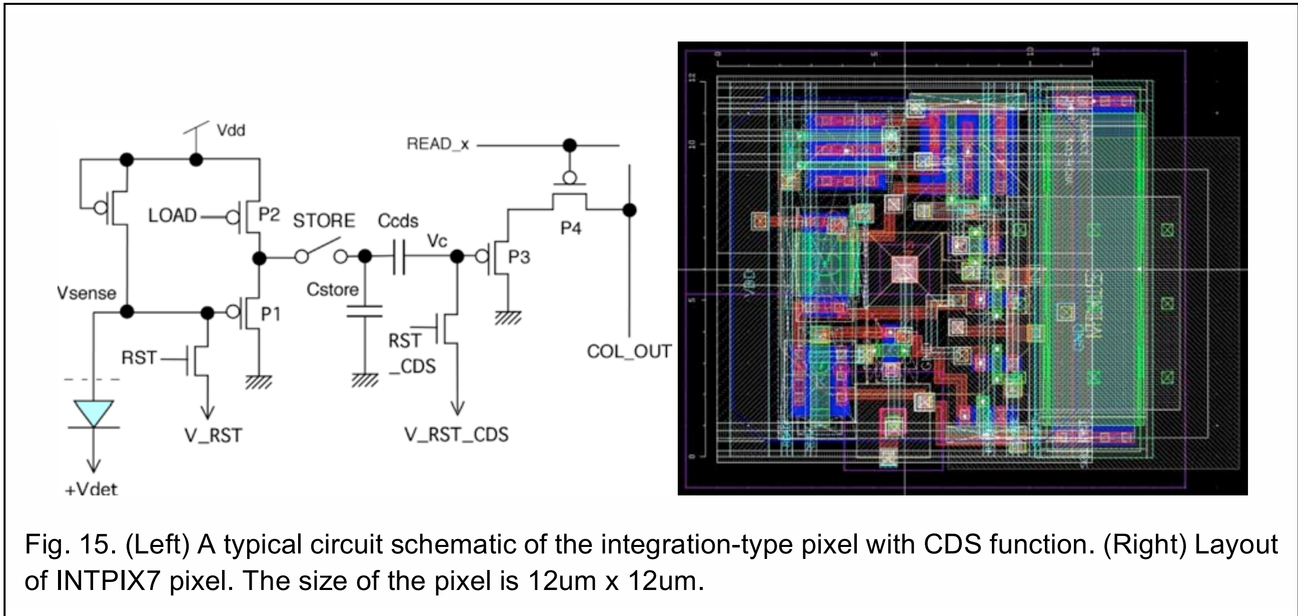
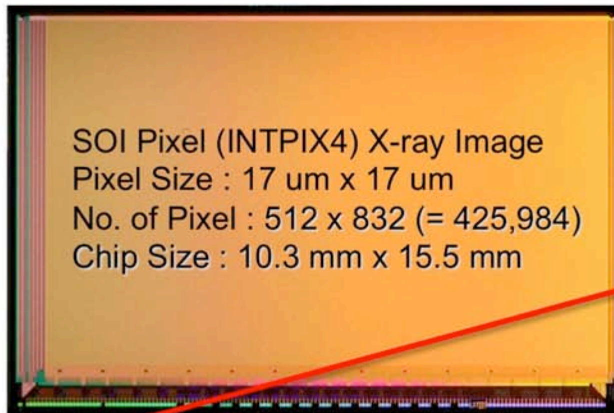


Fig. 15. (Left) A typical circuit schematic of the integration-type pixel with CDS function. (Right) Layout of INTPIX7 pixel. The size of the pixel is 12um x 12um.

Table 3. Specification of major integration-type pixel detectors.

	DIPIX1/2	FPIX1	INTPIX4	INTPIX5/6	INTPIX7 (under process)
Pixel Size [um]	14 x 14	8 x 8	17 x 17	12 x 12	12 x 12
Chip Size [mm]	5 x 5	6 x 6	10.2 x 15.4	12.2 x 18.4	18.4 x 18.4
BPW width [um]	10	6	12	9	9
CDS	Pixel CDS	-	Pixel CDS	Column CDS	Pixel CDS
Store Switch	O	-	O	O	O
Wafer	n or p	n and p	n	n and p (INT5) n or p (INT6N or P)	p (Double SOI)
Gain	Fix (9.3 uV/e-)	Fix (~28 uV/e-)	Fix (12.6 uV/e-)	2 gain (~16 or 2.5 uV/e-)	Fix
Max. Charge	~110 ke-	~40 ke-	80 ke-	~70 or 460 ke-	-
No. of Pixels	256 x 128 x 2 (~65 kpix)	512 x 512 (~260 kpix)	512 x 832 (~430 kpix)	896 x 1408 (~1,260 kpix)	1408 x 1408 (~1,982 kpix)
No. of Output	1	1 or 9	1 or 13	1 or 11	1 or 11
Rolling Shutter	-	O	-	O	O



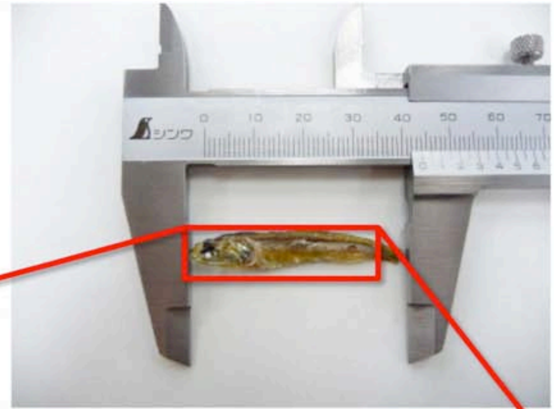
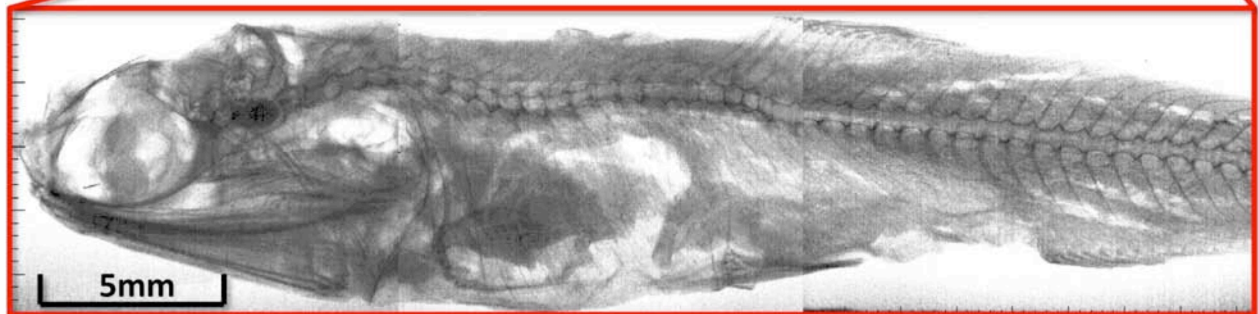



Fig. 16 An example of X-ray image (small fish) taken by the integration-type SOI sensor.

3.3 X-ray Detector for Astrophysics (XRPIX)

XRPIX detector [iv] has been developed for X-ray astronomical satellite by Kyoto Univ. and KEK/SOKENDAI member. Basic structure of the detector is same as that of the integration type detector, but it also has trigger generation function. By combining the trigger function and active shield system, background event caused by charged particles can be removed (Fig. 17).

In addition to source-follower type pixel used in the INTPIX, we have also developed Charge Sensitive Amplifier (CSA) type pixel recently. Fig. 17 shows energy spectrum of ^{55}Fe X-rays taken by the XRPIX CSA pixel. CSA type pixel shows much better resolution compared to source follower type, and achieved noise level of 33 e- while source follower type has 76 e- noise level.

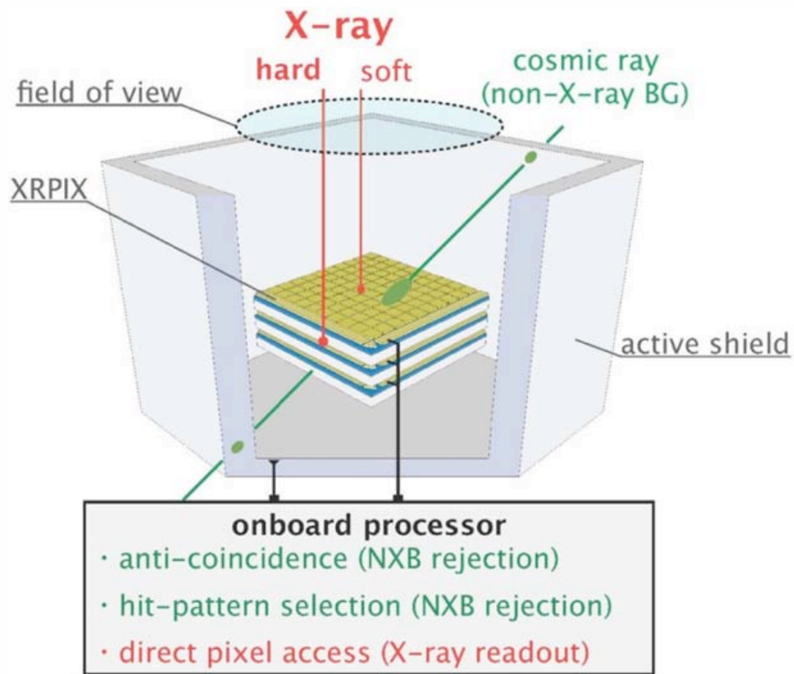


Fig. 17 Concept of an active shield system with the XRPIX. Non-X-ray background can be rejected by anti-coincidence with the active shield (scintillation counters).

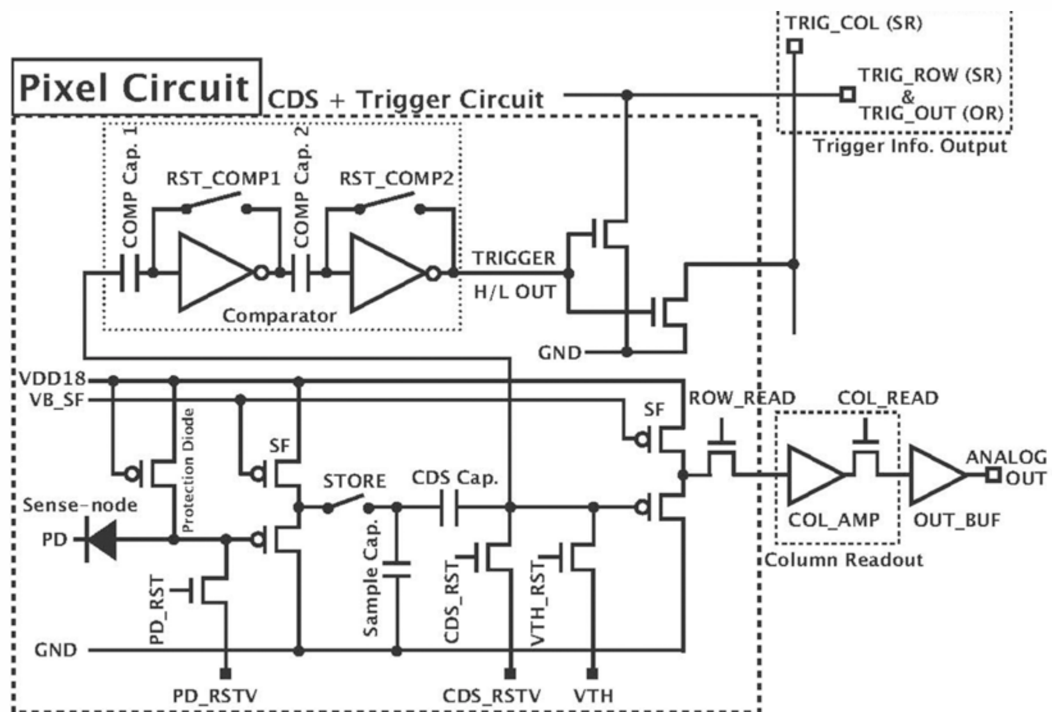


Fig. 18 Block diagram of the XRPIX detector.

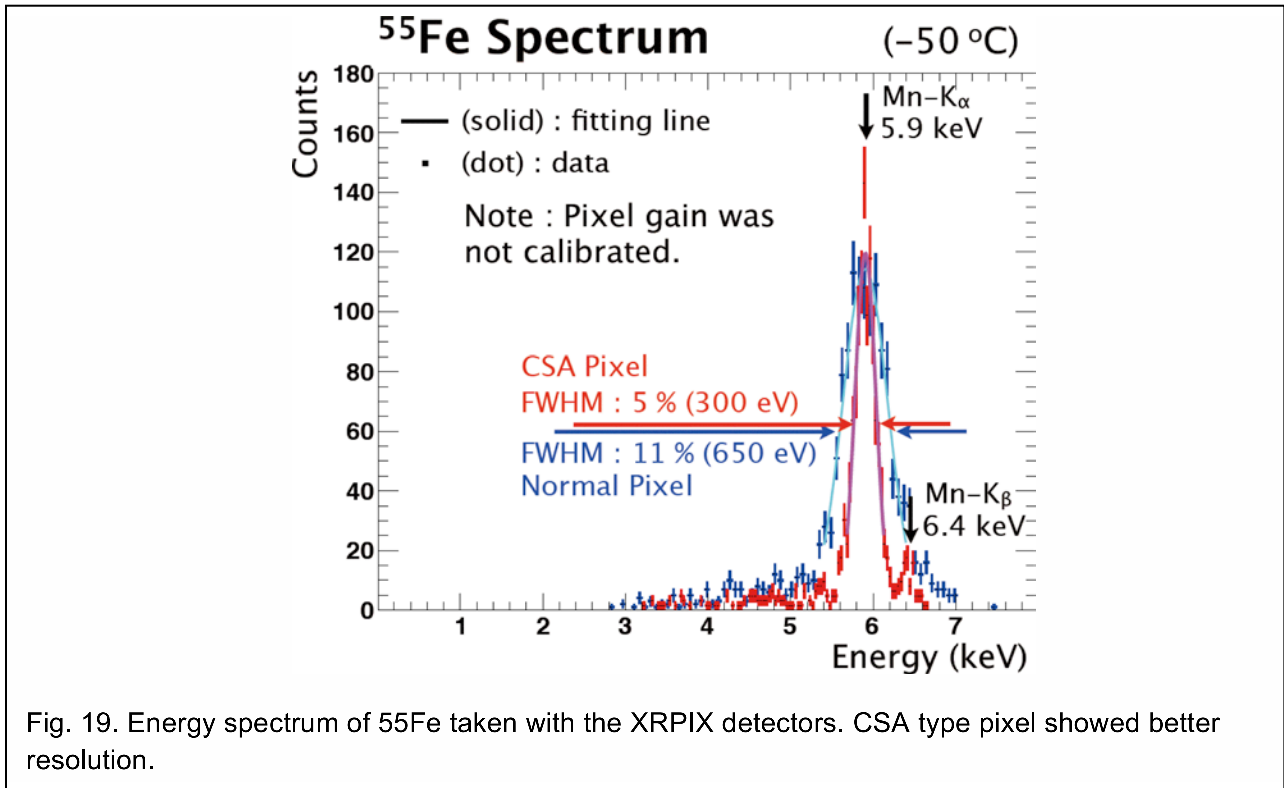


Fig. 19. Energy spectrum of 55Fe taken with the XRPIX detectors. CSA type pixel showed better resolution.

3.4 XFEL Detector (SOPHIAS)

A large dynamic range X-ray image Sensor has been developed for X-ray Free-electron Laser Facility, SACLA. The detector is named SOPHIAS (Silicon-On-Insulator PHoton Imaging Array Sensor) and developed by Riken group [v]. The sensor consists of 1.9 M pixels with 30 um pixel square shape. The single layer sensor give 40 % quantum efficiency at 20 keV X-ray photons with 500um thick handle wafer.

Each pixel has high and low gain channels to achieve large dynamic range. The different gain is achieved by different value of the input capacitance and different number of sensor nodes (Fig. 20). To fabricate larger detector than mask size, stitching technique is developed and used (see 2.7 Stiching).

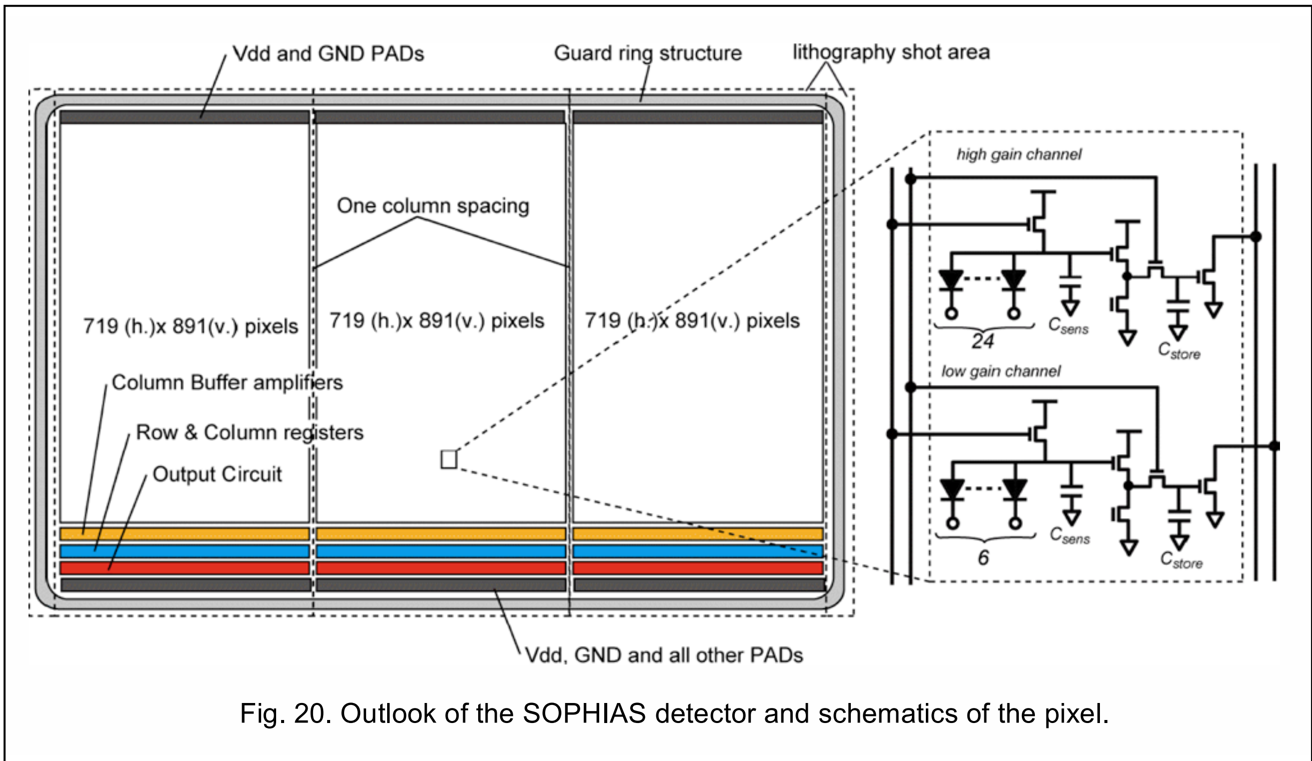


Fig. 20. Outlook of the SOPHIAS detector and schematics of the pixel.

3.5 Vertex Detector (PIXOR)

As an R&D for future vertex detector for Belle II experiment, a new detector PIXOR (PIXel OR) is being developed by Tohoku Univ. group [vi]. An analog signal from each pixelated sensor is divided into two-dimensional directions, and 2N signal channels from a small N-by-N pixel matrix are ORed as N column and N row channels (Fig. 21). Then the signals are processed by a readout circuit in each small matrix and wait for a trigger (Fig. 22).

This PIXOR scheme reduces the number of readout channels and avoids a deterioration of intrinsic position resolution due to large circuit area that was a common issue for monolithic detectors. This feature allows high resolution, low occupancy and on-sensor signal processing at the same time.

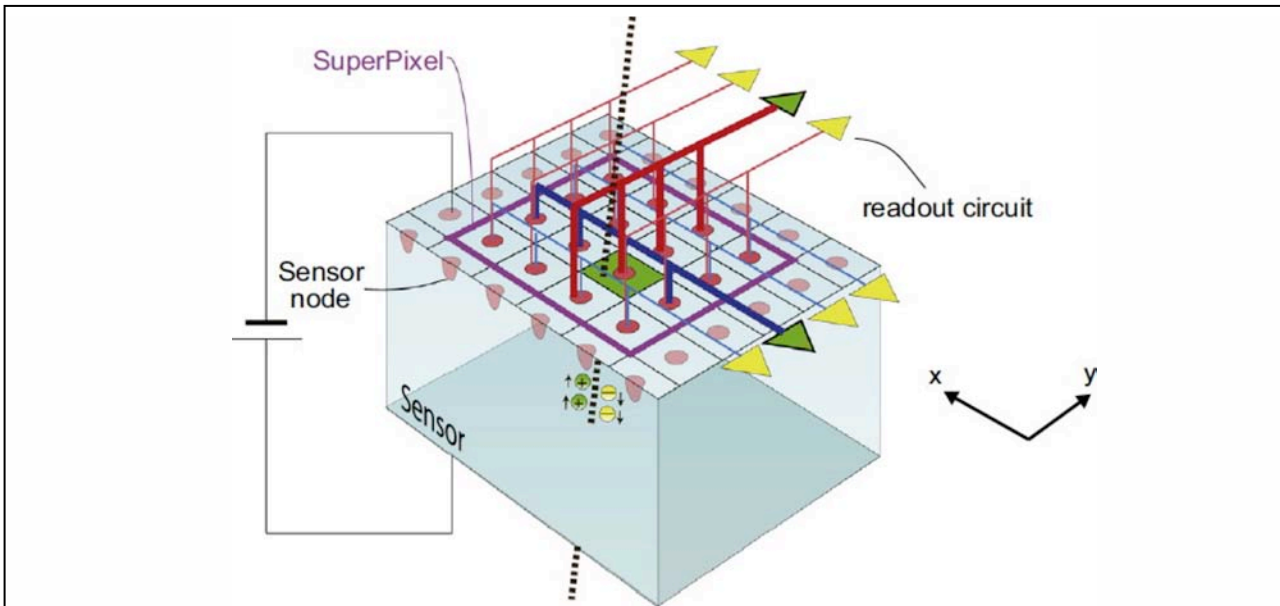


Fig. 21. Conceptual view of PIXOR (4x4 Super Pixel case). A charged particle penetrates the green pixel. The signal is divided into X(blue)/Y(red) directions. In this figure, readout circuit is not shown.

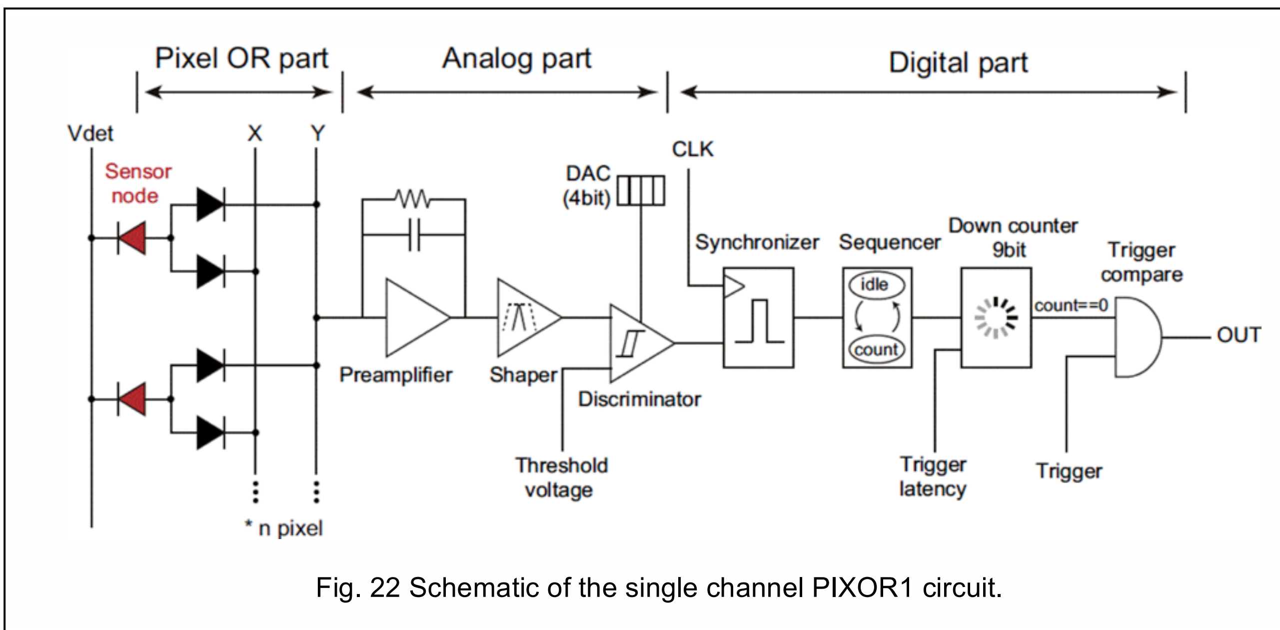


Fig. 22 Schematic of the single channel PIXOR1 circuit.

3.6 Low Temperature Applications

People in JAXA/ISAS have interest in using SOI devices in cryogenic temperature. They developed CMOS amplifiers and switches by using the SOI process, and confirmed to work without problem in low temperature where bulk CMOS devices cannot work. Typical performance of the amplifier is shown in Table 4.

Table 4. Performance of FD-SOI CMOS amplifier at 4.2K.

	design	measurement
Open loop gain	> 1000	> 7000
Power consumption	1.1 μW	1.3 μW
Output Voltage swing	> 1V	1.3 V
Input referred noise at 1 Hz	14-20 $\mu V/\sqrt{Hz}$	19 $\mu V/\sqrt{Hz}$
Input offset voltage	0 mV	2mV
Variation of input offset voltage	0 mV	4.2 mV(1σ)
Leak current of reset switch	0.1 fA	0.1 fA

After the success of the cryogenic operation, we started a project to build Superconducting Tunnel Junction (STJ) devices on processed SOI wafer with Univ. of Tsukuba group. When we want to arrange the STJ devices in array, extraction of STJ signals to room temperature is always annoying issue. If we succeed to build the STJ on processed SOI wafer and make good connections between them, number of the connection can be greatly reduced and S/N can be improved.

We have tested characteristics of SOI transistors at below 1K (Fig. 23). Both NMOS and PMOS show good performance. Then we build Nb/Al STJ device on top of the SOI wafer. The STJ devices successfully build and output signal is observed by illuminating laser light (465 nm) to the device (Fig. 24).

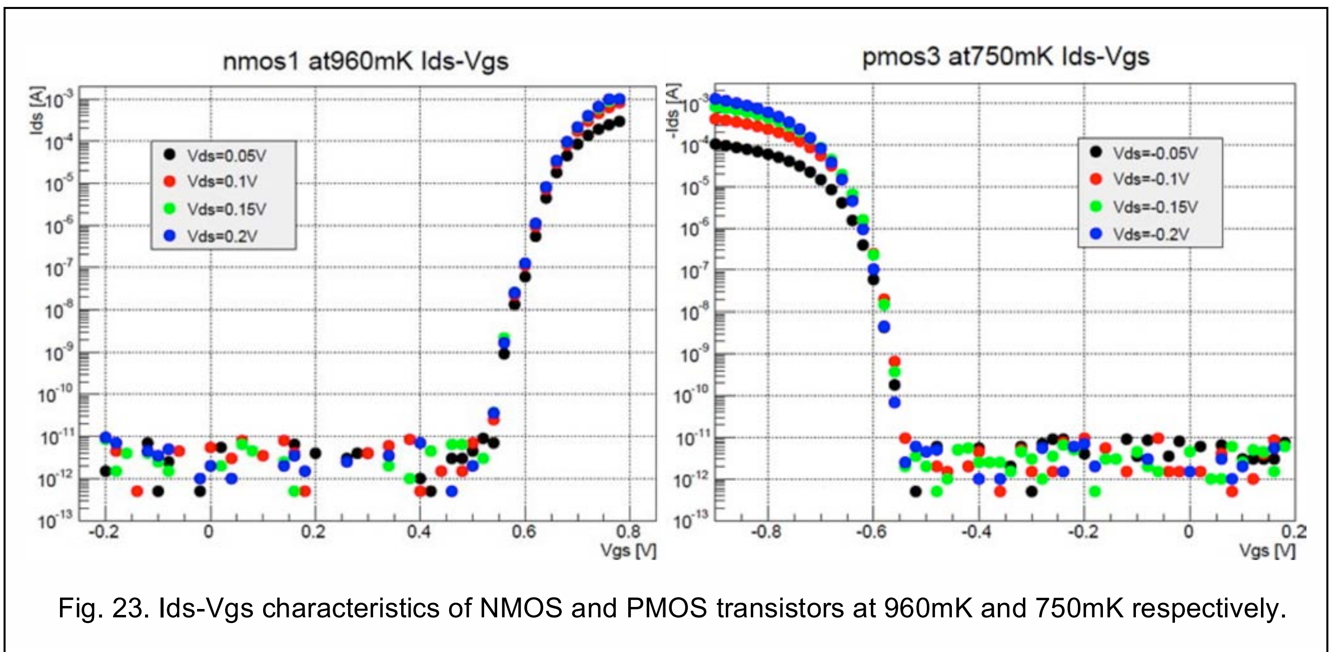


Fig. 23. Ids-Vgs characteristics of NMOS and PMOS transistors at 960mK and 750mK respectively.

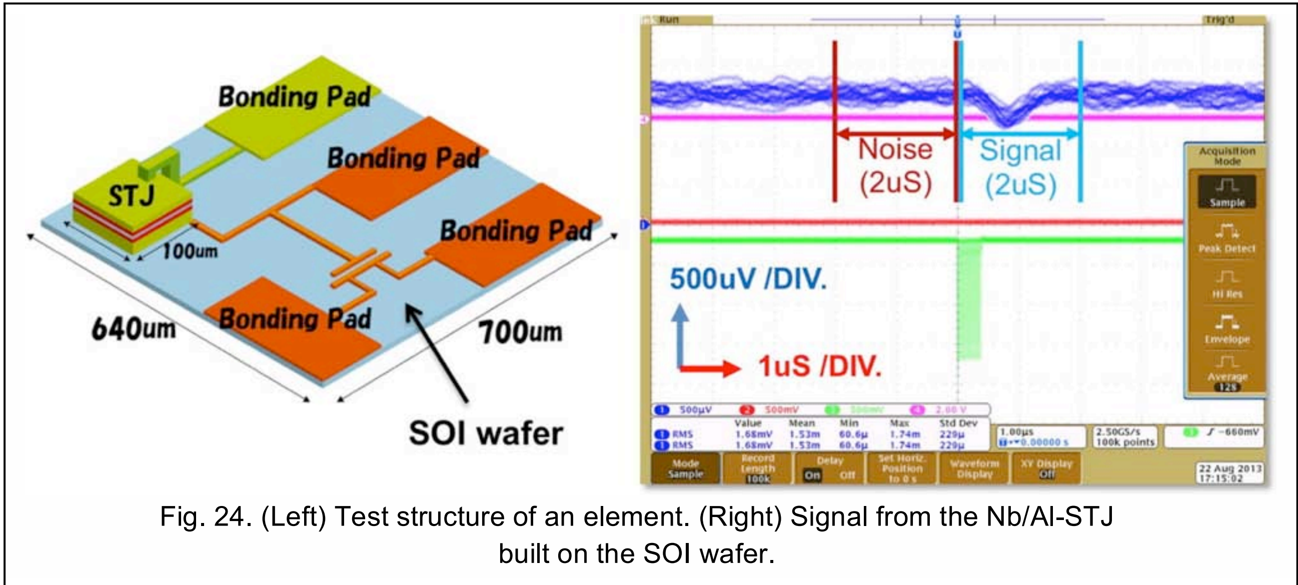


Fig. 24. (Left) Test structure of an element. (Right) Signal from the Nb/Al-STJ built on the SOI wafer.

3.7 Other Detector R&Ds

There are many other detectors R&Ds which are going on by using our MPW run.

Counting-type pixel (CNTPIX)

One of most important R&D for next step is development of counting type detectors. Schematic of the counting type pixel and its pixel layout are shown in Fig. 25. We already have test chips that show proper responses, but we also observe crosstalk between sensor and the circuits. Thus the development is postponed until double SOI technology is available (4.1 Double SOI).

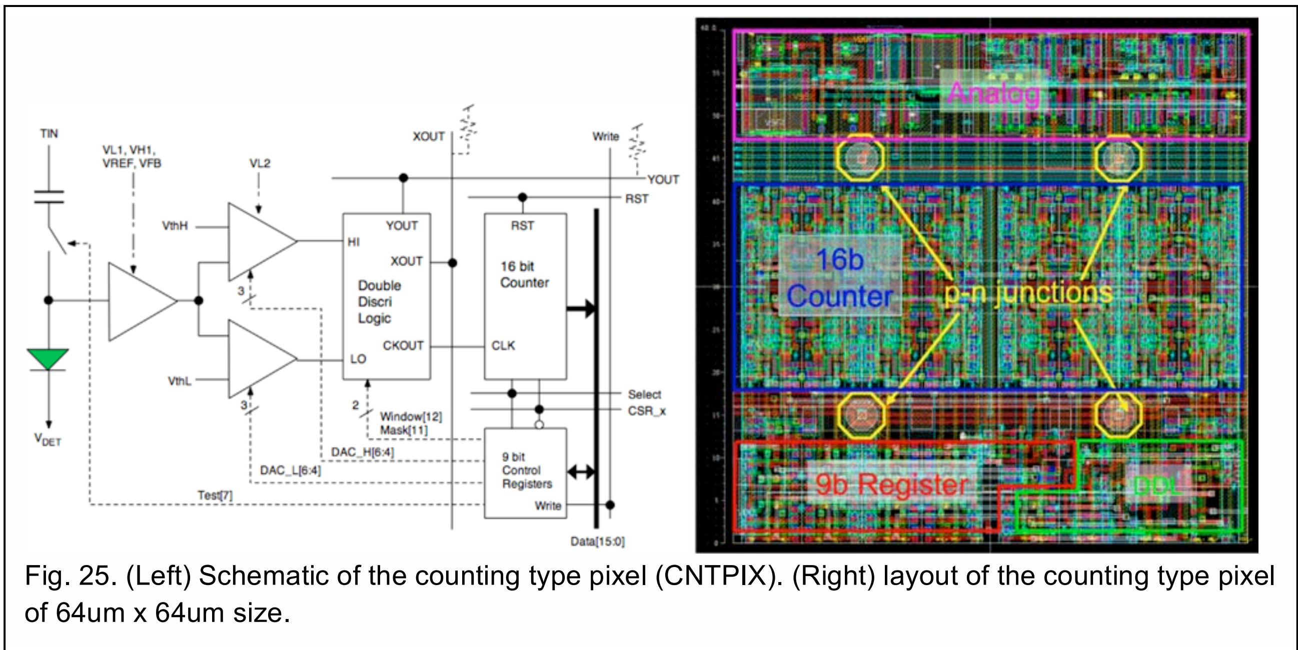


Fig. 25. (Left) Schematic of the counting type pixel (CNTPIX). (Right) layout of the counting type pixel of 64um x 64um size.

Detector for Imaging Mass Spectrometer (MALPIX)

Multi-Turn Time of Flight Mass Spectrometer (MULTUM) is being developed at Osaka Univ. as a compact and high performance mass spectrometer for next generation. It requires two-dimensional detector that can measure ion arrival timing in 1 ns resolution. Although it does not use sensor part of the SOIPIX, our pixel circuit can be utilized for this application. Then we started collaboration with Osaka group and developing a pixel detector called MALPIX. Ions from the spectrometer are converted to electrons by using Micro-Channel Plate (MCP), and a prototype detector was successfully tested.

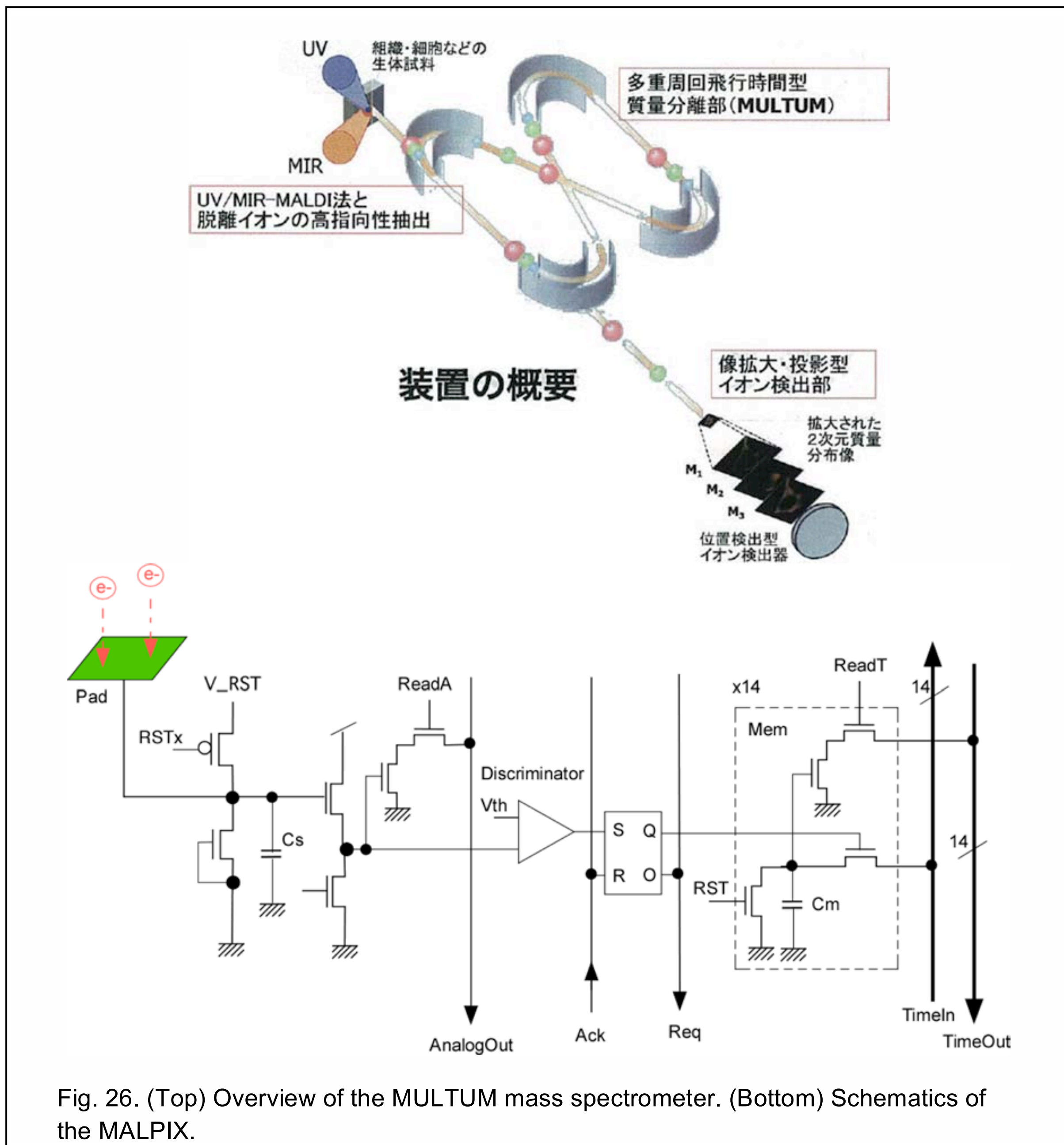


Fig. 26. (Top) Overview of the MULTUM mass spectrometer. (Bottom) Schematics of the MALPIX.

LHD pixel

To investigate inside of nuclear fusion plasma, measurement of X-rays from the inside of plasma gives valuable information. We have started collaboration with National Institute for

Fusion Science (NIFS) for measurement of Large Helical Device (LHD). First test is scheduled on Dec. 2013.

TDI pixel

X-ray detectors are used widely in many kinds of inspection system. Especially to find small metallic debris of ~10um size within battery has crucial demand in future electrical vehicles and so on. To find such small debris from materials on high-speed belt conveyor, SOIPIX is very suitable with its high resolution. However, to receive enough X-rays from moving object, Time Delayed Integration (TDI) method is mandatory. Although it is easy to implement the TDI in CCD device, it is difficult to do in CMOS device. We have invented a new method to implement digital TDI in the SOIPIX.

RADPIX

After the accident of the Fukushima nuclear power plant, people become very sensitive to radiations. Although SOIPIX does not have high efficiency for a few hundreds keV gamma rays, pixelated sensor has advantage to identify type of the radiation and detection of alpha and beta rays. Thus we are developing a pixel detector (RADPIX) for monitoring environmental radiation. It includes leakage current compensation circuit for continuous detection of radiation.

4. ADVANCED R&DS

4.1 DOUBLE SOI

While we solved the back gate problem by introducing BPW layer, there still remain two issues to make the SOIPIX used widely.

- Crosstalk between sensor node and circuit,
- Radiation tolerance of the detector.

The crosstalk generates unwanted signals and makes operation of the detector unstable. While the SOI is immune to Single Event Effect (SEE), it is not so rad-hard to Total Ionization Dose (TID) due to the BOX and surrounding oxide. Tolerable radiation level of present SOIPIX devices is about 2 kGy, and many applications require more than 10 kGy (1 Mrad) tolerance.

After all, to solve these issues, we need another conduction layer between sensor and circuit. We asked SOITEC to make double SOI wafer which has two sets of thin Si and BOX pair layers. General view of the double SOI pixel detector is shown in Fig. 27, and cross section of processed double SOI wafer is shown in Fig. 28. In addition to above two issues, the newly introduced middle Si layer (SOI2) shields back gate effect too (Fig. 29), so that we can optimize the size of the BPW without considering the back gate effect.

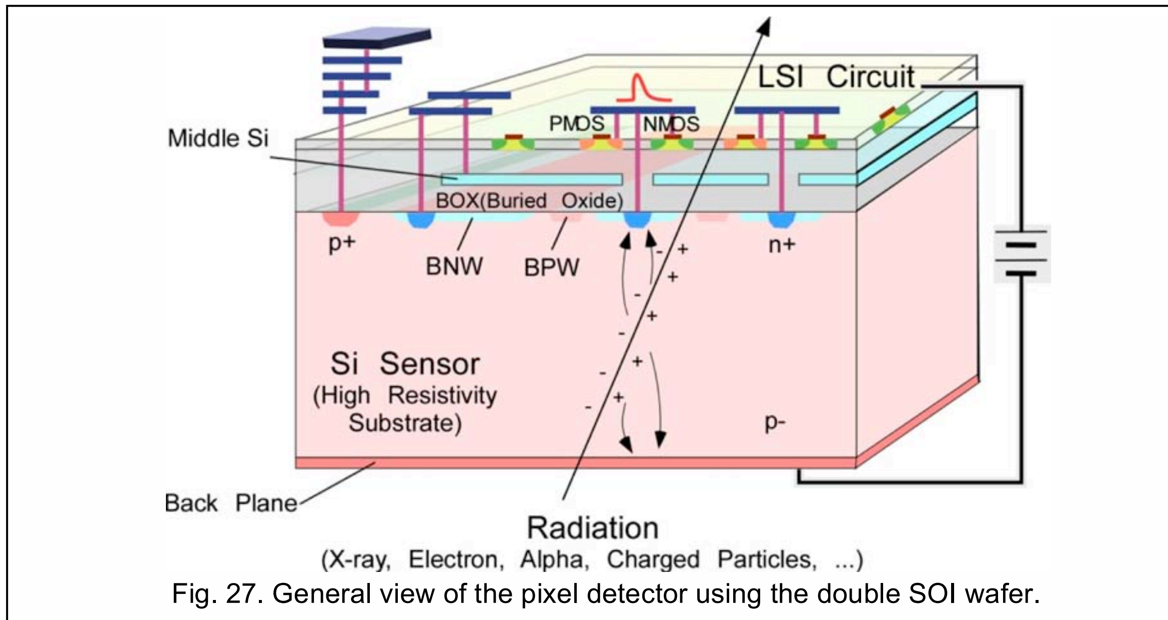


Fig. 27. General view of the pixel detector using the double SOI wafer.

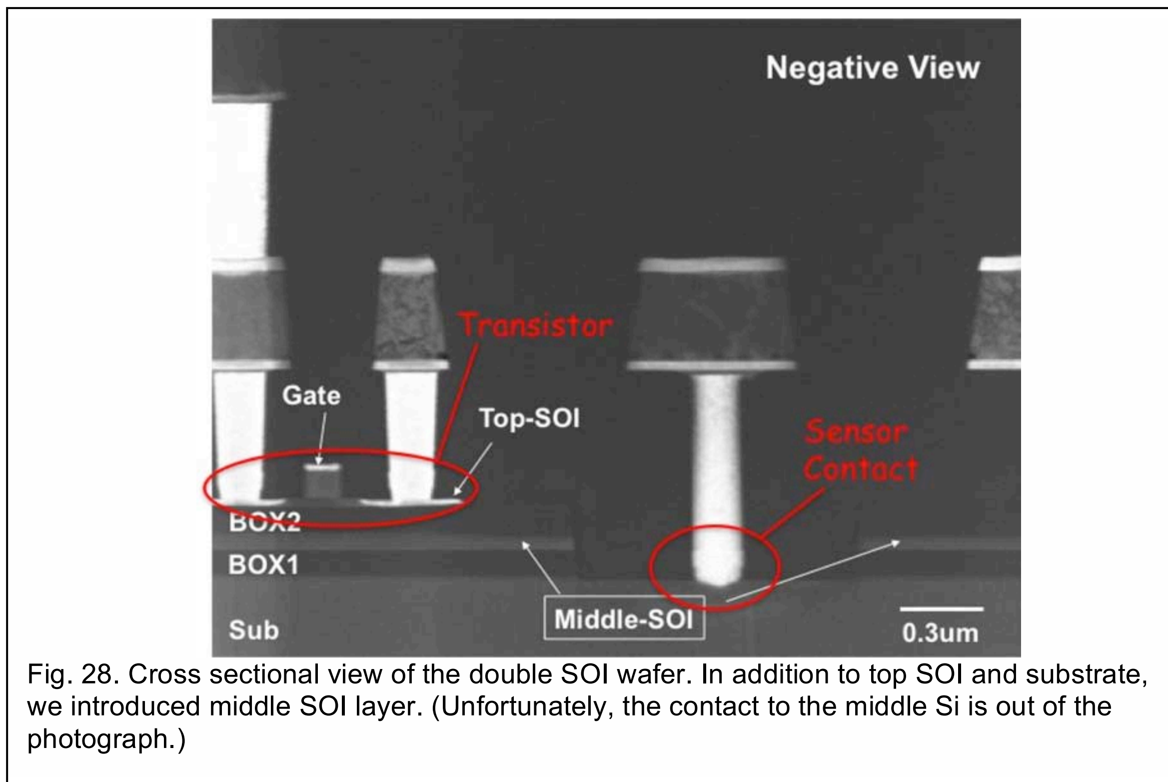


Fig. 28. Cross sectional view of the double SOI wafer. In addition to top SOI and substrate, we introduced middle SOI layer. (Unfortunately, the contact to the middle Si is out of the photograph.)

The first double SOI wafers were produced by SOITEC Co. with n-substrate, but second DSOI wafers have been produced by Shin-Etsu Chemical Co. Ltd, Japan, with p-type substrate.

When we irradiate gamma rays to the SOI, transistor threshold voltage will move to negative direction (Fig. 29 left) due to hole trapping in the oxide. However, by applying negative voltage to the middle Si, electric field generated by the hole is compensated and the threshold voltage will return to almost original value (Fig. 30).

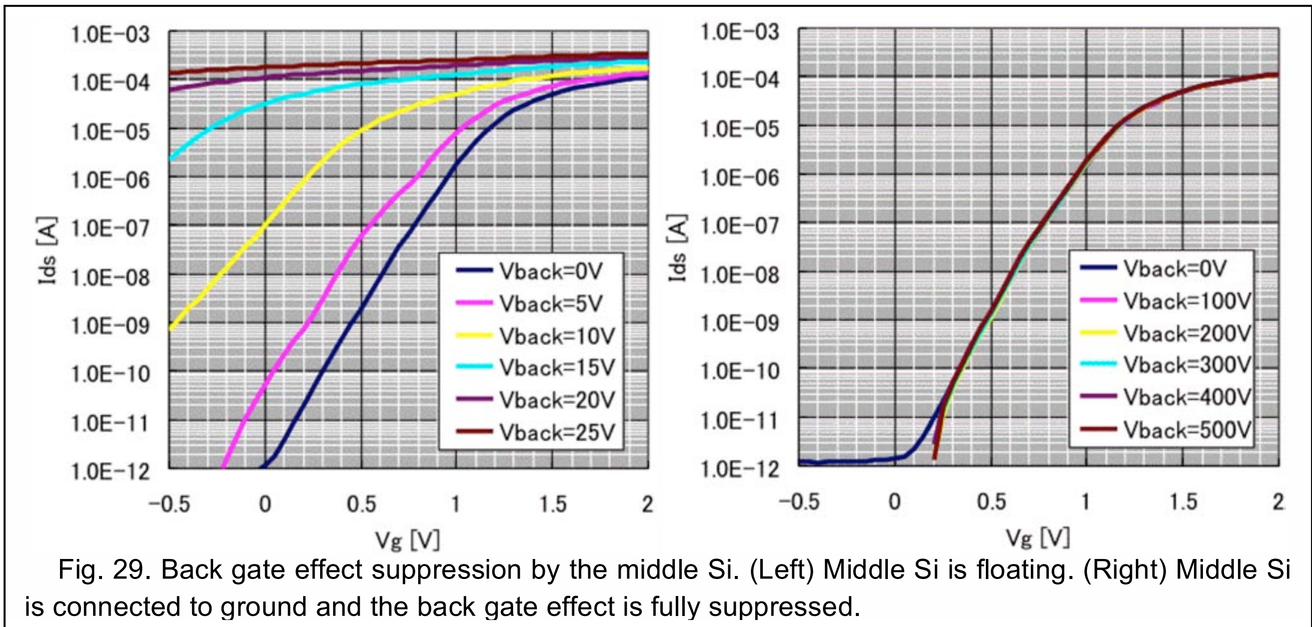


Fig. 29. Back gate effect suppression by the middle Si. (Left) Middle Si is floating. (Right) Middle Si is connected to ground and the back gate effect is fully suppressed.

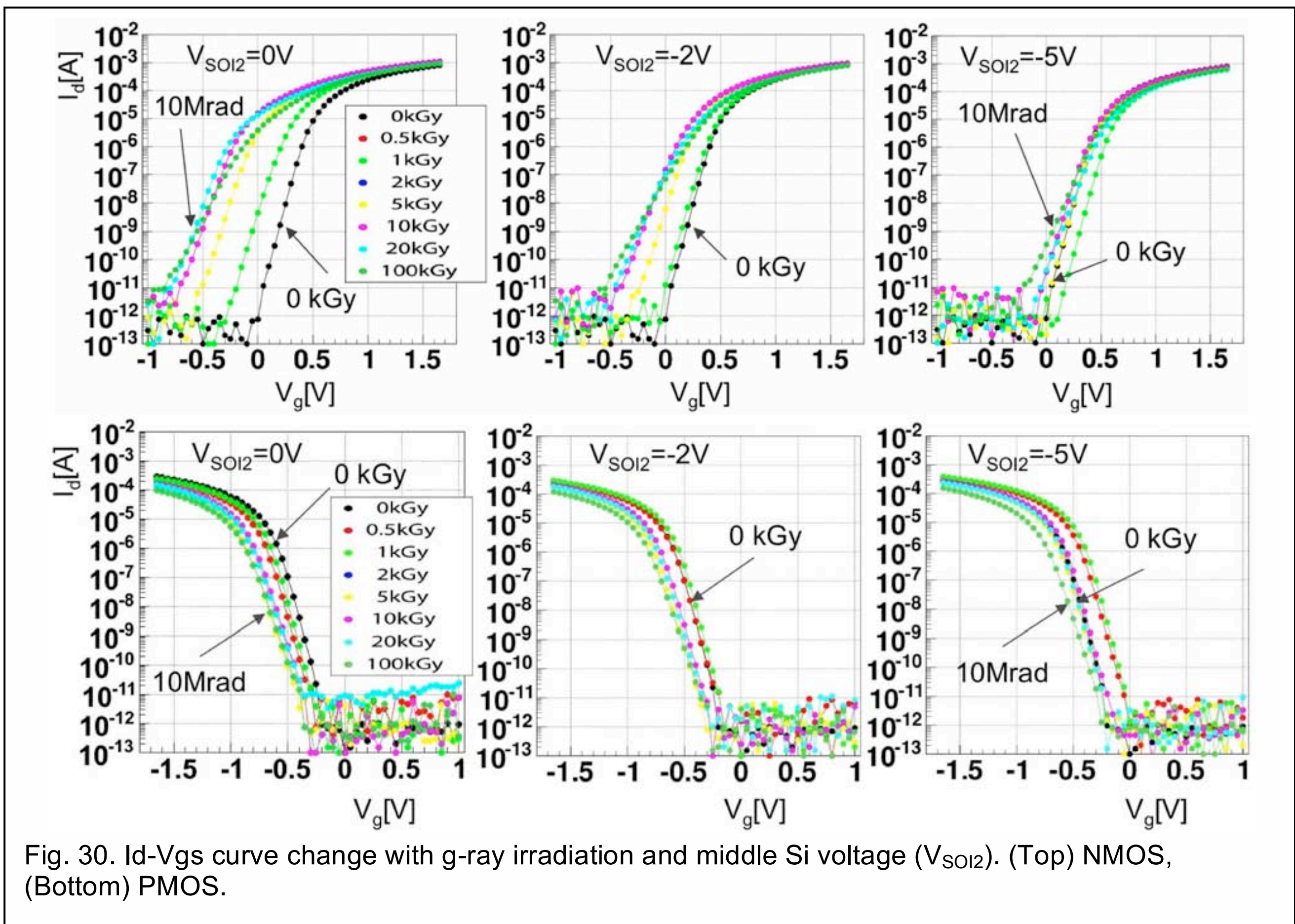


Fig. 30. Id-Vgs curve change with g-ray irradiation and middle Si voltage (V_{SOI2}). (Top) NMOS, (Bottom) PMOS.

Fig. **31** plots optimum value of the SOI2 layer to return the threshold value to original value [vii]. The statistics of the data is not yet enough and there is large variation in the data of NMOS core transistors. However we can see the optimum value for dose up to 20 kGy looks same for all the transistors. On the other hand, at above 20 kGy, we see some rebound in

NMOS transistors. Then we may need to separate the SOI2 layer between NMOS and PMOS for the application that requires more than 20 kGy radiation tolerance.

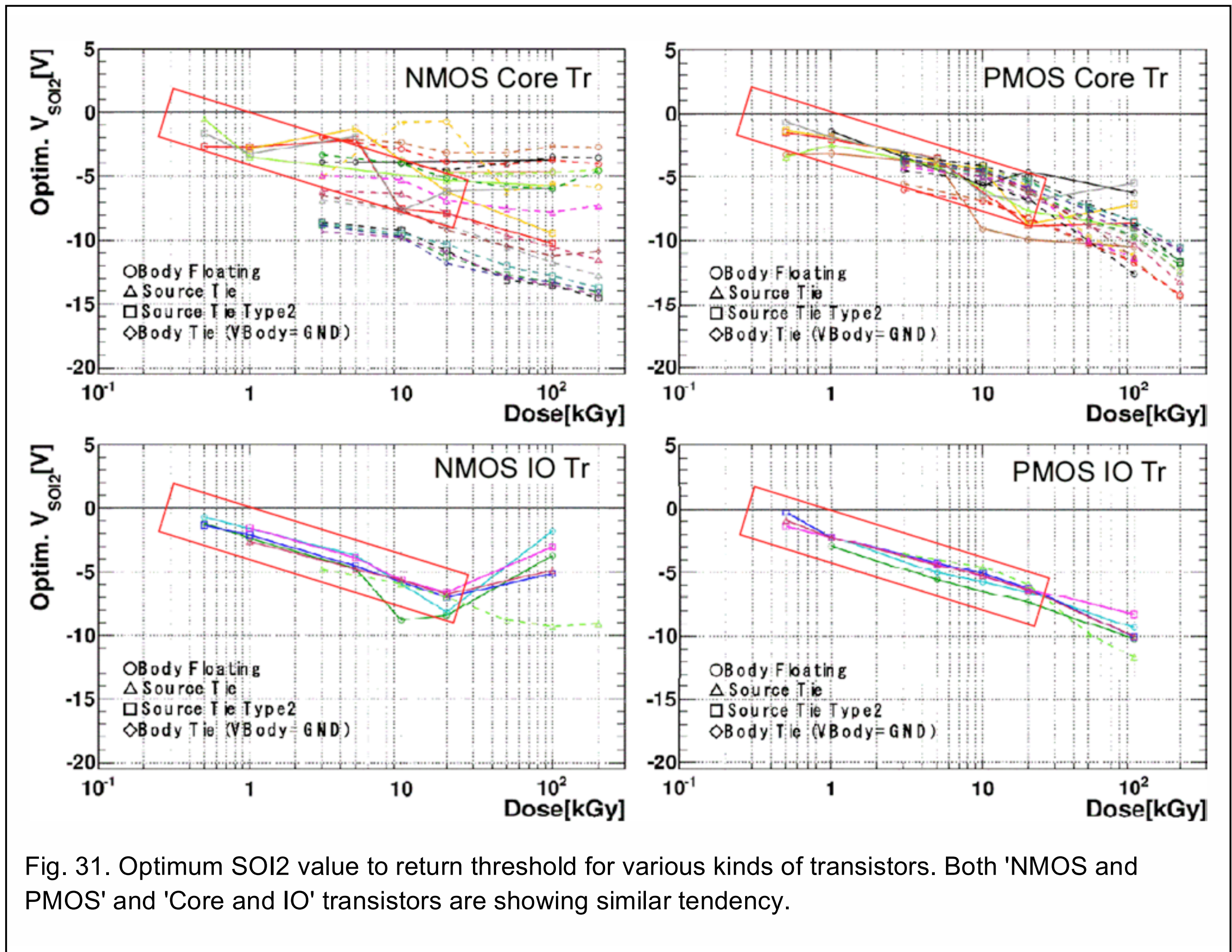


Fig. 31. Optimum SOI2 value to return threshold for various kinds of transistors. Both 'NMOS and PMOS' and 'Core and IO' transistors are showing similar tendency.

4.2 3D Vertical Integration

Although the SOI detector is successfully being developed, future pixel detectors such as used in the International Linear Collider (ILC) requires much more transistors to implement memories and data processing logics than available today. Since the readout circuit needs analog amplification circuits etc., it is not necessary good to go fine node process.

If we try to implement such memory and logics inside the pixel, the pixel size must be very large (> 60 x 60 um^2), while the experiment requires smaller pixel size less than 20 x 20 um^2. To solve this, we have started R&D of 3D vertical integration by using μ-bump technology [viii] in collaboration with T-Micro Co.

Fig. 32 shows the process flow of the vertical stacking of circuit layers. Base SOI chips as upper and lower tiers are fabricated in a SOI wafer. Minimum bump pad opening size is 3 μm x 3 μm. After forming under bump metallization (UBM), Indium bumps are formed using

evaporation and lift-off technique. The minimum bump size and pitch are 2.5-μm sq. and 5 μm respectively.

Lower tier and upper tier are aligned using IR microscope. Initial alignment error before welding bumps must be kept less than 1.0 μm in order to obtain stable electrical connection. After fusing into one connection, the tiers are self-aligned to less than 0.6 μm. The gap between tiers is about 1.5 μm. An array of Indium μ-bump junctions does not have enough mechanical strength. So combining gap fill with adhesive is indispensable and injection method is the key of this process.

Fig. **33** shows layout of alignment mark and photographs of the alignment marks at 4 corners after the bonding and the adhesive injection. The chips are aligned at better than 1 um accuracy. Since the space between tiers is not uniform due to unbalance distribution of the μ-bumps in the chip, adhesive injection caused voids at the points where rapid pressure loss occurs. White island area seen in Fig. **33**-bottom upper left photo is such a void. Number of the voids is greatly reduced by controlling differential pressure assisted capillary action. Although we are bonding chip to chip in this study, chip to wafer bonding techniques are also being developed for mass production.

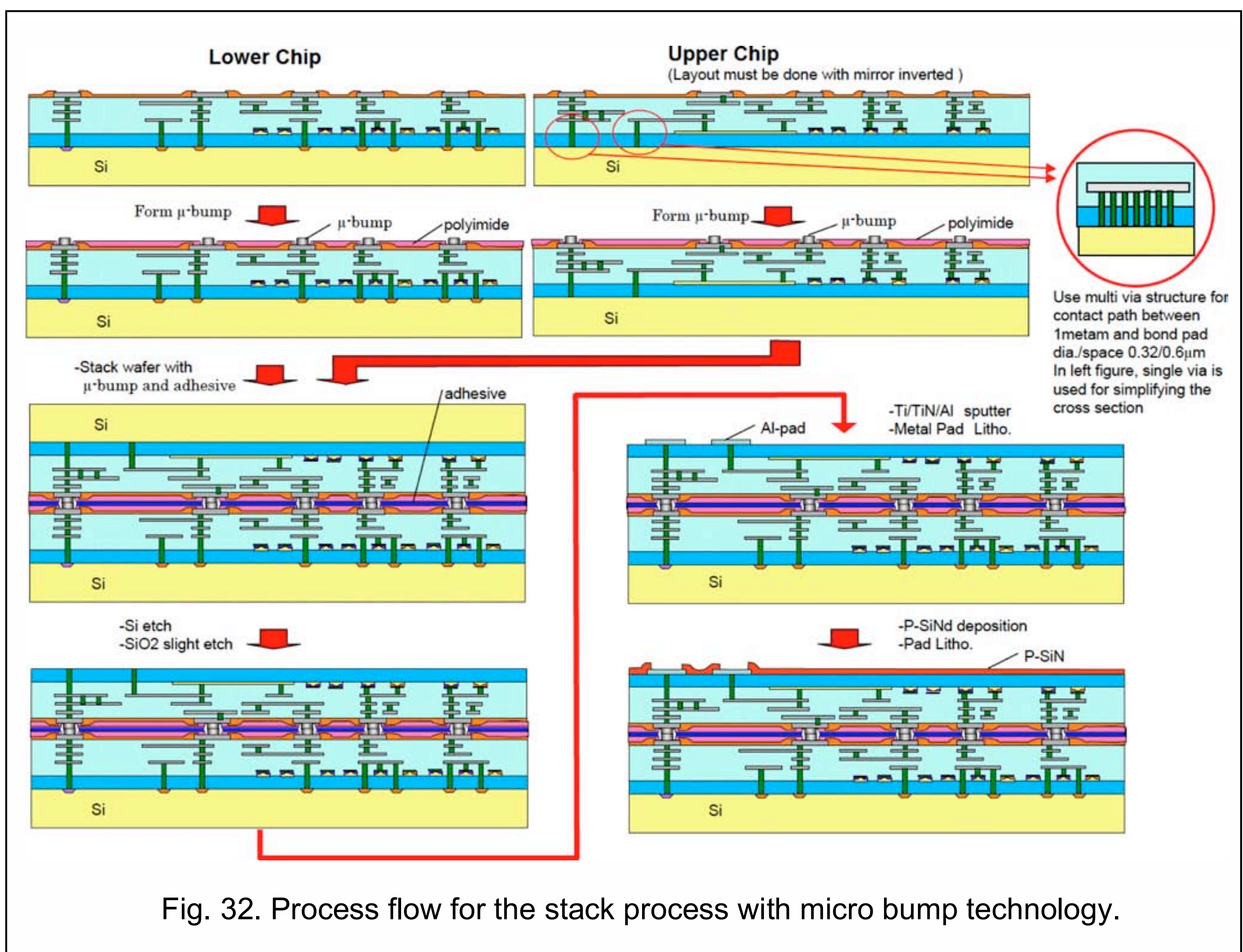


Fig. 32. Process flow for the stack process with micro bump technology.

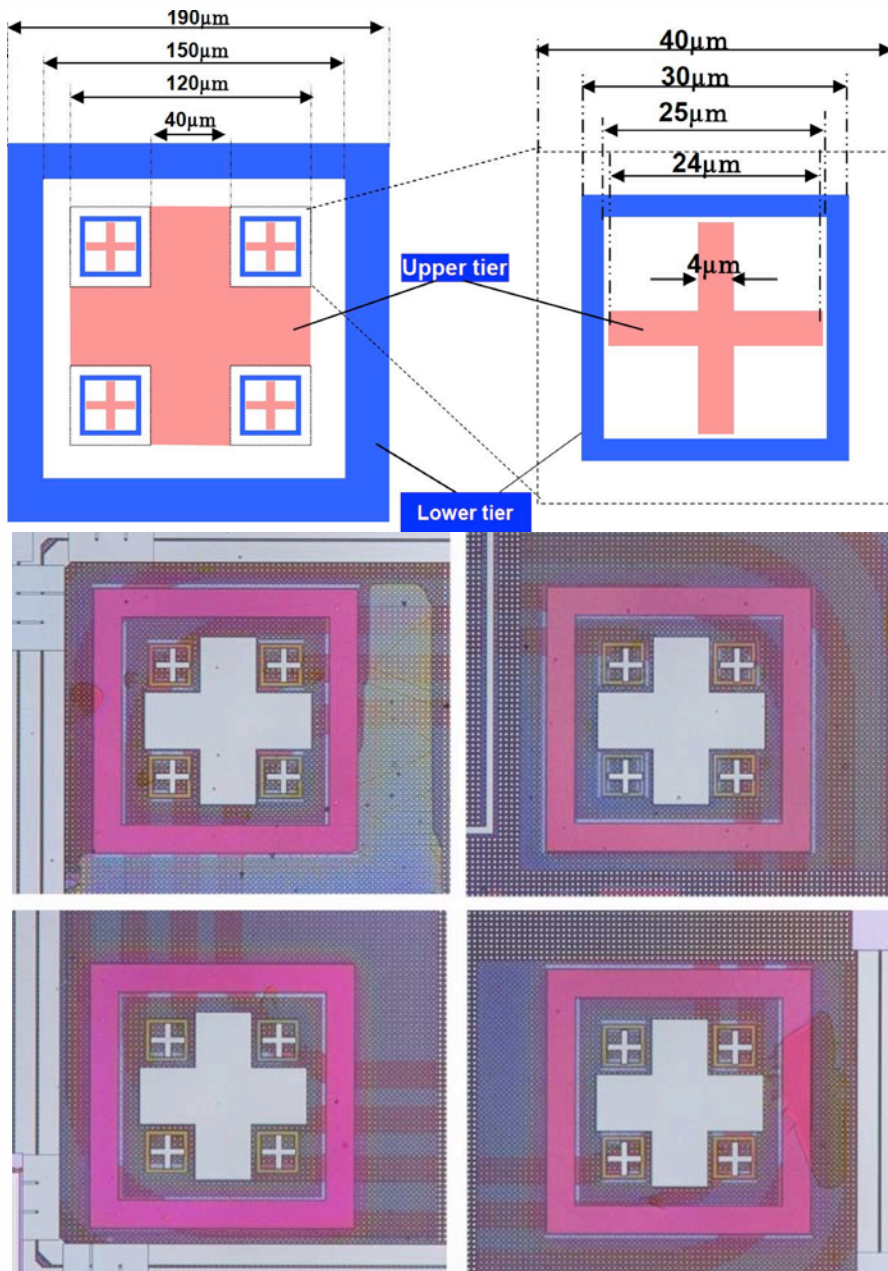


Fig. 33. (Top) Alignment mark size, (Bottom) Alignment of upper and lower chips after stacking.

5. DATA BASE

5.1 Development History

2005. 5 Propose SOI Pixel R&D to KEK Detector Technology Project

2005. 7 Start Collaboration with OKI Electronics Co. Ltd.

2005.10 First submission to Univ. of Tokyo (VDEC) 0.15μm SOI MPW run.

2006.12 First MPW run of 0.15um SOI process operated by KEK.

2007.3 First SOI Workshop @KEK

2007. 6 Process change to Miyagi 0.2um line due to discontinue of Hachioji 0.15 μm line.

2007.10 First User Meeting @U. of Hawaii (IEEE NSS)

2008. 1 First MPW run of 0.2μm SOI process.

2008.3 SOI Workshop @KEK

2008.10 OKI semiconductor division was spin-off to OKI semiconductor Co. Ltd, and enters under Rohm Co. group.

2009. 1 Metal Pitch is shrunken from 0.88um to 0.58um.
Introduce Buried P-Well structure.

2009.2 SOI W.S. @Kyoto Univ.

2010.3 Collab. Mtg. @Fermilab

2011.2 International Review @KEK

2011.3 OKI Semi Miyagi Fab. was damaged by the large earthquake.

2011.9 Name of OKI Semi was changed to Lapis Semiconductor Co. Ltd.

2011.10 Mask size was increased from 20.6 mm square to 24.6 mm x 30.8 mm.

2012.3 Collab. Mtg. @LBNL

2012.8 First double SOI wafer was processed.

2012.9 PIXEL2012 conference @Fukushima.

2013.2 Mini Workshop @IHEP (China)

2013.5 Collab. Mtg. @Krakow (AGH & IFJ)

2013.8 10th 0.2um MPW run was submitted.

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[Cooperation Companies]

Name
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Lapis Semiconductor Miyagi Co. Ltd.
A-R-Tec Co.
Rigaku Co.
T-micro Co. Ltd.
REPIC Co. Ltd.
Digian Technology Inc.

5.3 Master Thesis

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2） "First Results of 0.15um CMOS SOI Pixel Detector", Y. Arai, M. Hazumi, Y. Ikegami, T. Kohriki, O. Tajima, S. Terada, T. Tsuboyama, Y. Unno, H. Ushiroda, H. Ikeda, K. Hara, H. Ishino, T. Kawasaki, E. Martin, G. Varner, H. Tajima, M. Ohno, K. Fukuda, H. Komatsubara, J. Ida, SNIC Symposium, Stanford, California, 3-6 April 2006, SLAC-PUB-12079, KEK preprint, 2006-34, SLAC Electronic Conference Proceedings Archive (SLAC-R-842, eConf: C0604032) PSN-0016. http://www.slac.stanford.edu/econf/C0604032/papers/0016.PDF.

3） "Monolithic Pixel Detector in a 0.15mm FD-SOI Technology", Y. Arai,presented at the 6th Hiroshima symposium of Development and Application of semiconductor tracking devices, Sep. 11-15, 2006, Carmel, California, U.S.A.

4） "Development of a CMOS SOI Pixel Detector", Y. Arai, M. Hazumi, Y. Ikegami, T. Kohriki, O. Tajima, S. Terada T. Tsuboyama, Y. Unno, Y. Ushiroda, H. Ikeda, K. Hara, H. Ishino, T. Kawasaki, H. Miyake, E. Martin, G. Varner, H. Tajima M. Ohno, K. Fukuda, H. Komatsubara, J. Ida,Proceedings of 12th Workshop on Electronics for LHC and Future Experiments (LECC 2006), 25-29 September 2006, Valencia SPAIN.

5） "Monolithic Pixel Detector in a 0.15um SOI Technology", Y. Arai, M. Hazumi, Y. Ikegami, T. Kohriki, O. Tajima, S. Terada, T. Tsuboyama, Y. Unno, H. Ushiroda, H. Ikeda, K. Hara, H. Ishino, T. Kawasaki, E. Martin, G. Varner, H. Tajima, M. Ohno, K. Fukuda, H. Komatsubara, J. Ida, H. Hayashi,, IEEE Nuclear Sci. Symposium, San Diego, Oct. 29 - Nov. 4, 2006, Conference Record, Vol. 3, Oct. 2006 Page(s):1440 - 1444, Digital Object Identifier 0.1109/NSSMIC.2006.354171.

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9） "SOI Monolithic Pixel Detector R&D in a 0.15 mm SOI Technology", Y. Arai, Y. Ikegami, Y. Unno, T. Tsuboyama, S. Terada, M. Hazumi, T. Kohriki, H. Ikeda, K. Hara, H. Ishino, H. Miyake, K. Hanagaki, G. Varner, E. Martin, H. Tajima, Y. Hayashi, M. Ohno, K. Fukuda, H. Komatsubara, J. Ida., 16th International Workshop on Vertex detectors, September 23-28, 2007, Lake Placid, NY, USA, Vertex 2007, Poster Presentation.

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5.5 External Fundings

1） 平成 19-22 年度, 科学技術振興機構　先端計測分析技術・機器開発事業（要素技術開発），「SOI 技術による時間・空間Ｘ線イメージセンサー」
2） 平成 20-21 年度、日米科学技術協力事業(高エネルギー物理分野)、衝突実験用測定器の開発、「SOI 技術を用いた先進的ピクセルセンサーの開発」
3） 平成 18 年度－19 年度、科学研究費補助金　基盤研究(A)（一般）　研究代表者　坪山透、「SOI 技術を用いたピクセルセンサーの開発」
4） 平成 20 年度－22 年度、科学研究費補助金　基盤研究(B)（一般）　研究代表者　鶴　剛、「SOI 技術による低バックグラウンド・精密分光撮像・広帯域Ｘ線ピクセル検出器の開発」
5） 平成 21 年度～24 年度、科研費　基盤研究（A)、「ＳＯＩ技術による高分解能・薄型ピクセル検出器の研究」、研究代表者　新井康夫。
6） 2012-2014 JST 先端計測分析技術・機器開発事業　開発成果の活用・普及促進　(SOI Ｘ線イメージ装置の活用・普及促進）
7） 2013.7-2018.3, Grant-in-Aid for Scientific Research on Innovative Area, "Interdisciplinary research on quantum imaging opened with 3D semiconductor detector.

5.6 Patents

1） 「半導体装置及び半導体装置の製造方法」、特願 2010-52173、PCT/JP2011/055546(2011.3.9), US13/583,409 (02/21/2013)
2） 「半導体装置」、特願 2010-226717(2010.10.6)、特開 2012-80045(P2012-80045A)、公開日 2012.4/19
3） 「半導体装置」、特願 2010-196075（出願日 2010/09/01、特開 2012-54421）
4） 「半導体装置及び半導体装置の製造方法」特願 2011-208180（出願日 2011/09/22）
5） 「半導体装置およびその製造方法」特願 2013-4017(2013.1.11)
6） 「デジタル TDI 方式検出器」、特願 2012-242275 (2012.11.2)
7） 「半導体装置およびその製造方法」特願 2013-79859 (2013.4.5)

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