Looking with a SOI monolithic pixel sensor

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from the movie 'The Mummy: Tomb of the Dragon Emperor'
I. Introduction
II. Recent Progress
III. Looking with SOI pixel
IV. Summary
Monolithic Detector having fine resolution of silicon process and high functionality of CMOS LSI by using a SOI Pixel Technology.
Features of SOI Pixel Detector

- Monolithic device. No mechanical bonding.

- Fabricated with semiconductor process only, so high reliability and low cost are expected.

- High Resistivity fully depleted thick sensing region with Low sense node capacitance.

- On Pixel processing with CMOS transistors.

- 100% Fill-Factor with Back Illumination.

- No Latch up and Low single event cross section.

- Can be operated in wide temperature (1K-570K) range.

- Based on Industry Standard Technology.
## Lapis Semi. (*) 0.2 μm FD-SOI Pixel Process

| Process                  | 0.2μm Low-Leakage Fully-Depleted SOI CMOS  
1 Poly, 5 Metal layers.  
MIM Capacitor (1.5 fF/um²), DMOS  
Core (I/O) Voltage = 1.8 (3.3) V |
|--------------------------|--------------------------------------------------------------------------------------|
| SOI wafer                | Diameter: 200 mmϕ, 720 μm thick  
Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick  
Buried Oxide: 200 nm thick  
Handle wafer: Cz (n) ~700 Ω-cm,  
FZ(n) > 2k Ω-cm, FZ(p) ~25 k Ω-cm etc. |
| Backside process         | Mechanical Grind, Chemical Etching, Back side  
Implant, Laser Annealing and Al plating |

(*) Former OKI Semiconductor Co. Ltd.
II. Recent Progress

Double SOI

Single SOI

- Shield Crosstalk
- Compensate radiation induced oxide charge

Si Sensor
(High Resistivity Substrate)

CMOS Circuit

Box (Buried Oxide)

Back Plane

Radiation
(X-ray, Electron, Alpha, Charged Particles, ...)

- Shield Crosstalk
- Compensate radiation induced oxide charge
Cross section of the Double SOI Pixel

- Transistor
- Middle Si
- Metal 1
- Metal 5
- Sensor Contact
- Middle Si Contact

Scale: 3.00 μm
**Structure of 2 kinds of Double SOI wafer**

<table>
<thead>
<tr>
<th>Layer</th>
<th>D-1</th>
<th>D-2</th>
</tr>
</thead>
<tbody>
<tr>
<td>SOI1</td>
<td>p-type 88 nm, &lt;10 $\Omega \cdot$cm</td>
<td>p-type 88 nm, &lt;10 $\Omega \cdot$cm</td>
</tr>
<tr>
<td>BOX1</td>
<td>145 nm</td>
<td>145 nm</td>
</tr>
<tr>
<td>SOI2</td>
<td>p-type 88 nm, &lt;10 $\Omega \cdot$cm</td>
<td>n-type 150 nm, &lt;10 $\Omega \cdot$cm</td>
</tr>
<tr>
<td>BOX2</td>
<td>145 nm</td>
<td>145 nm</td>
</tr>
<tr>
<td>Substrate</td>
<td>n-type CZ 725um, &gt;700 $\Omega \cdot$cm</td>
<td>p-type CZ, 725um, &gt;1.0 k $\Omega \cdot$cm</td>
</tr>
</tbody>
</table>
Sheet Resistance of the Middle Si (SOI2)

Sheet resistance of the middle Si changes depend on its potential. D-2 wafer has lower resistance in operation region.
By using Double SOI wafer, Cross Talk between Circuit and Sensor reduced to 1/20.
Gamma-ray Irradiation Test
(Id-Vg Characteristics v.s. SOI2 Potential)

By setting V_{SOI2} \sim -5V, Id-Vg curve returned nearly to pre-irradiation value at 100 kGy(Si)

I/O normal Vth
Source-Tie Tr.
L/W = 0.35um/5um

⇒ Poster by Mari Asano
Variation of Id-Vg Characteristics and Effect of SOI2 Potential

PMOS

V_{SOI2}=0V

V_{SOI2}=-2V

V_{SOI2}=-5V

I/O Normal Vt
Source-Tie
L/W =0.35um/5um

Threshold voltage shift is not so large in PMOS, but Drain Current decreases much.

-80%
TID Improvement for PMOSFETs

- Major cause of drain current degradation by X-ray irradiation for PMOSFETs must be \( \text{Vt increase at gate edge due to positive charge generation in spacer.} \)
- To reduce this effect, \textit{lightly doped drain (LDD) concentration} may be a key factor.
- When the concentration is high, impurity diffused underneath the gate and consequently Vt of gate edge is not controlled by charge in the spacer.
- \textit{Higher LDD dose} for PMOSFETs should be one of TID improvement methods.

\textbf{When LDD dope is low or P- is offset, possibility to form parasitic transistor at gate edge.}

(by I. Kurachi)
Id-Vg Characteristics in Triode Region

With increasing Implantation dose of PLDD region 6 times higher than present value, the degradation reduces 80% to 20% at 112 krad(Si).

Removing Radiation Induced Oxide Charge with FN Tunneling

Radiation damage is recovered by applying HV pulses to under-layer of transistor.

 Poster by Miho Yamada
Back Gate Pinning SOI Pixel (BPSPRX)

- New sensor structure to deplete from backside.
- Suppress Back Gate effect and achieve small collection electrode.
- Low capacitance, High Gain.
- Lower surface leak current.
III. Looking with SOI Pixel detector

- Imaging of Elementary Particle Origin of Mass by Higgs Particle
- Imaging Mass Spectrometer Rapid Analysis
- 128x128 1.8K Operation
- Far Infra Red Evolution of Stars
- Harsh Environment
- Precise Time Resolution
- X-ray Imaging Synchrotron Radiation
- SOIPIX (目標) Distant X-ray
- Background Reduction
- Precise 1nm Resolution
- X-ray femto Second
- Gold Nano Particle Δx = ~10 nm
- ♯ of a Cell
- High Intensity
Timing resolution of CCD is too poor to make anti-coincidence.

Each pixel has its own trigger and analogue readout CMOS circuit.
• Generate Trigger signal when a hit is occurred.
• Then X- and Y- addresses of the hit are sent out.
Pixel Layout

**55Fe Spectrum**

- **(solid)**: fitting line
- **(dot)**: data

**Note:** Pixel gain was not calibrated.

- CSA Pixel
  - FWHM: 5% (300 eV)
- Normal Pixel
  - FWHM: 11% (650 eV)

**Mn-K$_\alpha$**
- 5.9 keV
- Mn-K$_\beta$
- 6.4 keV

Counts

Energy (keV)
History of XRPIX Noise & Gain

New SOI Pixel Detector (BSPPIX) (7e-, 30uV/e-)

Shizuoka Univ.
Looking XFEL

SOI Photon-Imaging Array Sensor (SOPHIAS)
Dual Sensor Camera for SACLA X-ray Free Electron Laser
XFEL Test: CoO
Ave. $\phi = 22\text{nm}$
t=1mm

Si Attenuation Film
Transmittance=5%

Sensor Temp.: $-24^\circ\text{C}$
Exposure 1ms
HV 200V

Beam stopper

Courtesy of T. Kudo (RIKEN)
of Intl. Image Sensor
Workshop (IISW) 3.05.
Looking 3D Fish with Synchrotron X-ray

- Sensor: INTPIX4 FZn, Backside Illumination
- HV: 200V, Integration Time: 1ms, Scan Time: 320ns/pix, 1000frame/event
- KEK PF, X-ray Energy: 9.5keV
- Took images for 0°~180° at every 1 degree.

(by R. Nishimura, K. Hirano (KEK) → [59] Development of X-ray Imaging system with SOI Pixel Detectors)
Looking Computed Tomography (CT) with Syncrotron X-ray

→ Poster by Nishimura
III. Summary

• SOI pixel detector is a monolithic detector which has both radiation sensor and CMOS circuit in a single die.
• The thickness of the sensor and pixel circuit can be easily tailored.
• Double SOI reduces cross talk between sensor and circuit.
• Radiation tolerance is improved by introducing the Double SOI and increasing the dose of LDD region.
• Radiation induced oxide charge can be extracted with HV pulsing in under-layer of transistors.
• Higher gain and lower noise are expected in new sensor structure (BPPIX).
• Many applications are being pursued within SOIPIX collaboration.