Progress on Silicon-on-Insulator Monolithic Pixel Process

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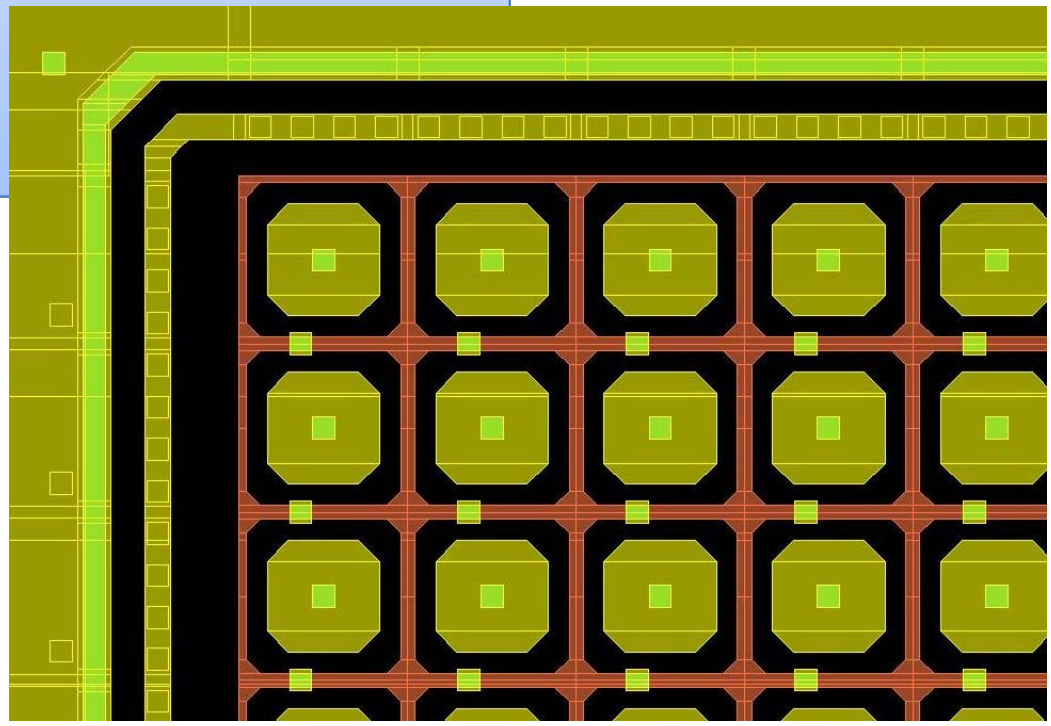
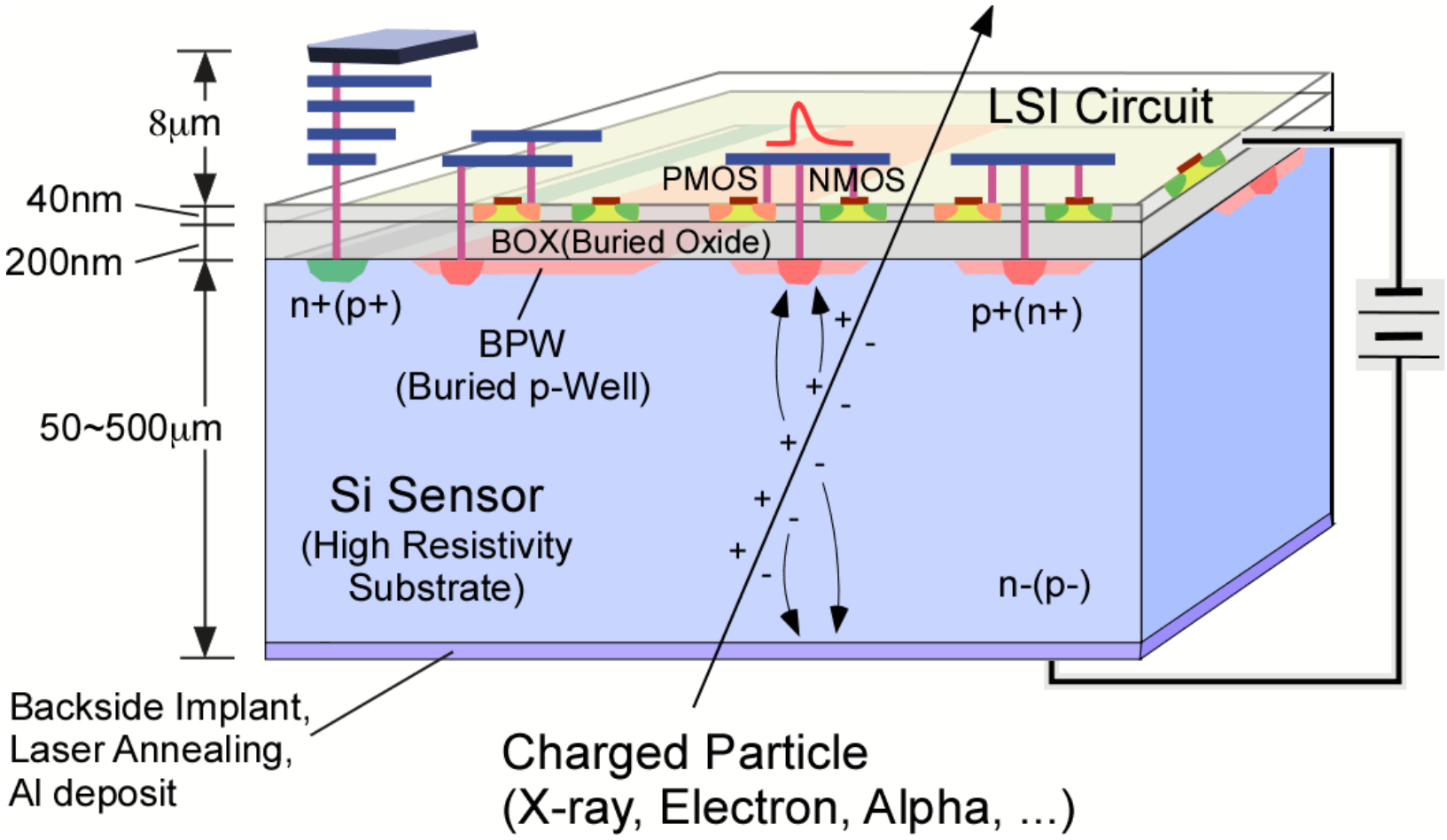
Outline

- Introduction
- Basic SOI Pixel Process
- Advanced Process Techniques
- Project Status
- Summary



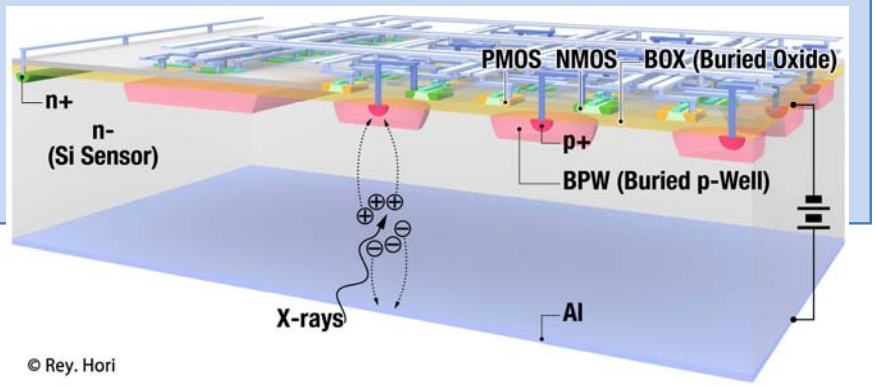
Introduction



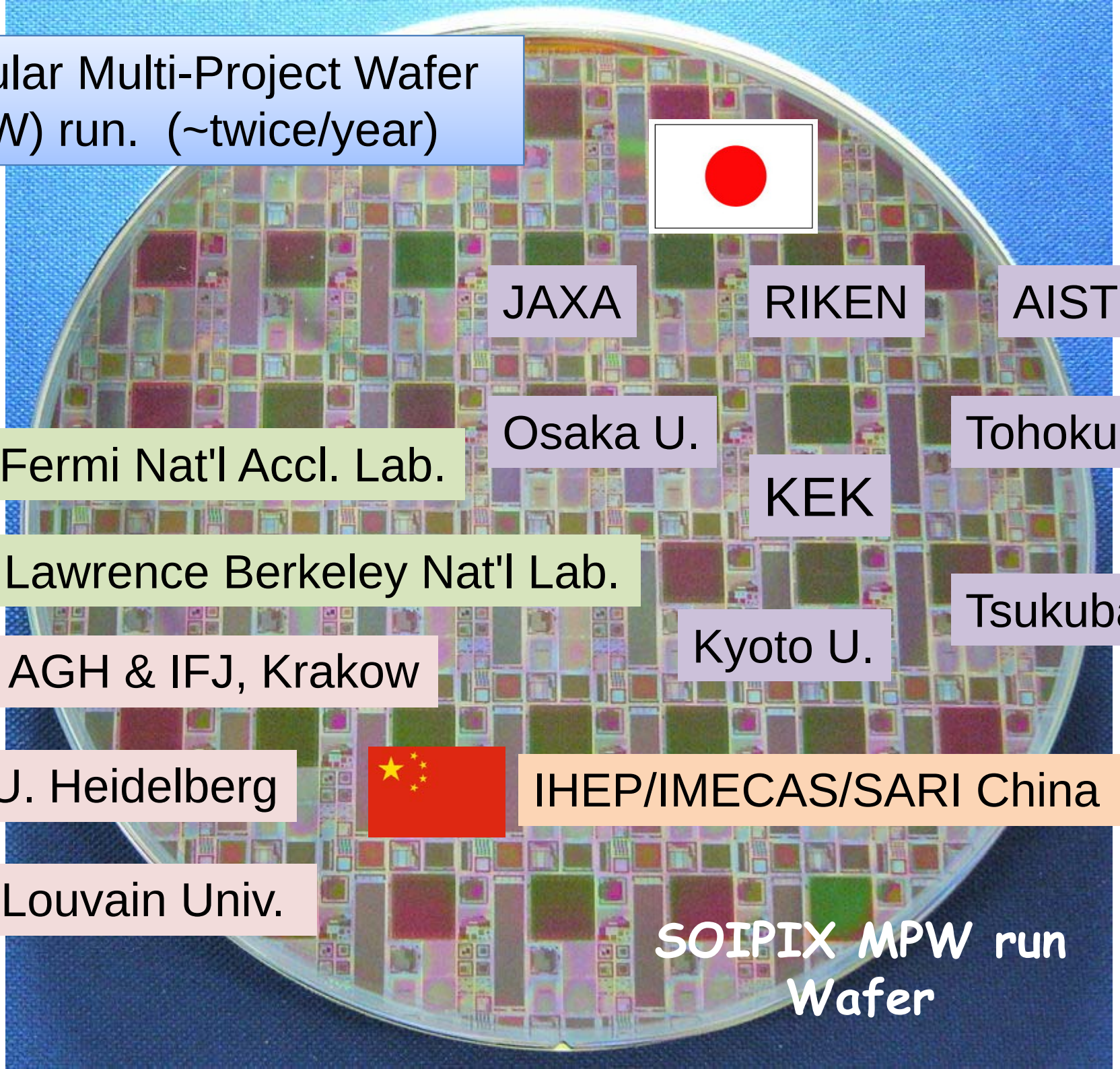
Silicon-On-Insulator Pixel Detector (SOIPIX)

Feature of SOI Pixel Detector

- No mechanical bonding. Fabricated with semiconductor process only, so high reliability, low cost are expected.
- Fully depleted thick sensing region with Low sense node capacitance.
- On Pixel processing with CMOS transistors.
- Can be operated in wide temperature (1K-570K) range, and has low single event cross section.
- Based on Industry Standard Technology.



Regular Multi-Project Wafer (MPW) run. (~twice/year)



JAXA RIKEN AIST

Osaka U. Tohoku U.

KEK

Fermi Nat'l Accl. Lab.

Lawrence Berkeley Nat'l Lab.

Tsukuba U.

Kyoto U.

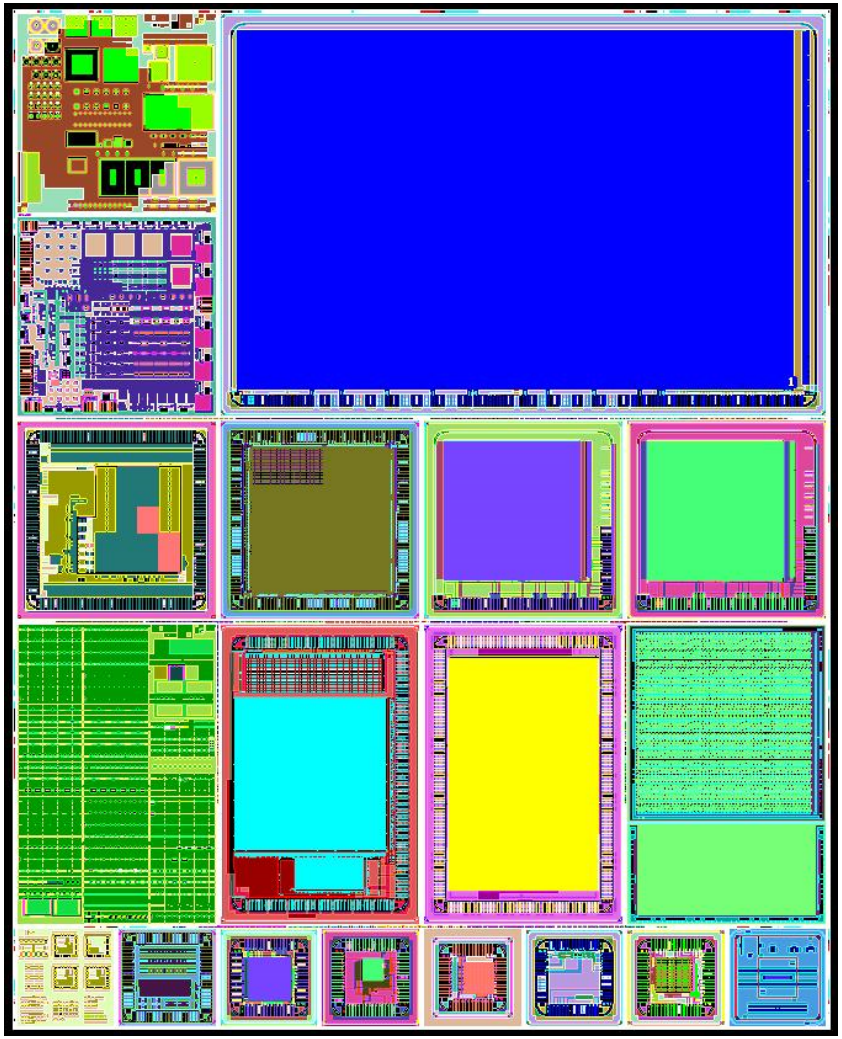
AGH & IFJ, Krakow

U. Heidelberg

IHEP/IMECAS/SARI China

Louvain Univ.

Basic SOI Pixel Process



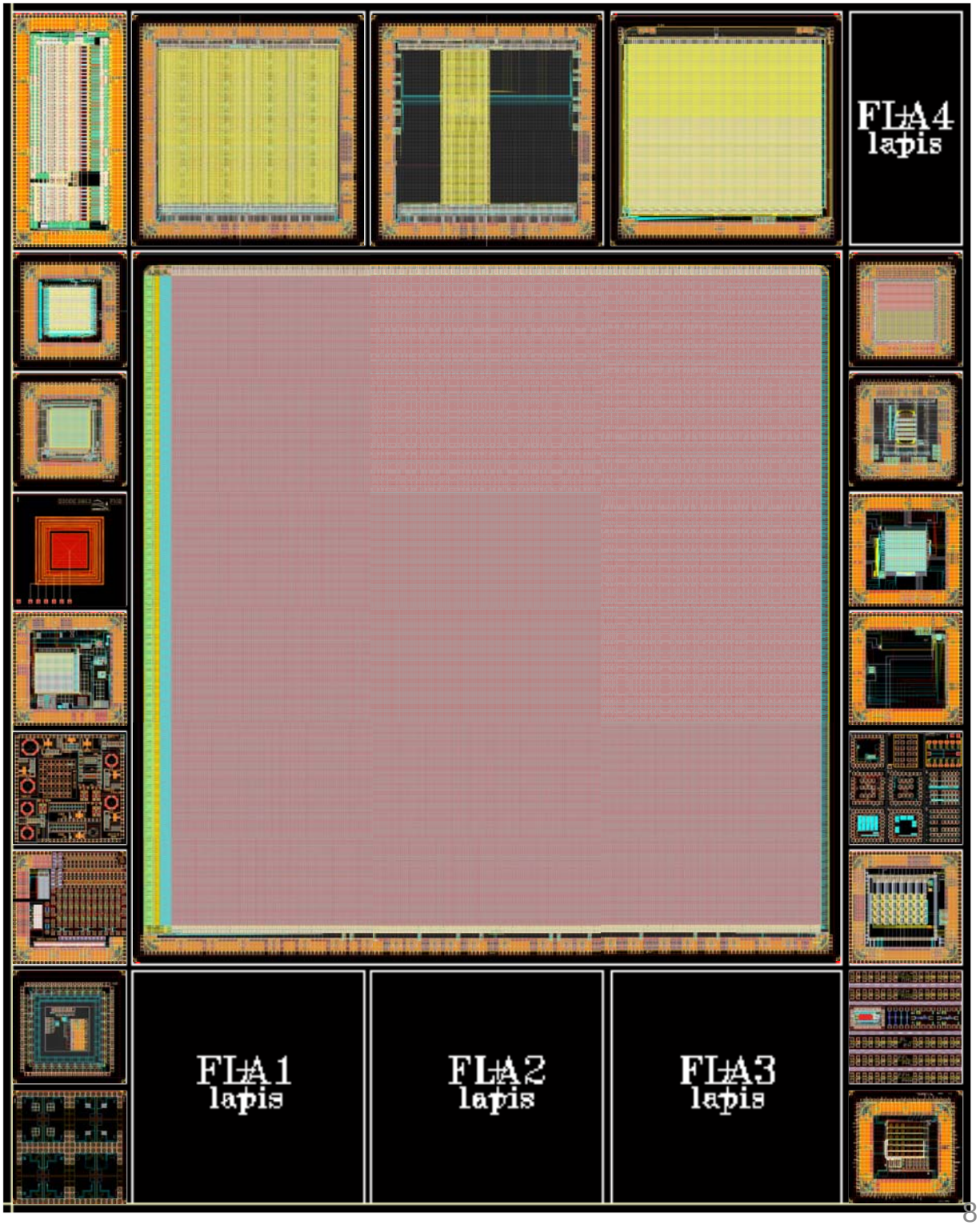
Lapis (*) Semi 0.2 μm FD-SOI Pixel Process

Process	0.2μm Low-Leakage Fully-Depleted SOI CMOS 1 Poly, 5 Metal layers. MIM Capacitor (1.5 fF/um^2), DMOS Core (I/O) Voltage = 1.8 (3.3) V
SOI wafer	Diameter: 200 mmϕ, 720 μm thick Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz (n) ~700 Ω-cm, FZ(n) ~7k Ω-cm, FZ(p) ~25 k Ω-cm etc.
Backside process	Mechanical Grind, Chemical Etching, Back side Implant, Laser Annealing and Al plating

(*) Former OKI Semiconductor Co. Ltd.

Mask Size

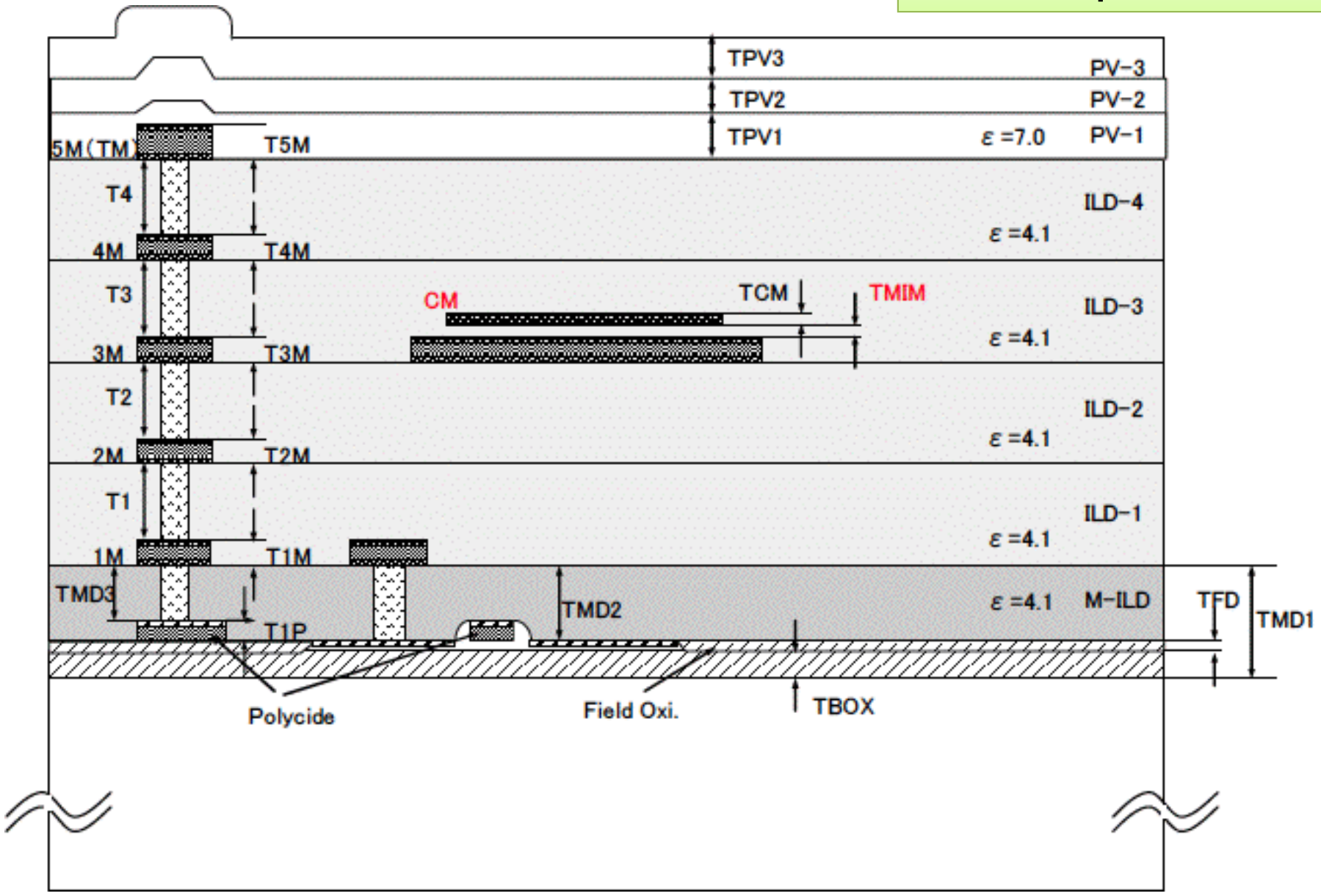
24.6 x 30.8 mm



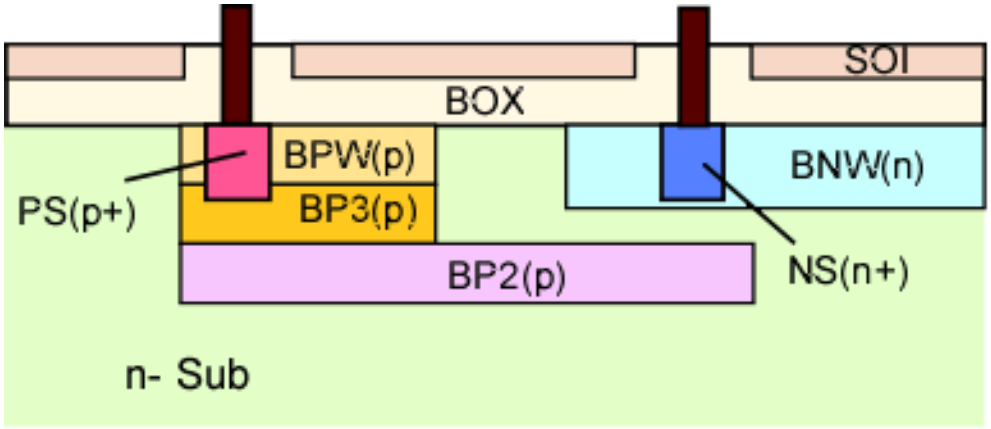
Smallest chip area for MPW run is 2.9mm x 2.9mm

Structure of Top Si

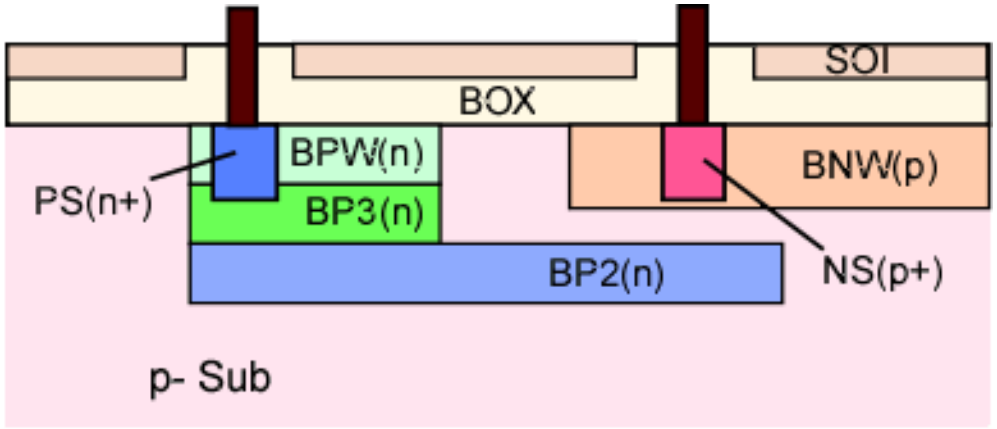
1 Poly + 5 Metal
MIM Capacitor on 3M



Structure of Bottom Si (Sensor part)



Normal Process for n- substrate

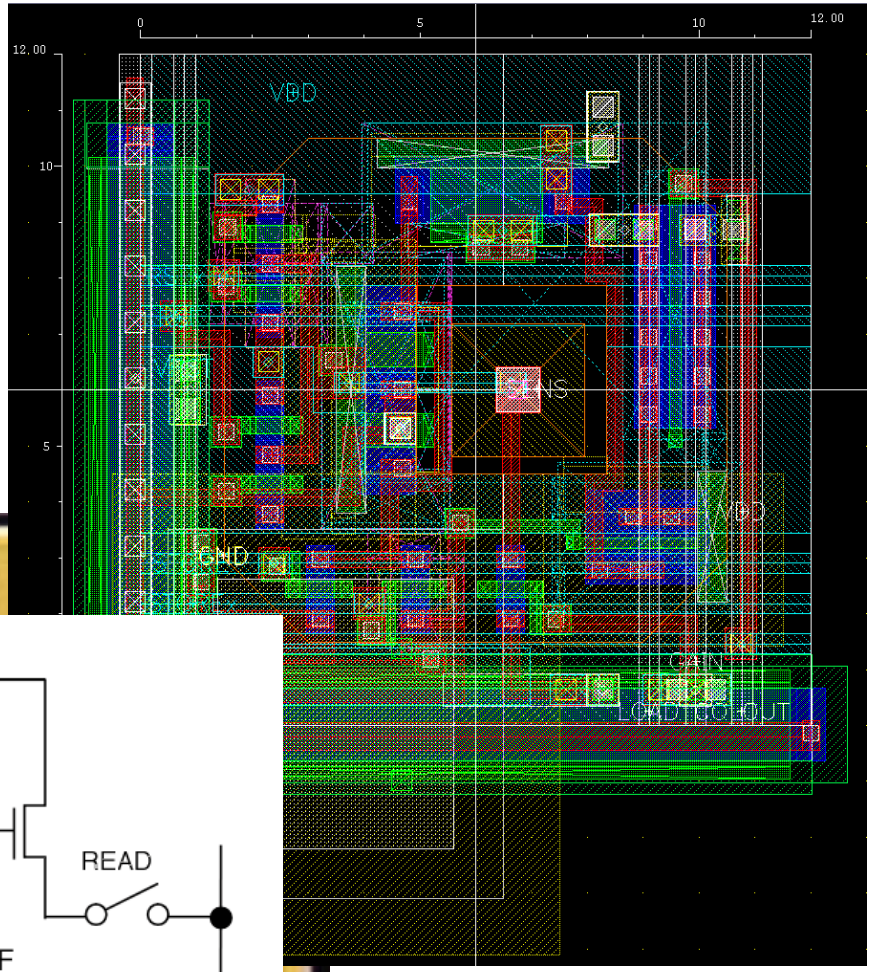


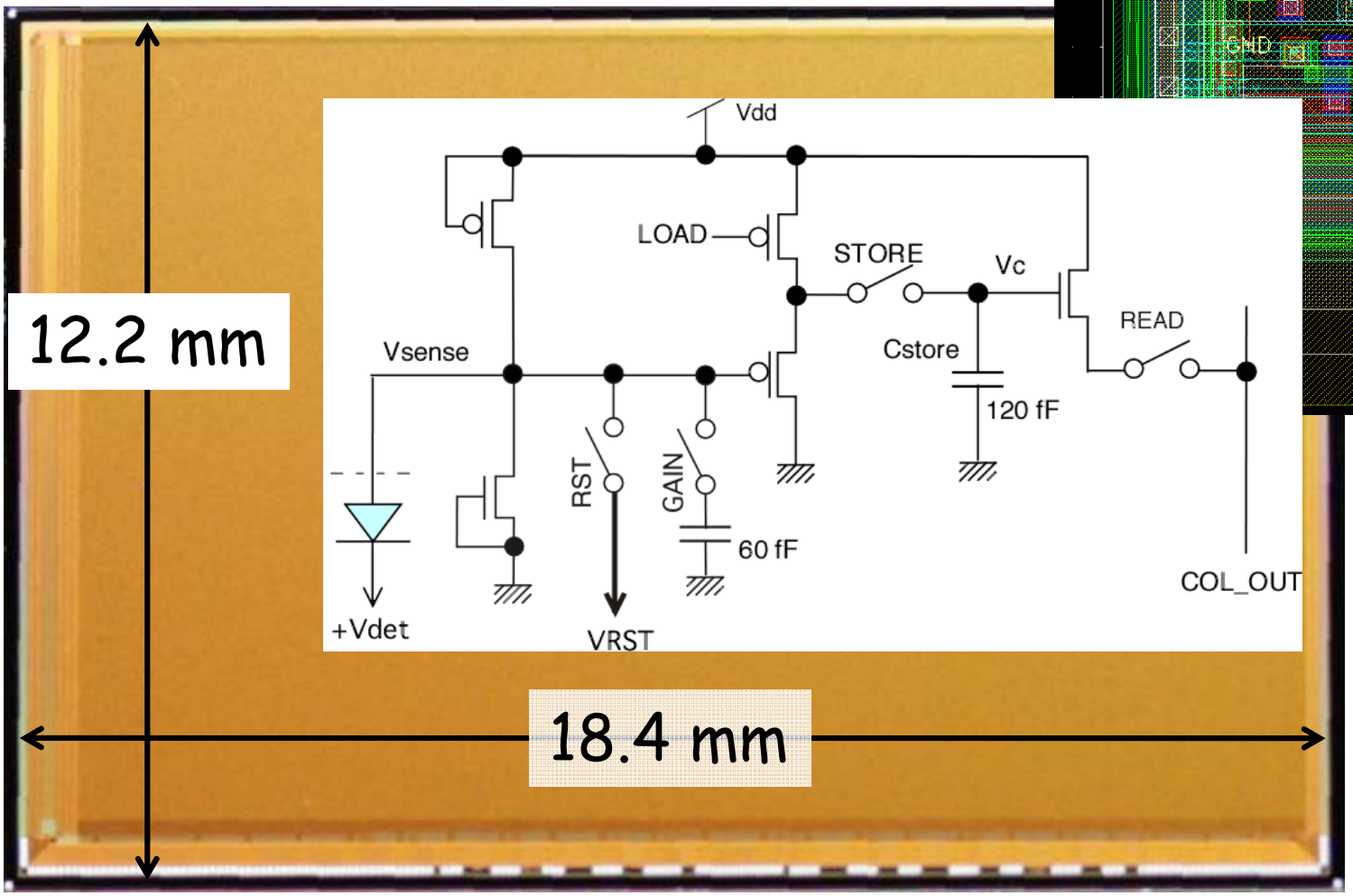
Reverse Process for p- substrate

- PS & NS --- High doping density Layer (Top Si is removed)
- Buried Well (BPW, BP2, BP3 & BNW)
  --- Low doping density buried Layer
- For p-type substrate, dopants are changed to create reverse polarity by using the same mask layers.
- Doping density and depth can be changed on request.

An example of SOIPIX: Integration Type Pixel (INTPIX)

Pixel Size : 12x12 μm^2
896x1408 (~1.3 M) pixels、
11 Analog out port、Column CDS.

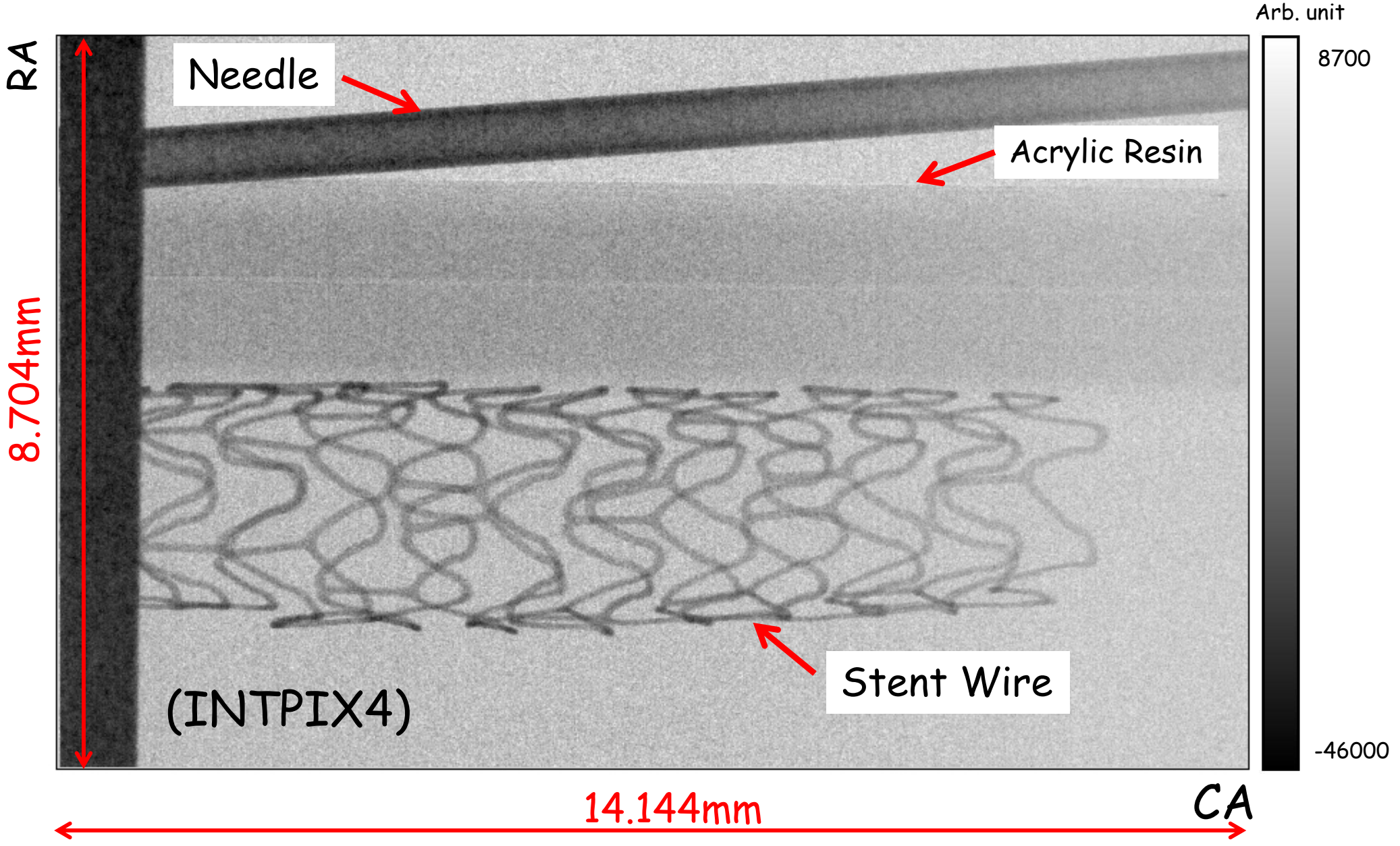




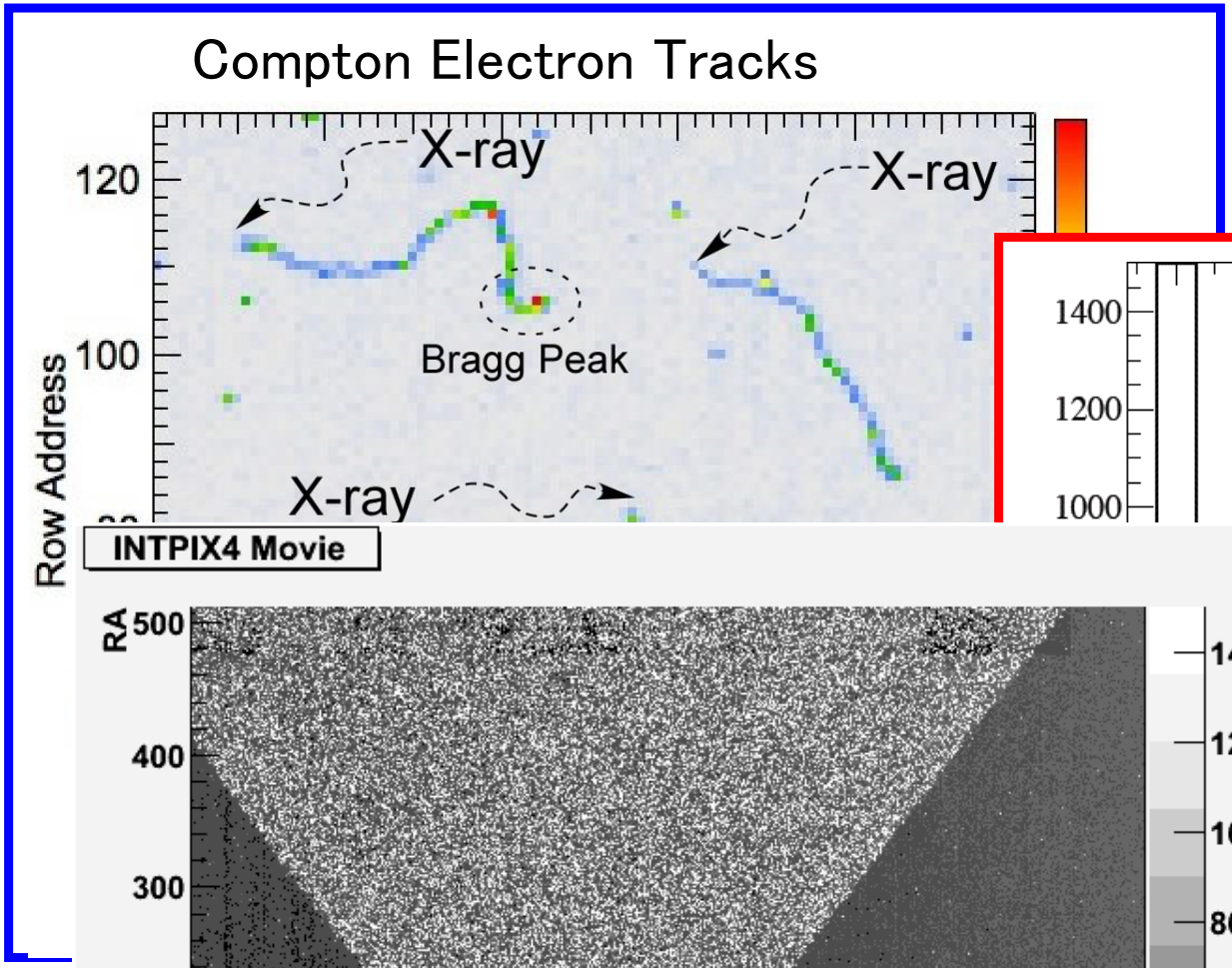
INTPIX5

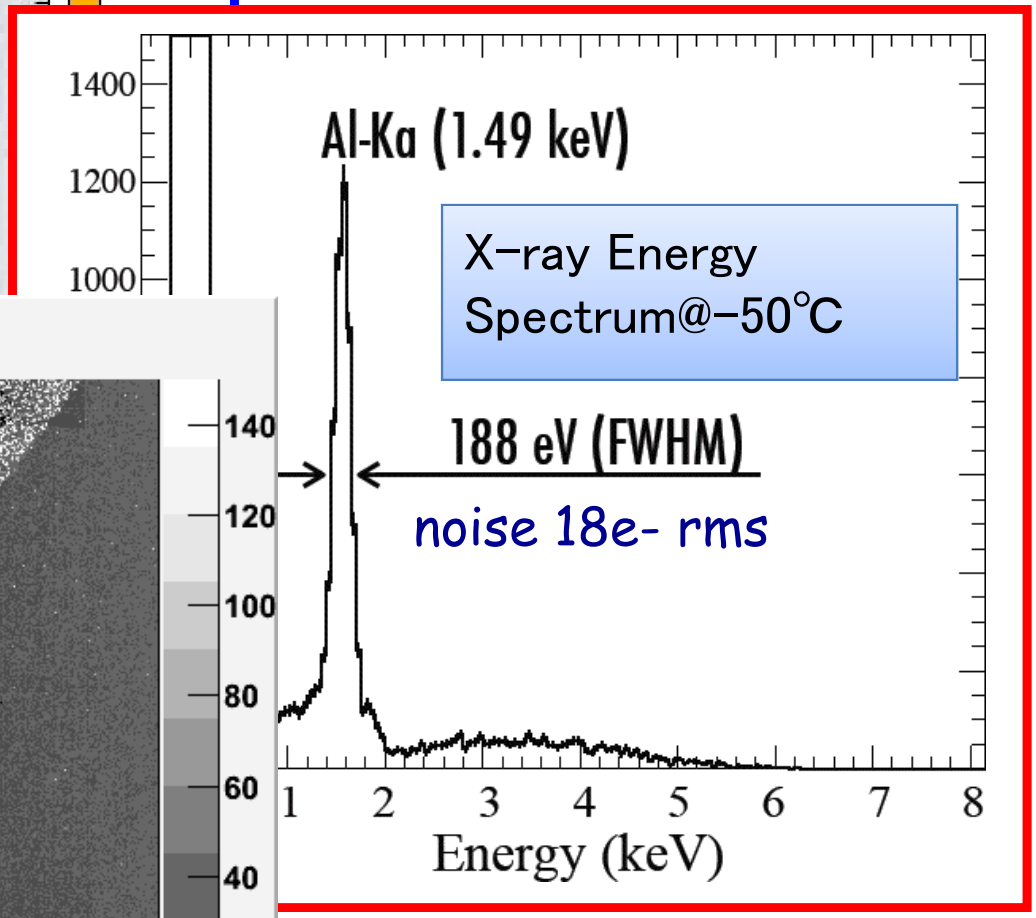
Examples of SOIPIX Measurement

PF-AR NE7A 33.3keV monochromatic
Acrylic resin 40mm
200us x 250 frames



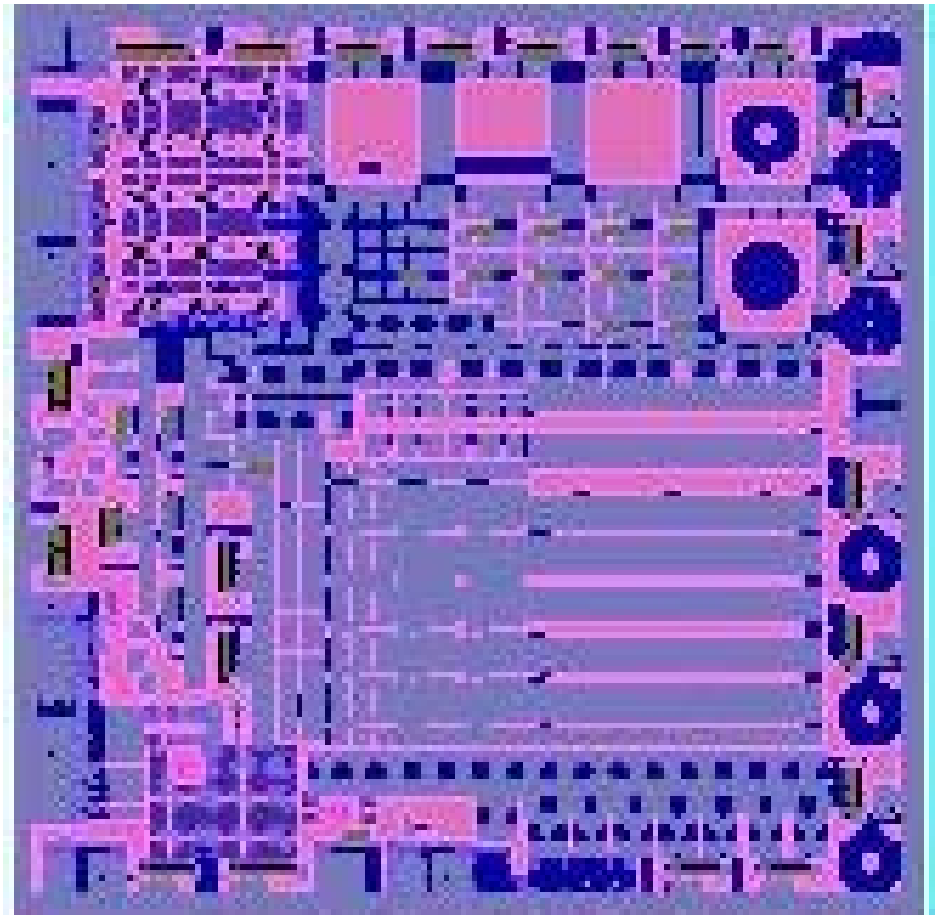
Examples of SOIPIX Measurement





Advanced Process Techniques

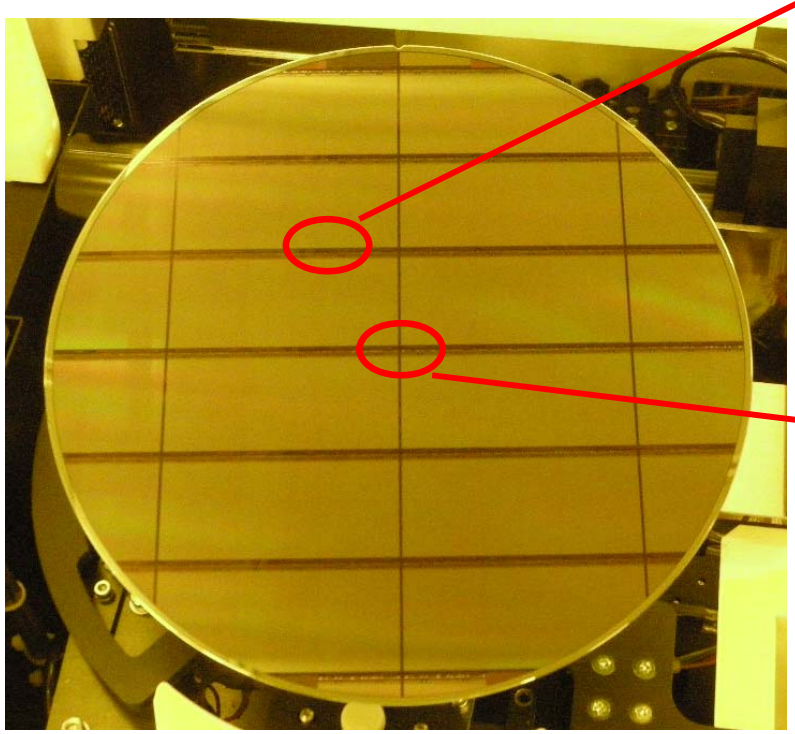
- Stitching
- Double SOI
- 3D Vertical Integration

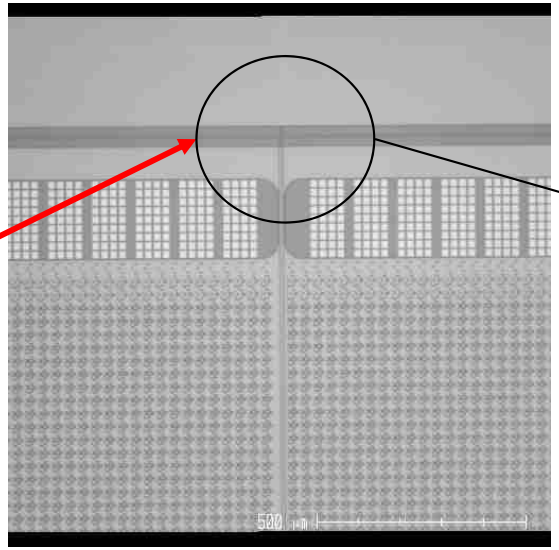


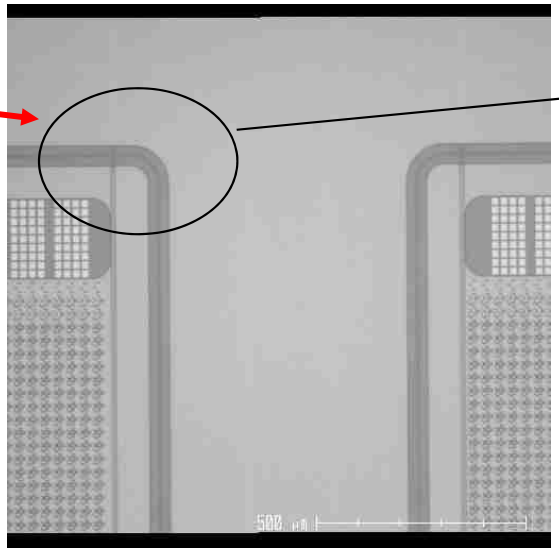
Stitching Exposure for Large Sensor

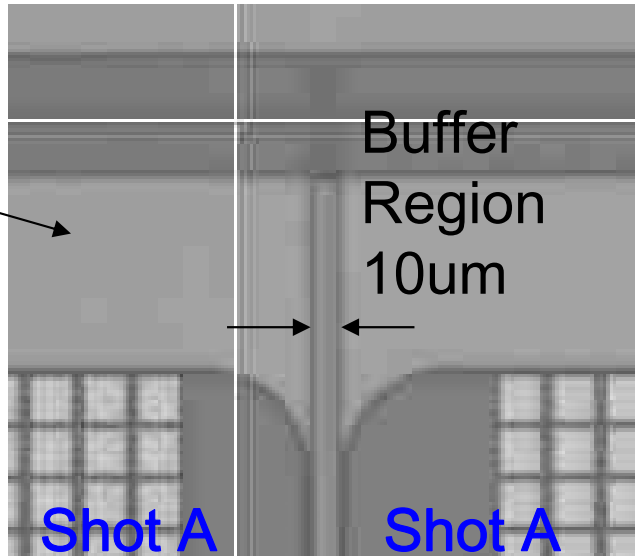
SOPHIAS by RIKEN

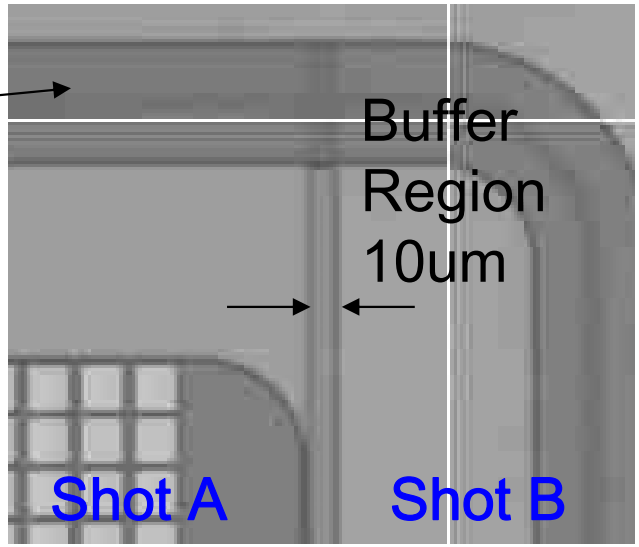
Reticule size
~25mm x 31mm







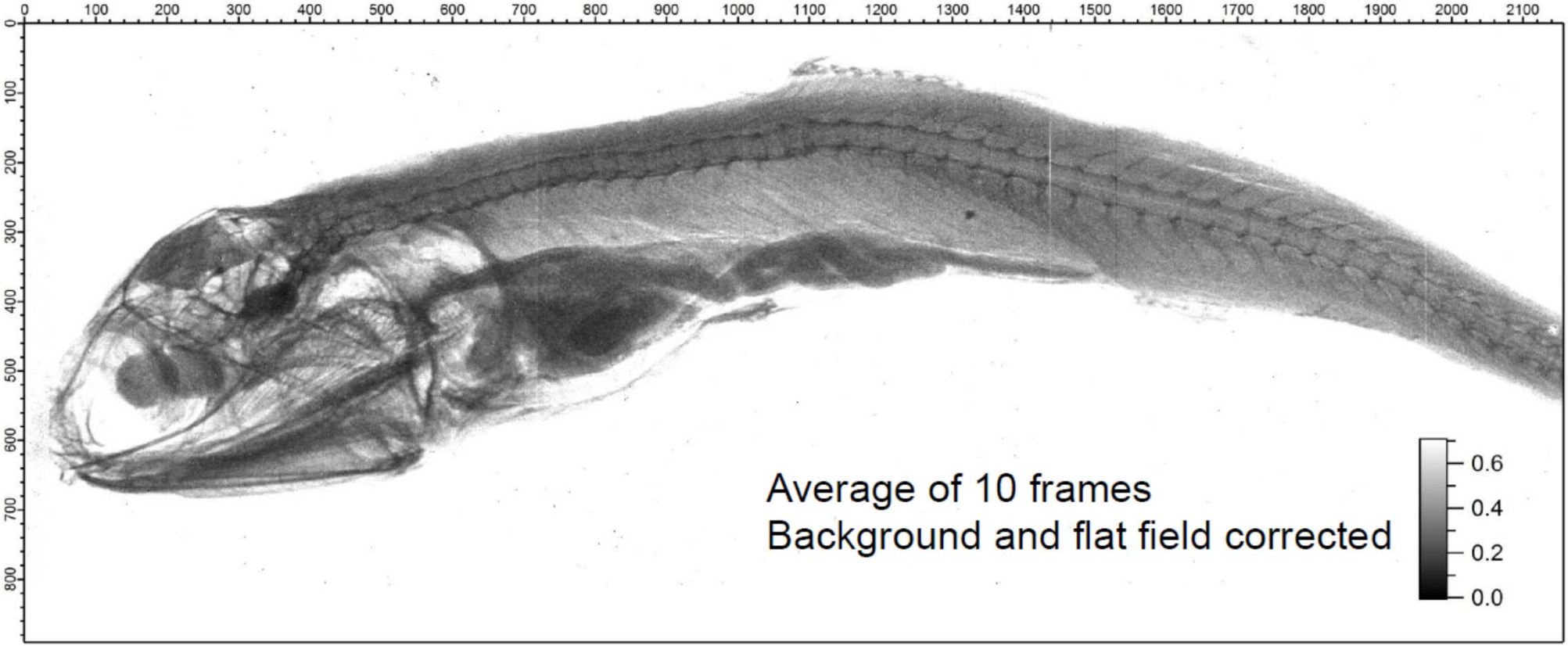




- Width of the Buffer Region can be less than 10um.
- Accuracy of Overwrap is better than 0.025um.

RIKEN SOPHIAS chip

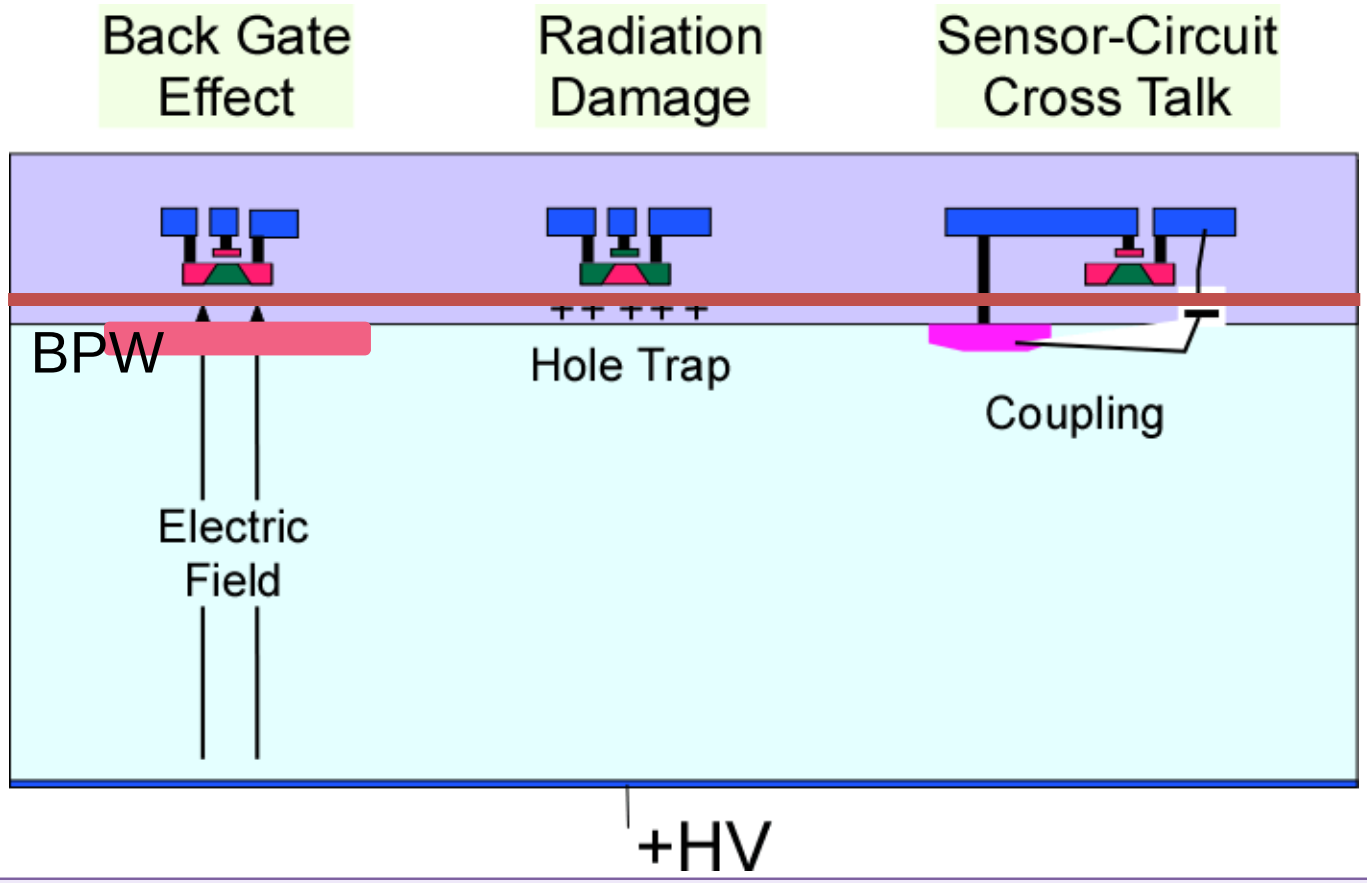
X-ray Transmission



- Source-sample : 200 mm
- detector-sample : 600 mm
- X-ray : 40 kV, 800 uA
- Cu target
- X-ray source size : ～3 um
- Exposure time : 10 msec
- Temperature : room temperature

Double SOI wafer

Sensor and Electronics are located very near. This cause ..



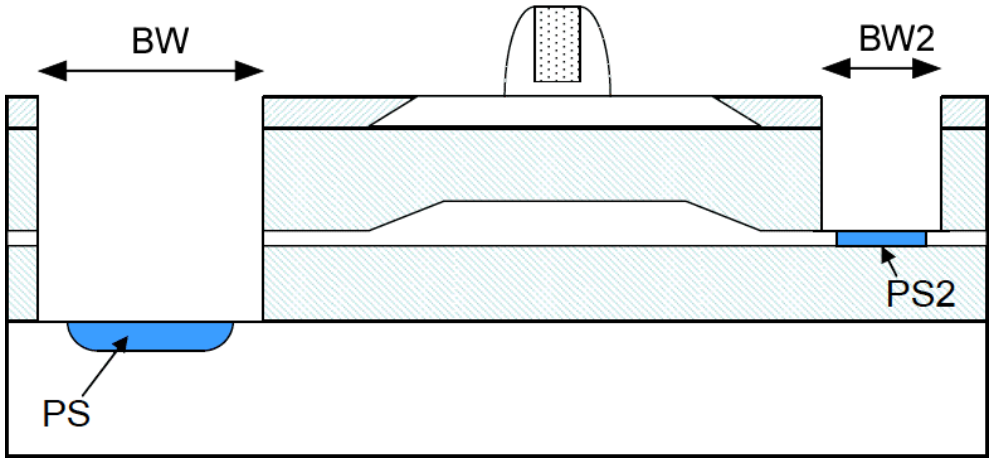
At first, we successfully introduced BPW layer to remove the back gate effect.

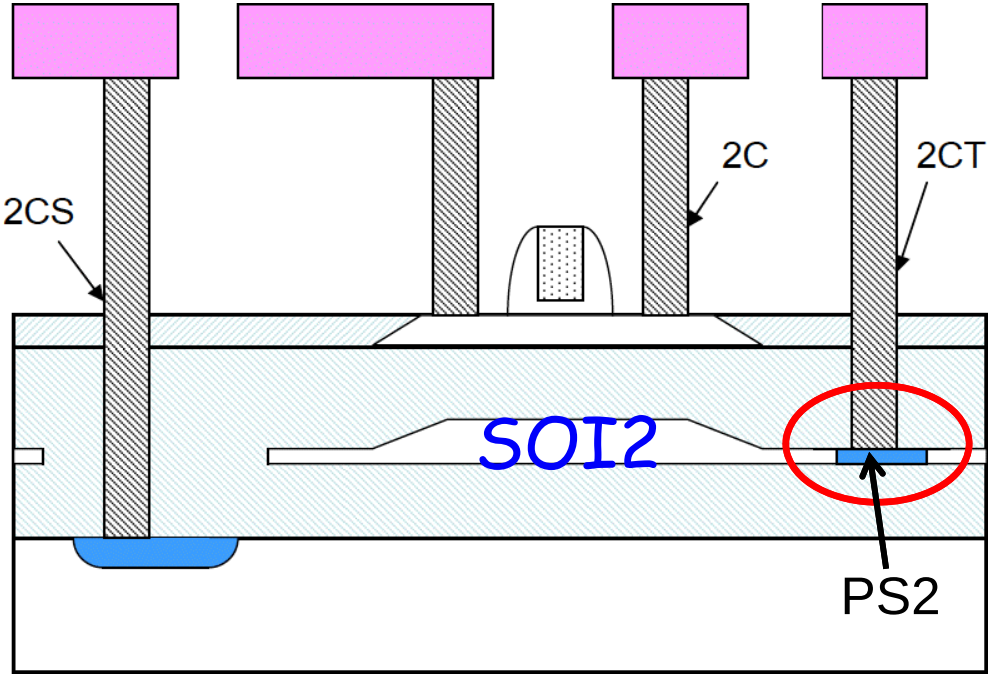
Then we newly introduced additional conductive layer under the transistors to reduce all effects (→ Double SOI).

Double SOI Process

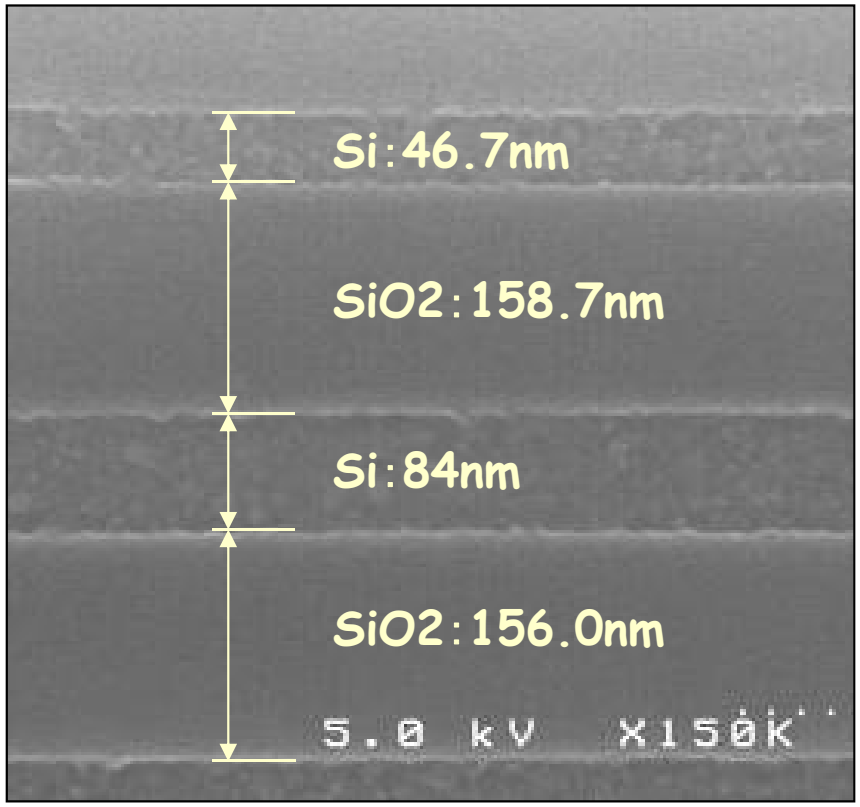
Middle Si Layer
(SOI2)

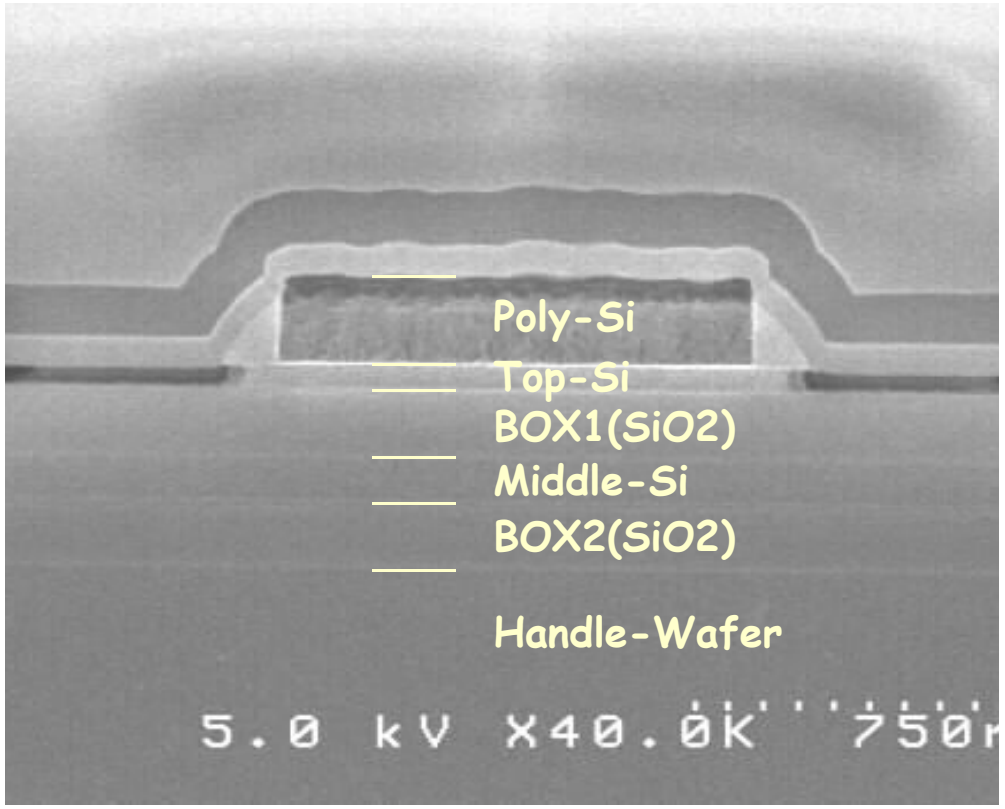
BW = BW or [NS] size +0.4um or [PS] size+0.4um
BW2 = BW2 or [PS2] size+0.4um





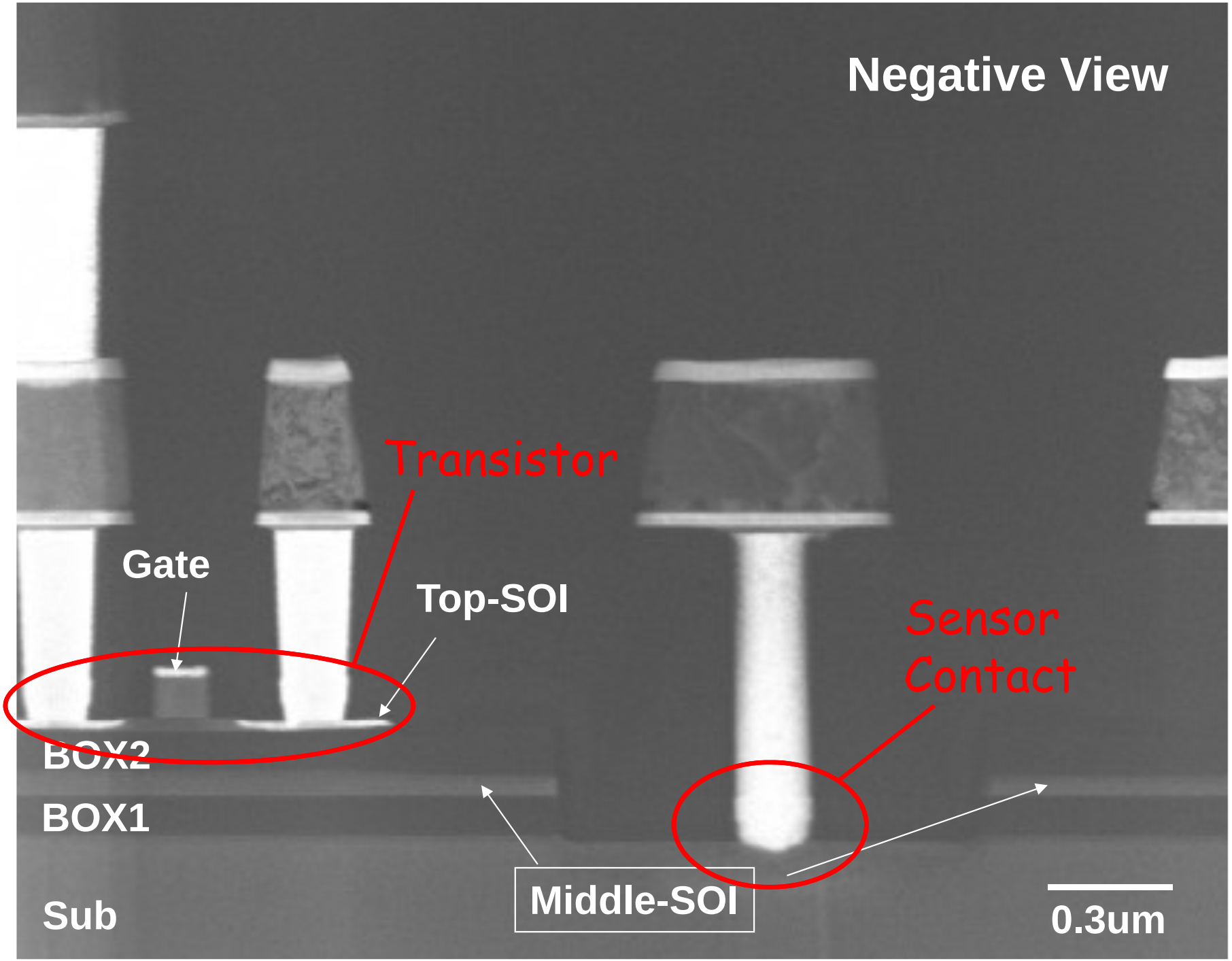
First Trial : Double-SOI from SOITEC





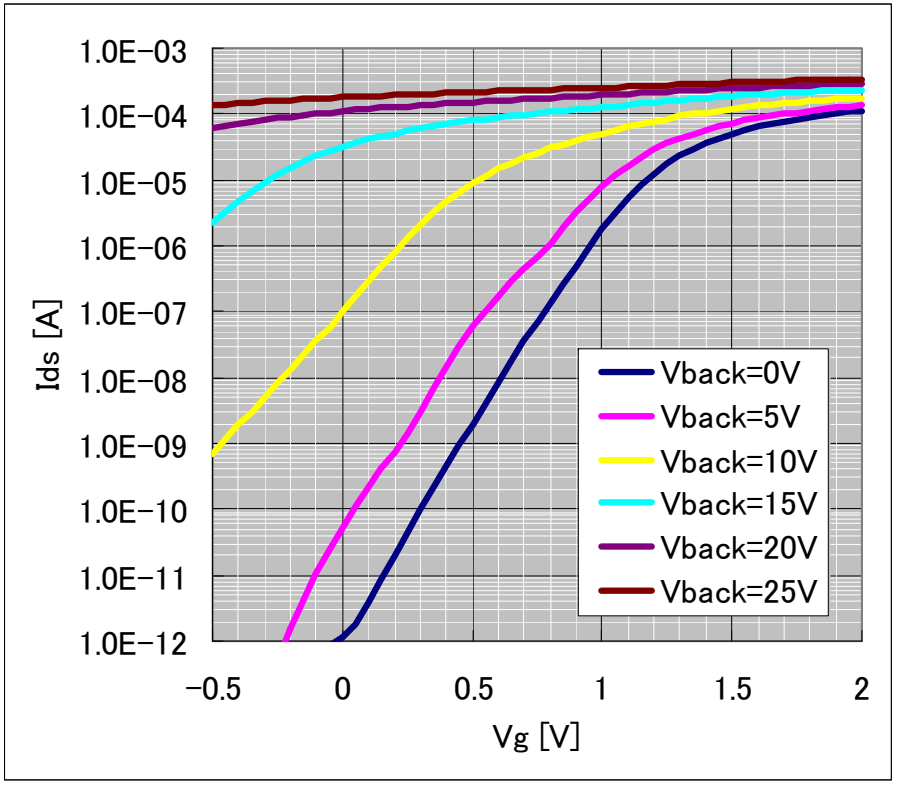
(after Field-Anneal)

Resistivity of the middle Si is ~10 Ohm•cm.
with CoSi2 : ~170 kOhm/ □
w/o CoSi2 : ~1 MOhm/ □

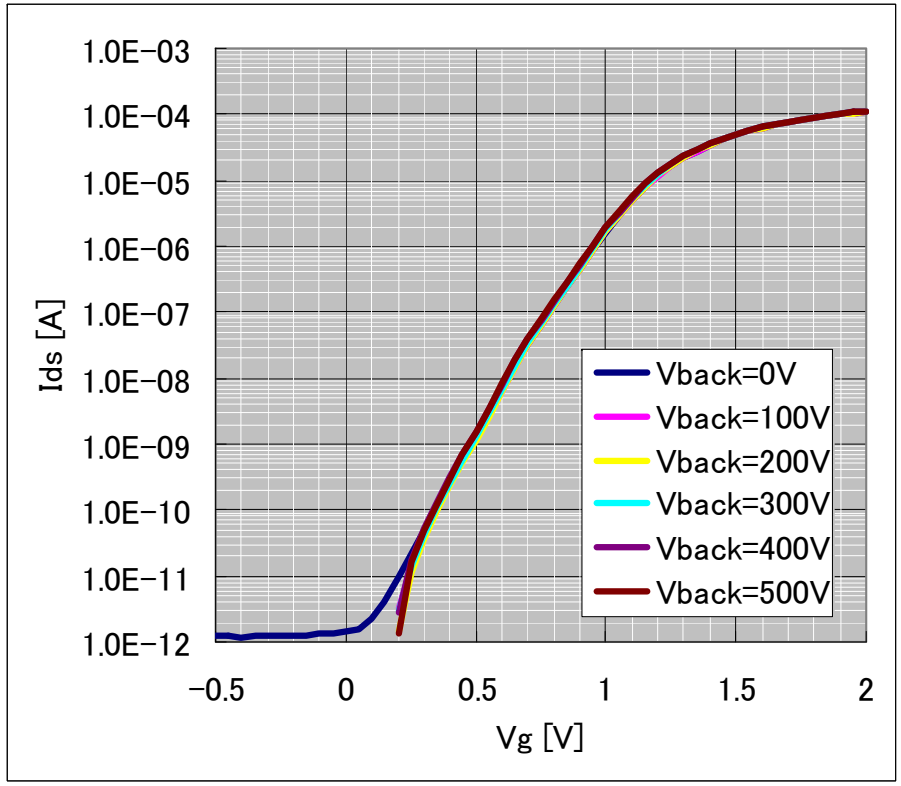

Negative View
Transistor
Gate
Top-SOI
Sensor
Contact
BOX2
BOX1
Sub
Middle-SOI
0.3um

Suppression of Back-Gate Effect with Middle-Si layer

a) Middls-Si Floating



b) Middle-Si = GND



Back-Gate Effect is fully suppressed with the Middle Si Layer of fixed voltage.

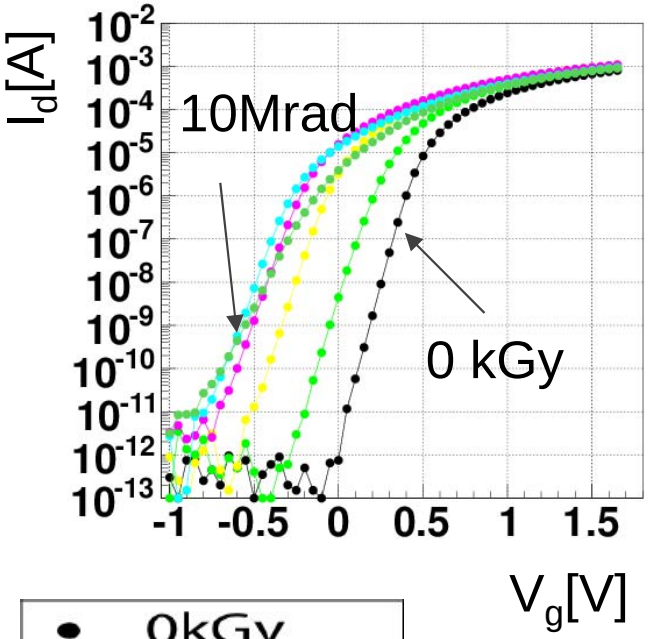
Nch Core Normal-Vt
L / W = 0.2 / 5.0um
Vd=0.1V

Gamma-ray Irradiation Test
(Id-Vg Characteristics v.s. SOI2 Potential)

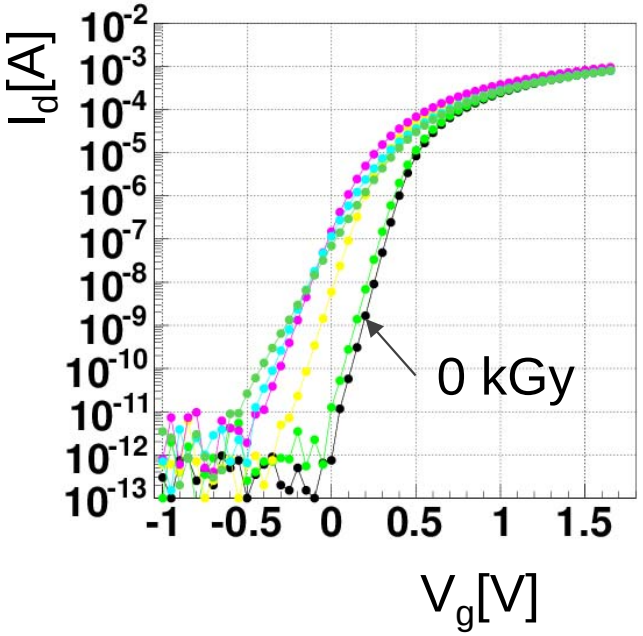
I/O normal Vth
Source-Tie Tr.
L/W =0.35um/5um

NMOS

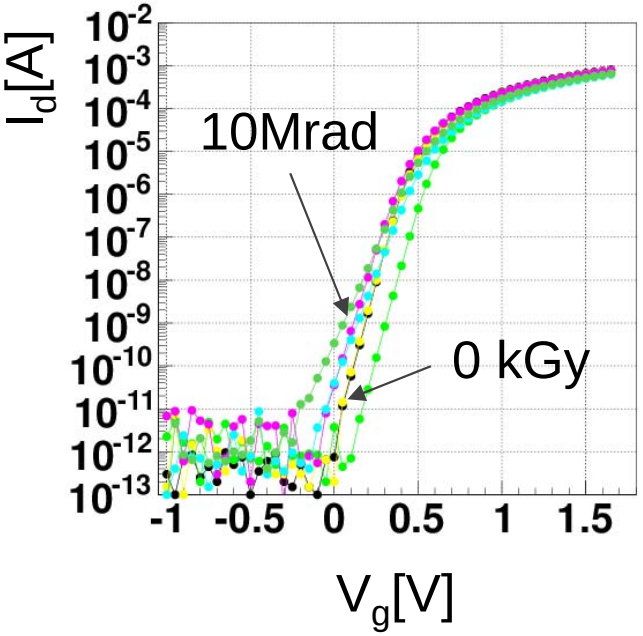
V_{SOI2}=0V



V_{SOI2}=-2V



V_{SOI2}=-5V



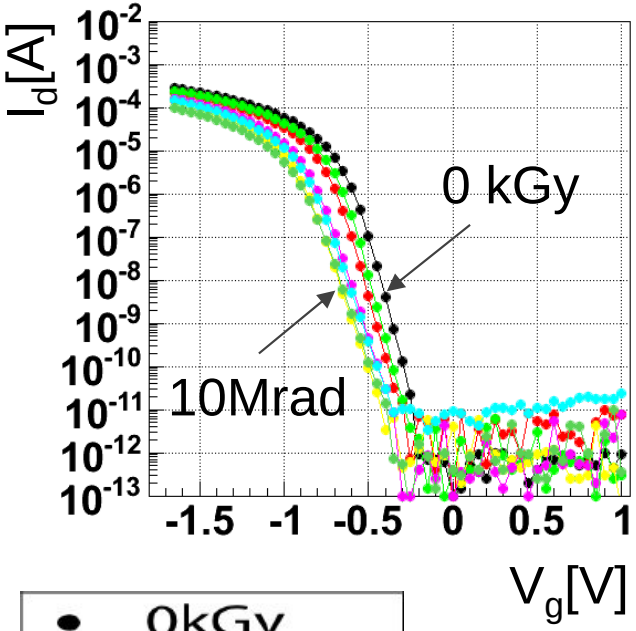
By setting Vsoi2 ~ -5V, Id-Vg curve returned nearly to pre-irradiation value.

Variation of Id-Vg Characteristics and Effect of SOI2 Potential

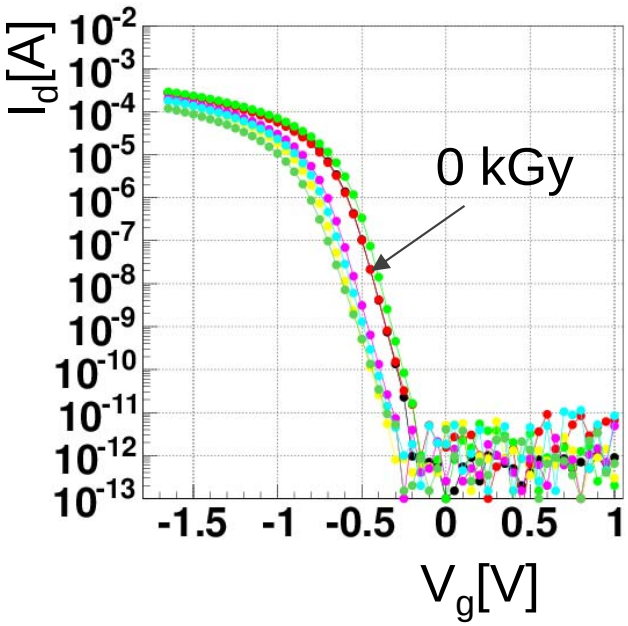
I/O Normal Vt
Source-Tie
L/W =0.35um/5um

PMOS

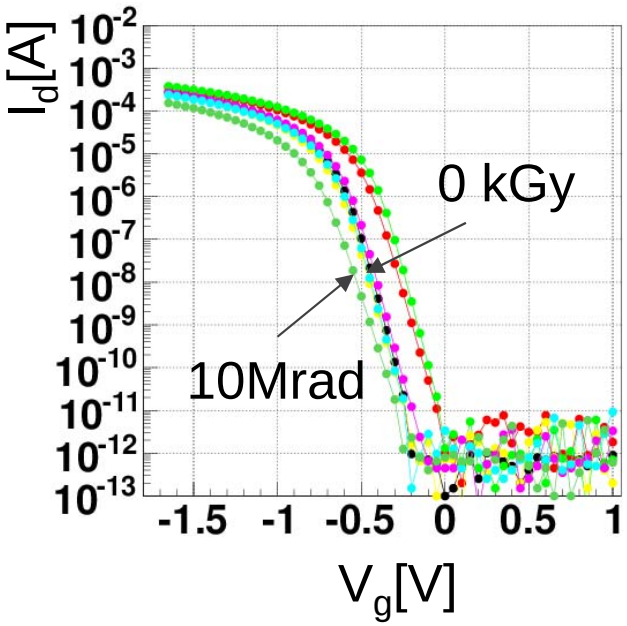
V_{SOI2}=0V



V_{SOI2}=-2V



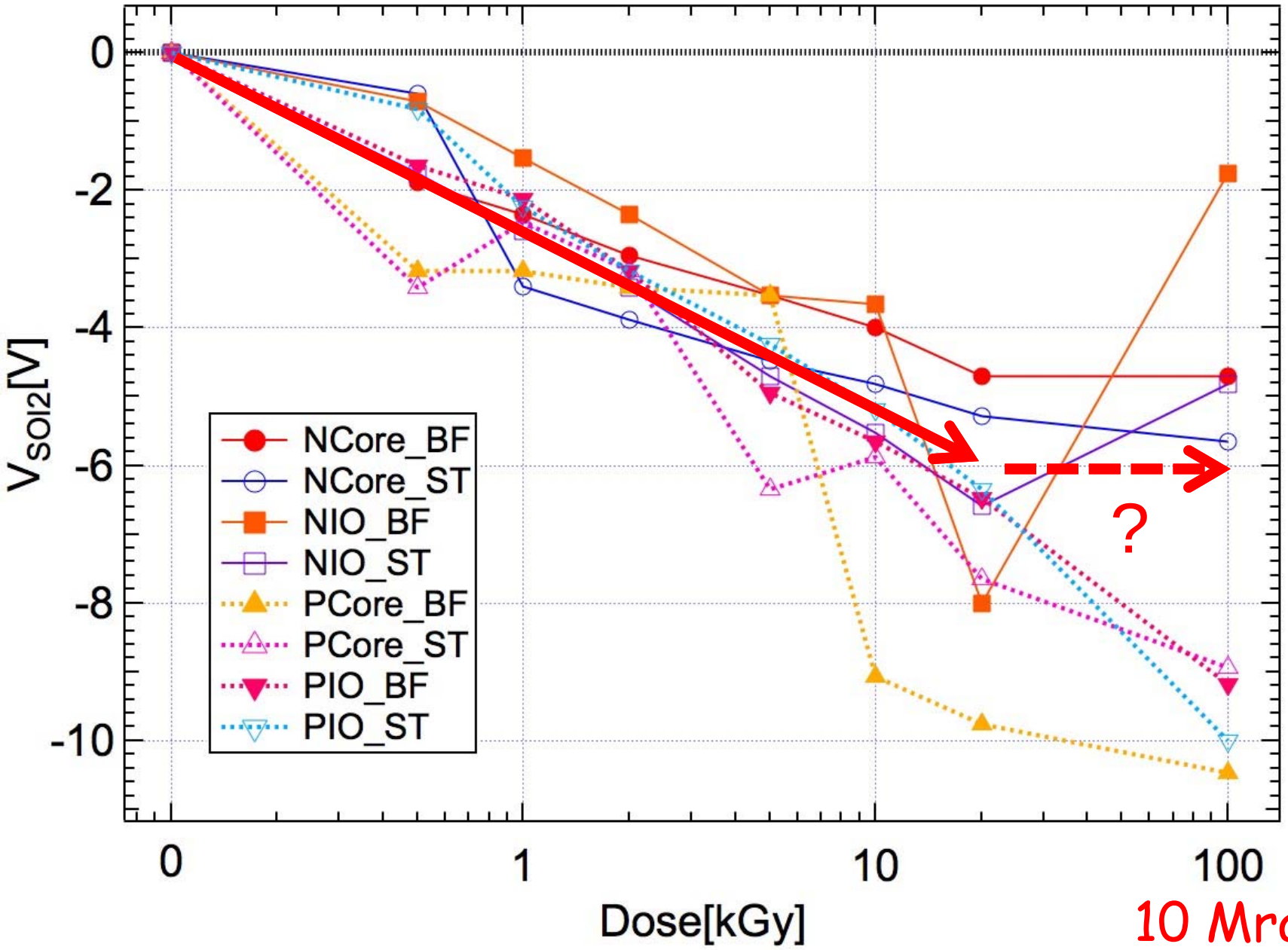
V_{SOI2}=-5V



The V_{SOI2} effect to PMOS is not so large compared to NMOS case.
Id-Vg curve also returned to pre-irradiation value @VSOI2~-5V.

Necessary V_{SOI2} voltage to restore original threshold voltage

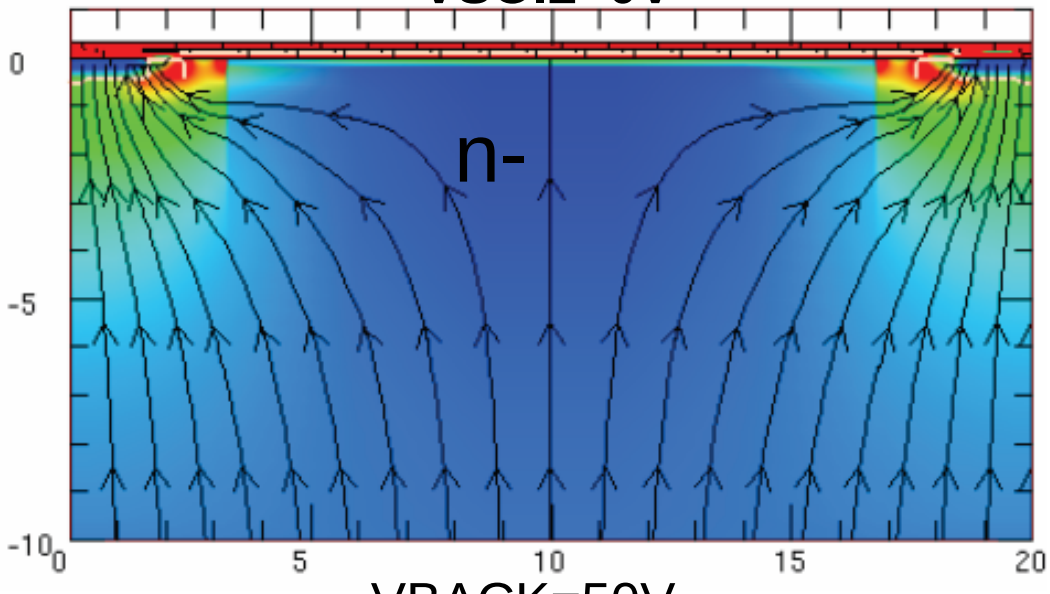
Preliminary!



Effect of Middle Si potential to Charge Collection

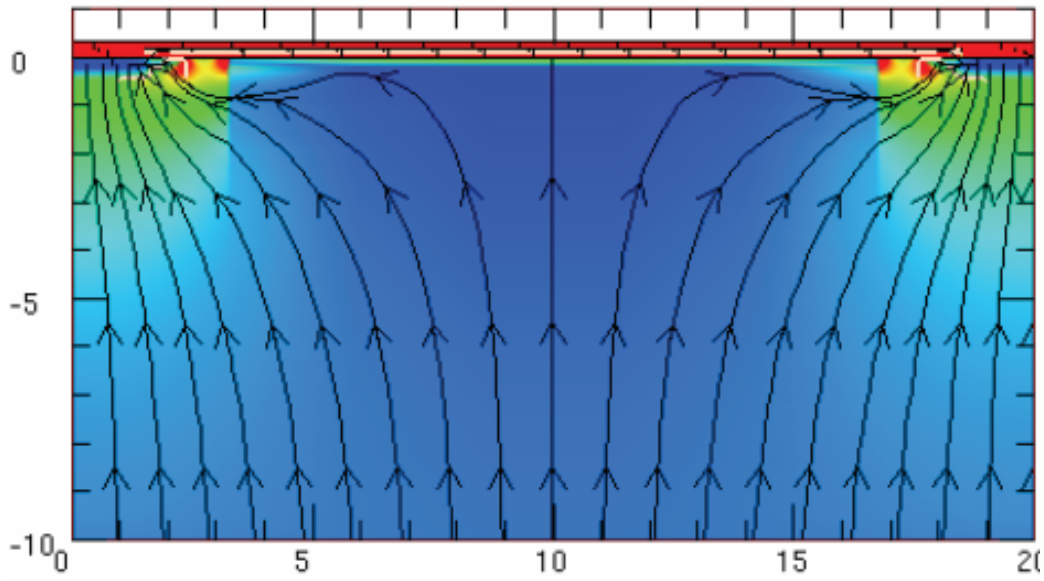
VSENSE=1V

VSOI2=0V



VBACK=50V

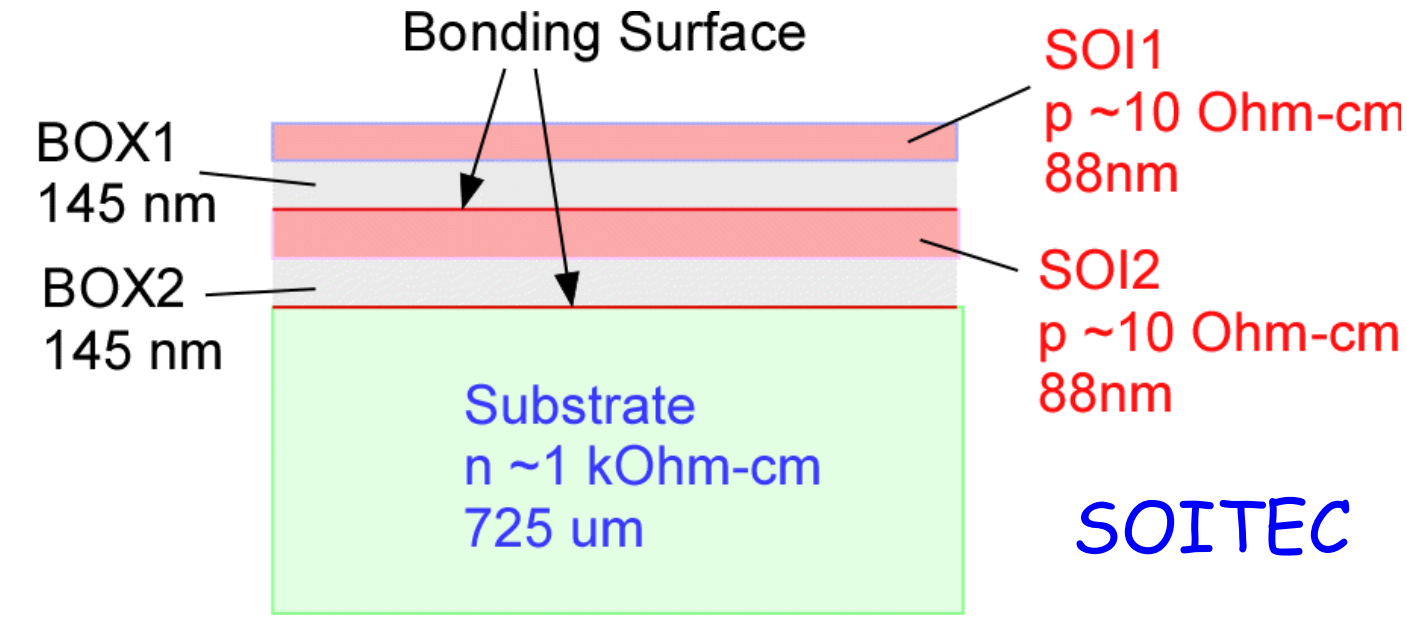
VSOI2=-2V



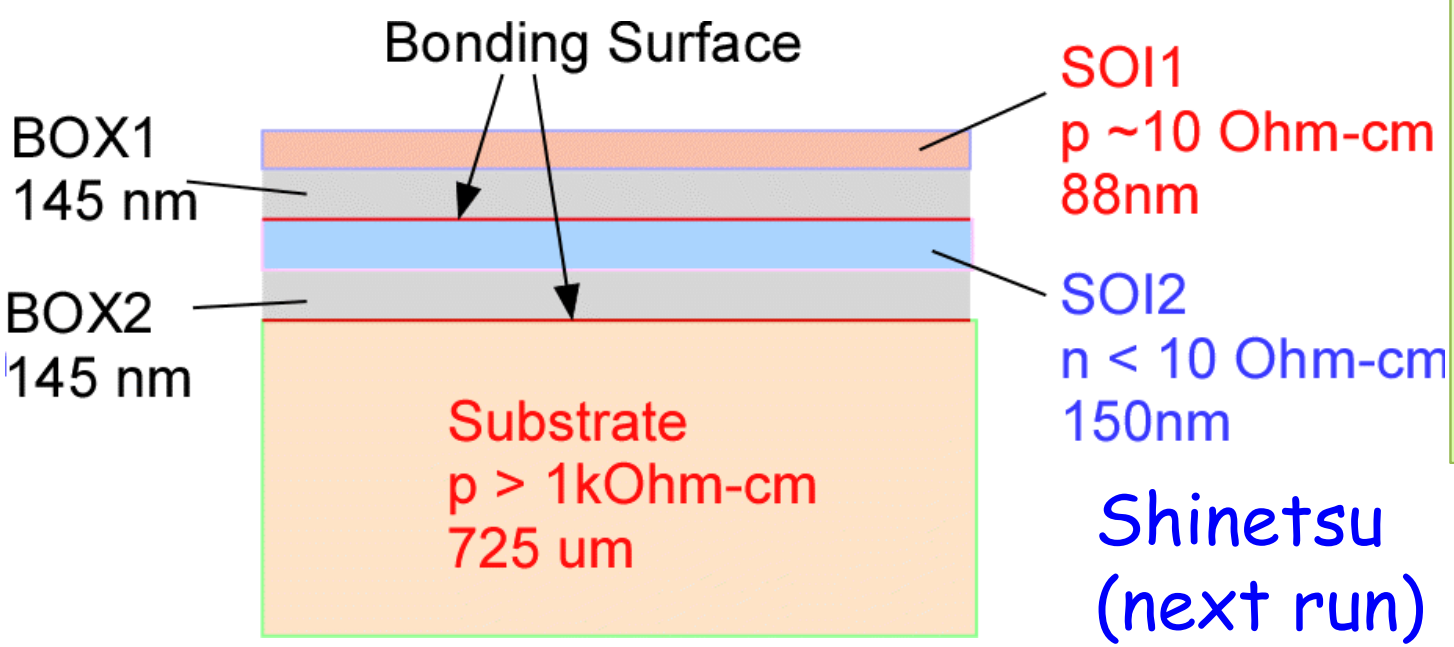
- To compensate trapped hole effect, → negative SOI2 voltage is necessary.
- To push electrical flux lines to sense node → positive SOI2 voltage is necessary.

It is better to use p-type substrate instead of n-type.

New DSOI Wafer



SOITEC

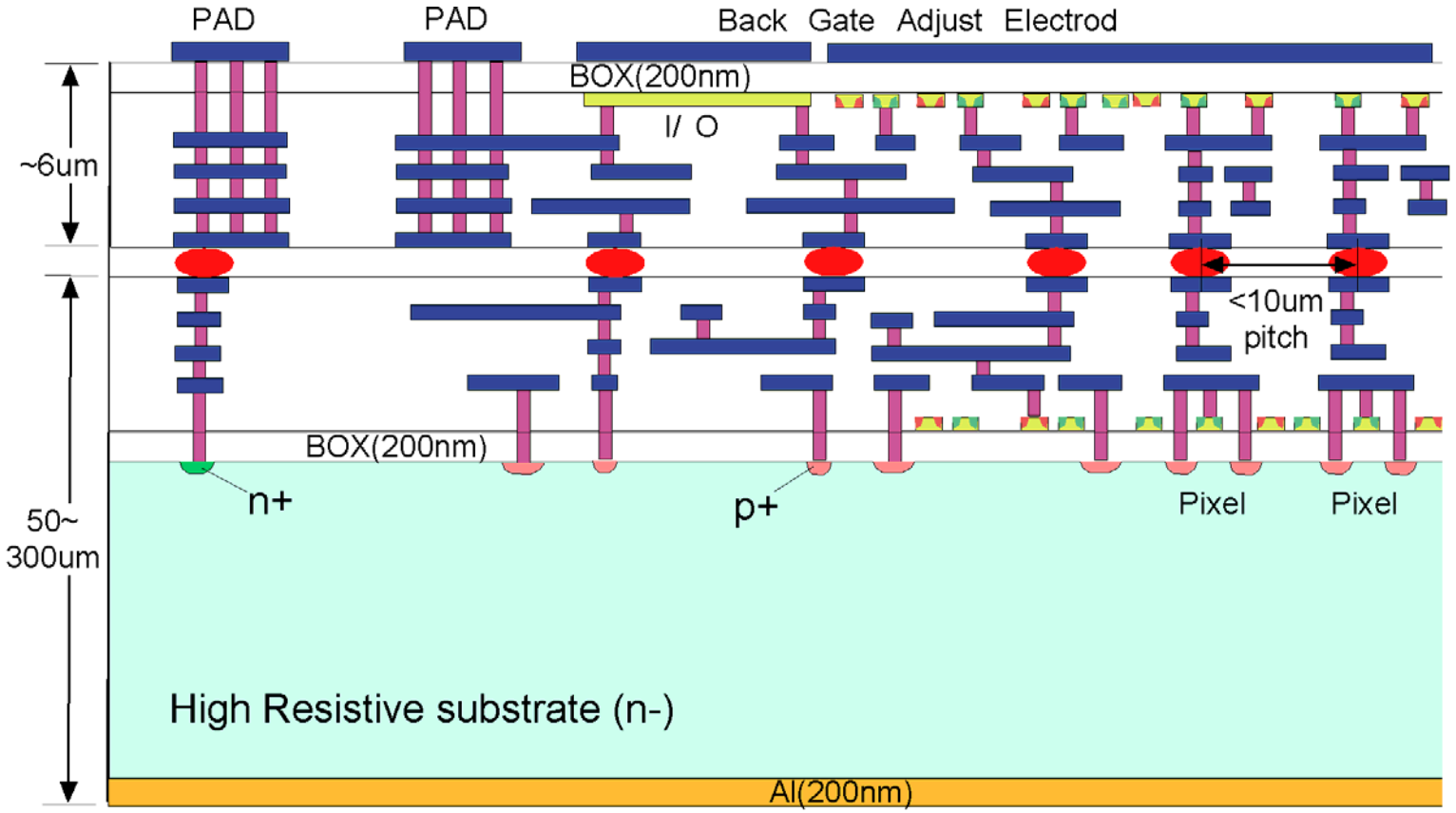


Shinetsu
(next run)

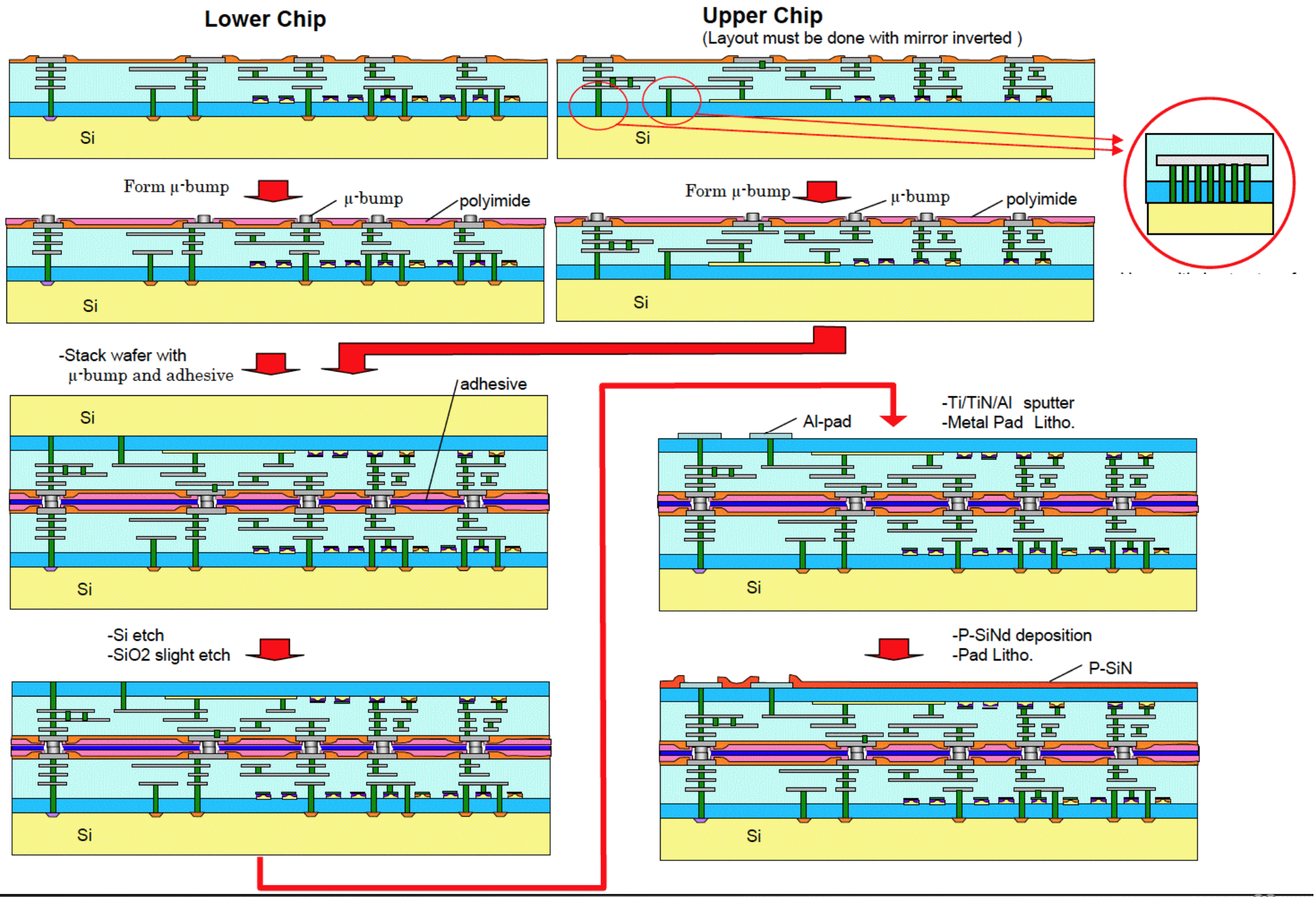
- Substrate is changed from n-type to p-type to have better field shape.
- Thickness of SOI2 is doubled to have lower resistance.
- Type of SOI2 layer is changed to n-type not to deplete the layer.
- Supplier is also changed.

Vertical (3D) Integration

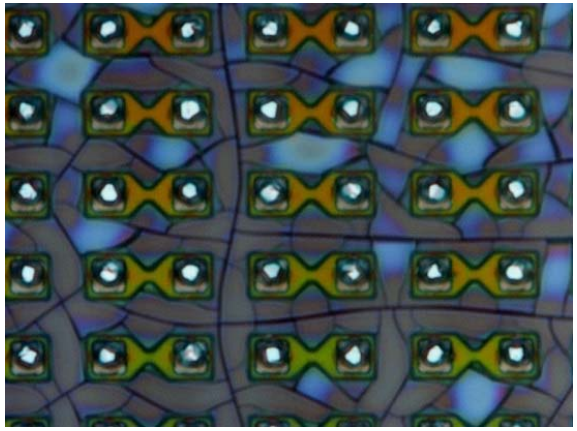
3D vertical Integration technique is expected to play an important role in future high performance pixel detector.
We have made 3D test chips. These chips were bonded with μ-bump technology (~5 um pitch) of T-micro Co. Ltd.



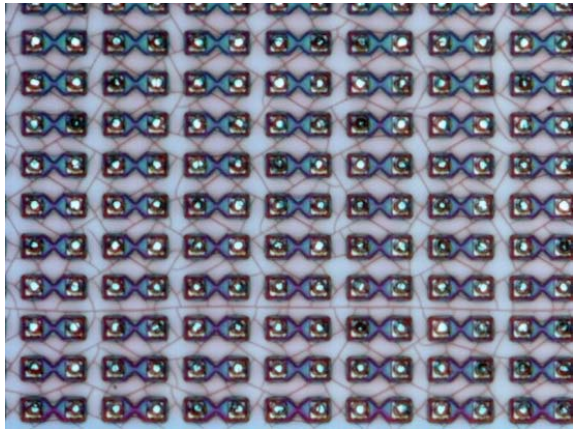
(1) Stack Process Flow (after finishing wafer process)



Daisy Chain TEG (After Deposition)

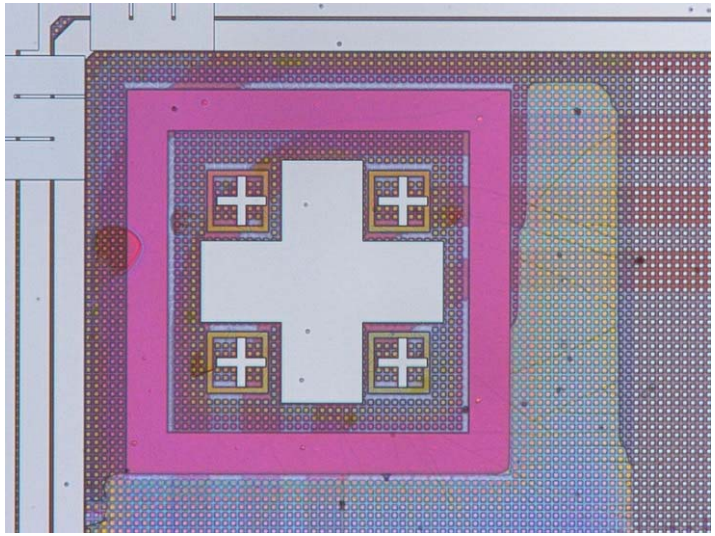


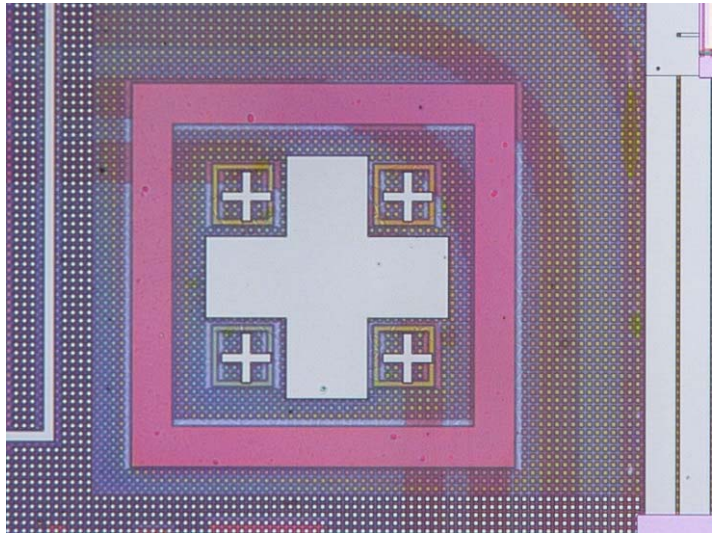
Upper Chip

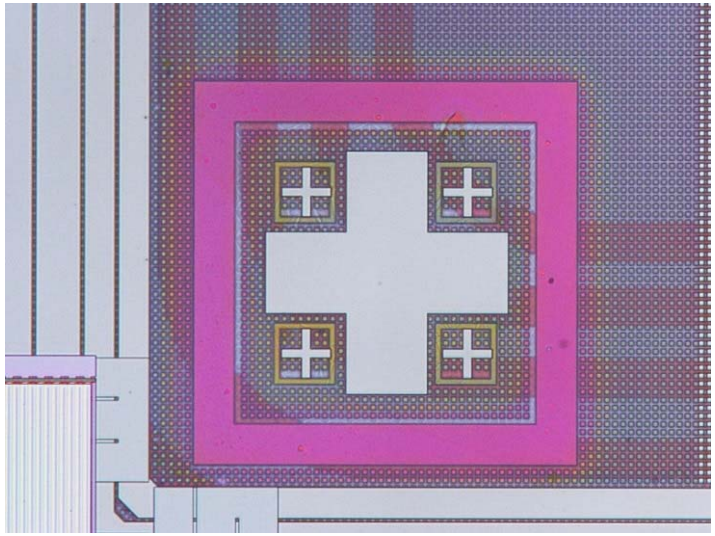


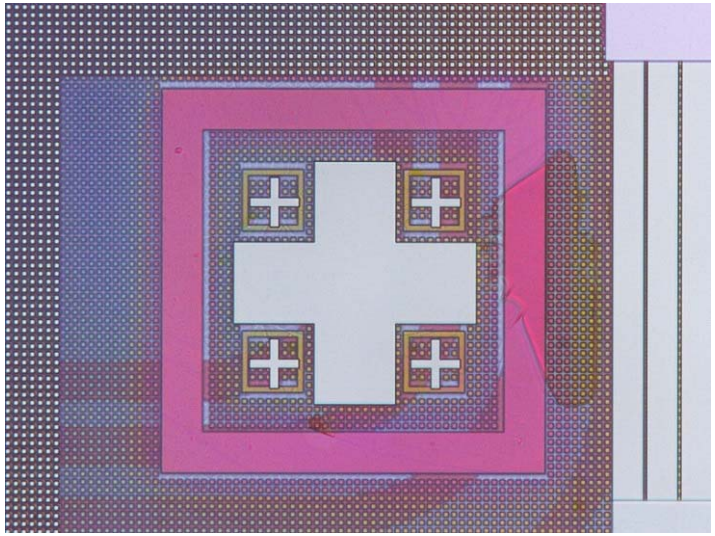
Lower Chip

Alignment Mark (After Stacking – Adhesive Injection – Si Wet Etching)





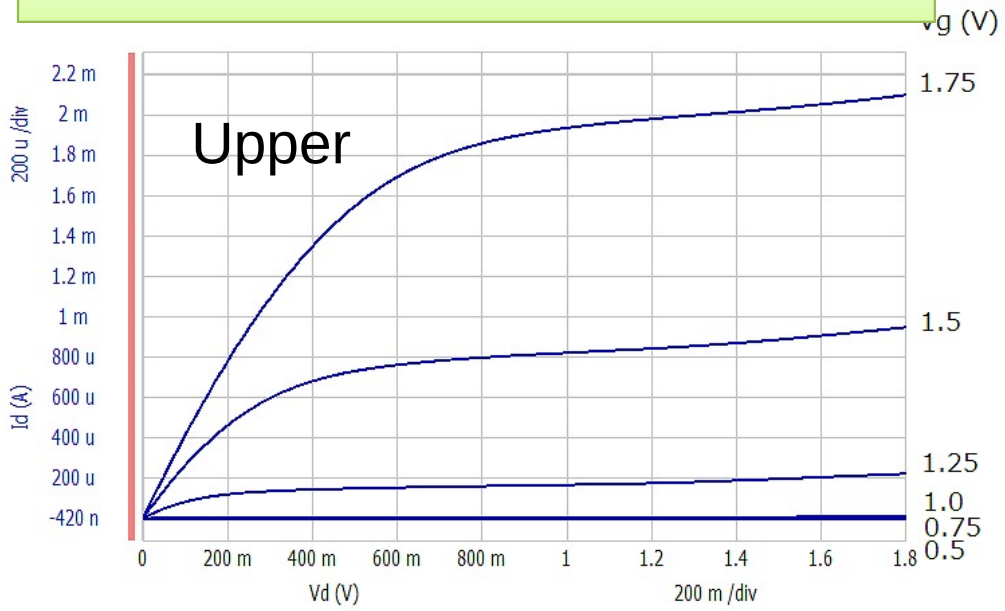


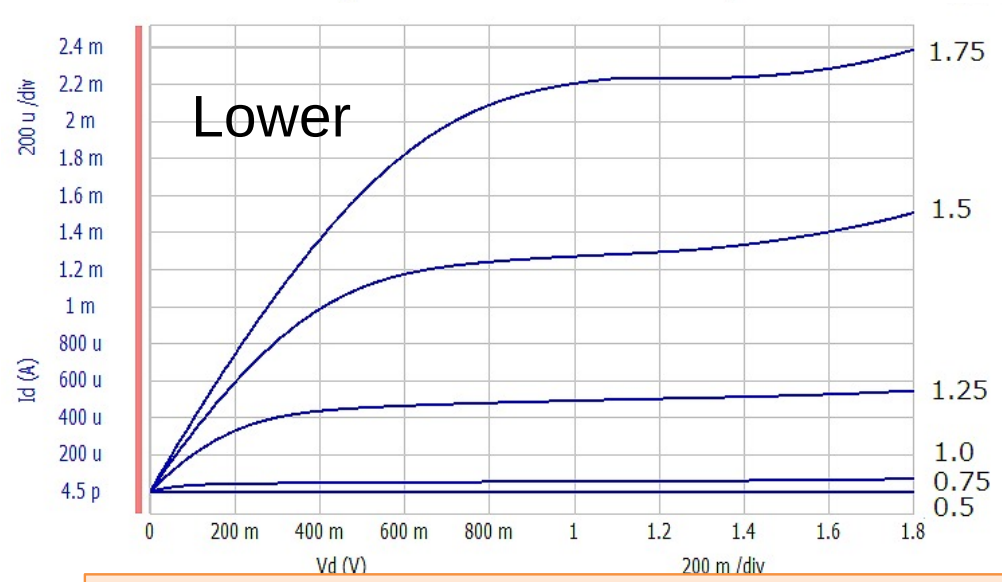


Id – Vd Characteristcs

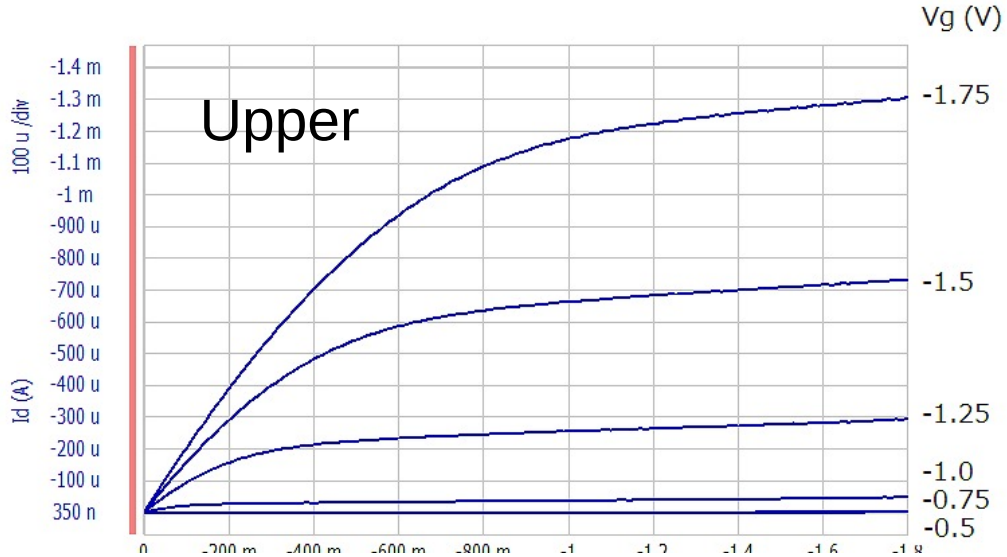
Preliminary!

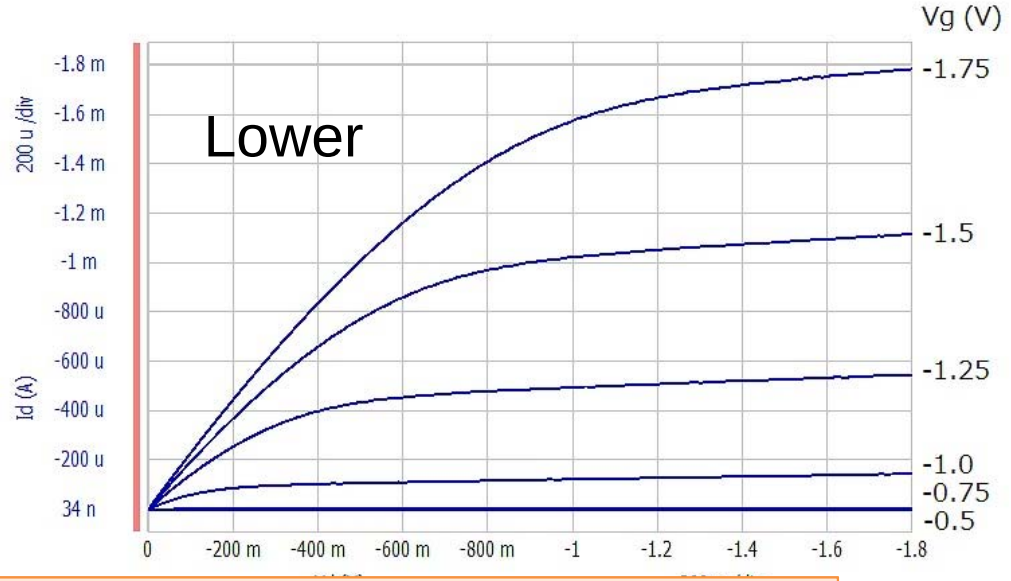
NMOS Source-Tie w/l=32u/0.35u





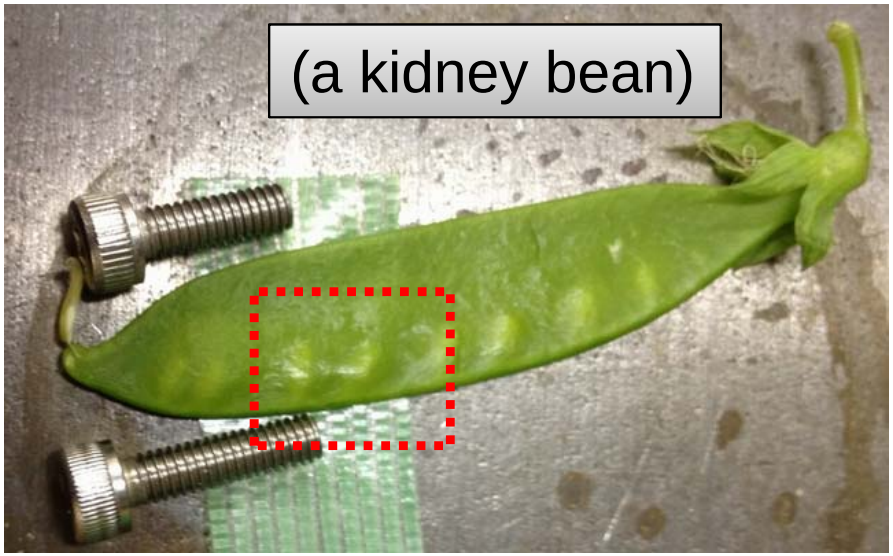
PMOS Body-Tie w/l=50u/0.35u



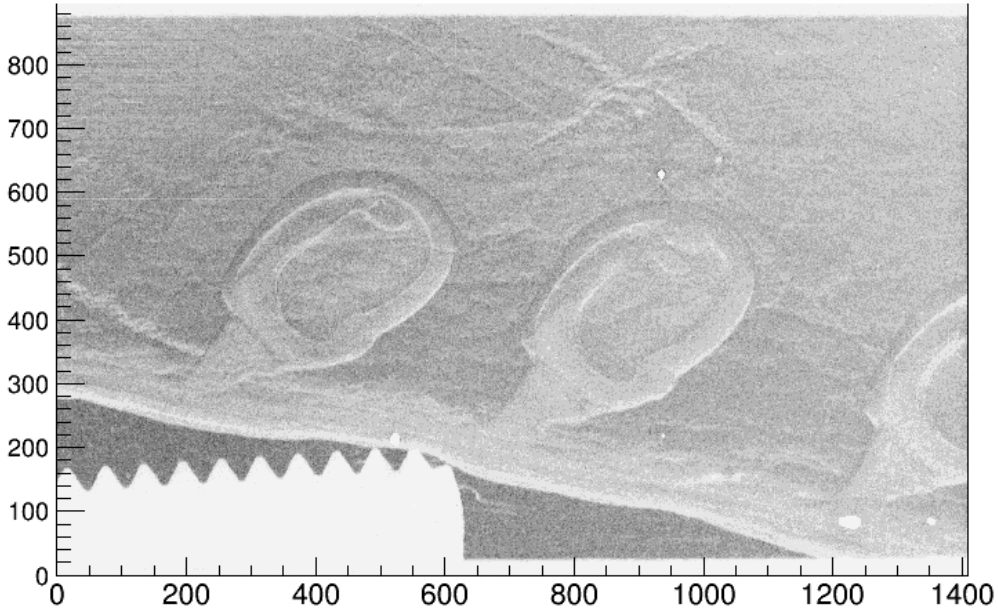


Id-Vd characteristic looks different between upper and lower tiers.

Project Status



Diffraction Enhanced (Low angle) Image



On-Going SOI Projects in Japan

- INTPIX : Genera Purpose Integration Type → KEK
- SOPHIAS : Large Dynamic Range for XFEL → Riken
- PIXOR : Belle II Vertex Detector → Tohoku Univ.
- XRPIX : X-ray Astronomy in Satellite → Kyoto Univ.
- STJPIX : Superconducting Tunnel Junction on SOI
  → Tsukuba Univ.
- CNTPIX : General Purpose Counting Type → KEK
- LHDPIX : Nuclear Fusion Plasma X-ray → KEK, NIFS
- MALPIX : TOF Imaging Mass Spectrometer
  → KEK, Osaka Univ.
- TDIPIX : Time Delaying Integration for X-ray Inspection
  → KEK
- …

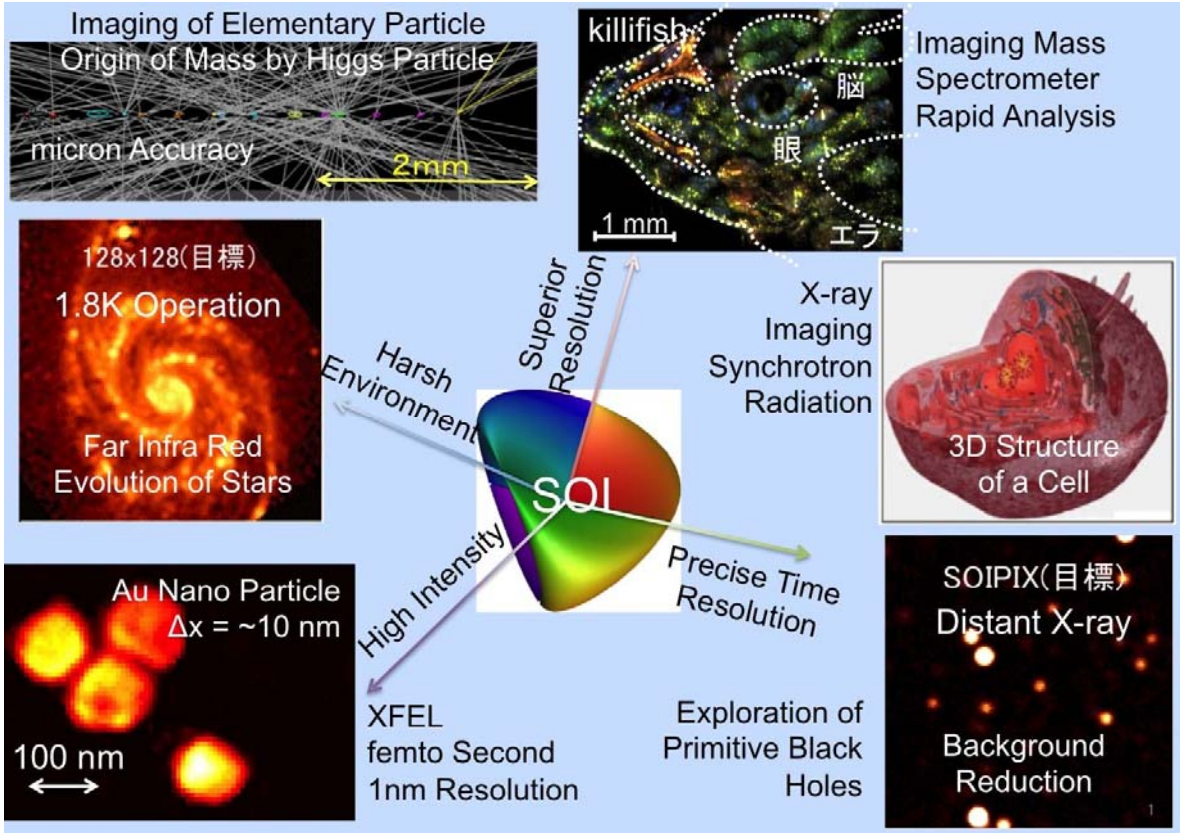
and Many Other Project are being planned

【Grant－in－Aid for Scientific Research on Innovative Areas(Research in a proposed research area)】

Science and Engineering

Title of Project Interdisciplinary research on quantum imaging opened with 3D semiconductor detector

High Energy Accelerator Research Organization (KEK), Institute of Particle and Nuclear Studies, Professor, Yasuo Arai



SOI project of 5 years is granted!

【Term of Project】

FY2013-2017

【Budget Allocation】

~$10M

Summary

- We have been developing SOI Pixel process and fabricated many kinds of SOIPIX detectors which integrate both radiation sensors and readout circuits in a single die.
- We have ~twice/year regular MPW runs with increasing No. of users.
- Many new process technologies have been developed; Buried P-well, High resistive SOI wafer, Nested well structure, Stitching, Double SOI, Vertical integration …
- Double SOI of p-type substrate looks promising for rad-hard counting-type pixel detector.
- New SOI project of 5 year period is approved by Japanese government.