PROCEEDINGS OF SCIENCE

SOI detector developments

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The novel particle and radiation detector using a Silicon On Insulator (SOI) technology has been developing by the SOI collaboration since 2005. The SOI technology can be applied to realize an ideal monolithic detector which consists of electrical insulator sandwiched low resistivity thin wafer for electronics and high resistivity thick wafer for sensor without bump bonding. The multilateral developments for both fundamental properties and dedicated application are progressing simultaneously. The one of the most important break through we had achieved is a buried p-well (BPW) technology. This technology help to lead recent various applications for specific scientific interest such as X-ray diffraction analysis, X-ray astronomy and high energy particle detector. We report recent studies of process based improvements, radiation tolerance and high energy particle tracking.

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1. Introduction

The SOI pixel detectors are fabricated by the OKI Semiconductor Co. Ltd. $0.2\mu m$ CMOS fully depleted (FD-)SOI process[1]. The SOI pixel detector is jointly developed by KEK and SOI collaboration with OKI Semiconductor Co. Ltd.[2]-[5]. The SOI detector consists of three layers: a thin low resistivity(Cz, $\sim 18\,\Omega$-cm, p-type) *Si* layer used for CMOS circuit, a buried oxide (BOX) used for electrical insulator, and a thick and high resistivity(Cz, 700Ω-cm, n-type) substrate used for sensor in Figure 1. The each thickness is $40nm$, $200nm$ and $260\mu m$, respectively.

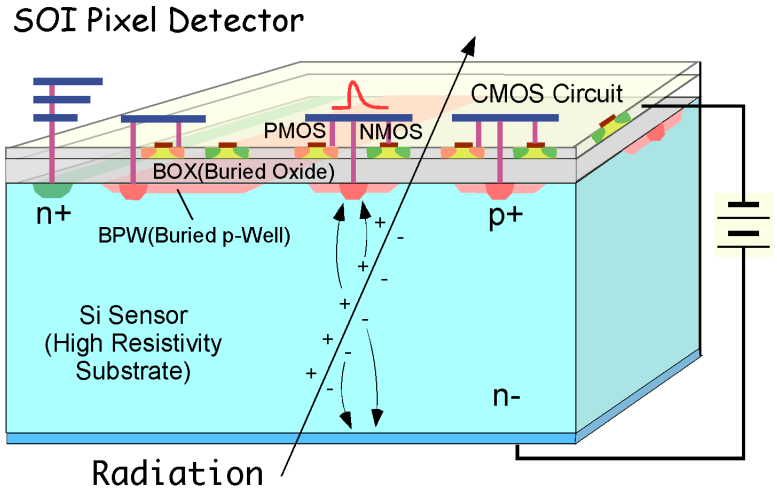

Figure 1: Block diagram of SOI pixel detector structure.

The SOI technology provides attractive advantages as follows: 1) There is no mechanical bump bonding that allow us to implement high density circuits and fine pixels without additional material budget. 2) Naturally, low parasitic capacitance through the substrate in SOI can be achievable to low noise and large gain. 3) Standard CMOS circuits can be implemented in the SOI layer. 4) Developing vertical integration (3D) technology is natural extension of the SOI technology. 5) The SOI device is as known as rad-hard devise for single event effects (SEE).

The various pixel detectors and TEGs have been submitted by the SOI collaboration in a multi project wafer organized by KEK approximately twice in a year since 2006.

2. Developed SOI pixel detector

The SOI pixel detector can be classified into two types, an integration type detector named INTPIX and a counting type detector named CNTPIX[6]. Up to now, the both series are progressed into finer pixel segment and more sophisticated functions implemented in a pixel.

2.1 INTPIX

The integration type detector integrates the generated carriers during a time in the capacitor. Then, the carriers are read out as a voltage. The first INTPIX with 32×32 arrays of $20\mu m$ square pixel in 2.4 *mm* square chip had been developed in 2006. Since 2007, several INTPIX series in

Process	$0.2\mu m$ FD-SOI CMOS 1 Poly, 4(5) Metal layers, MIM condenser DMOS option Core(I/O) voltage = 1.8 (3.3) V
Wafer	Diameter: 200 $mm\phi$ Top silicon (SOI layer): Cz, $\sim 18\Omega \cdot cm$, p-type, thickness(t) $\sim 40nm$ Buried Oxide (BOX): 200nm Bottom silicon (Handle wafer): Cz, $700\Omega \cdot cm$, n-type, $t \sim 725\mu m$
Backside treatment	After the processing, thinned down to 260 μm. Sputtering Al (200 nm)
Transistor	Standard and low V_{th} transistor for core and I/O, respectively. Three types of structure: body-floating, source-tie and body-tie.
Option	BPW (Buried p-well) and 3D integration.

Table 1: Specification of SOI process for radiation sensor.

chip size 5 mm square had been developed and the number of pixels reached at 128×128 pixels. Latest the series of INTPIX4 chip is $10.2mm \times 15.4$ mm and has 512×832 arrays of $17\mu m$ square pixel. The INTPIX4 has 13 parallel analog output lines and correlation double sampling (CDS) are implemented to reduce the noise.

The schematic of the INTPIX4 is shown in Figure 2.

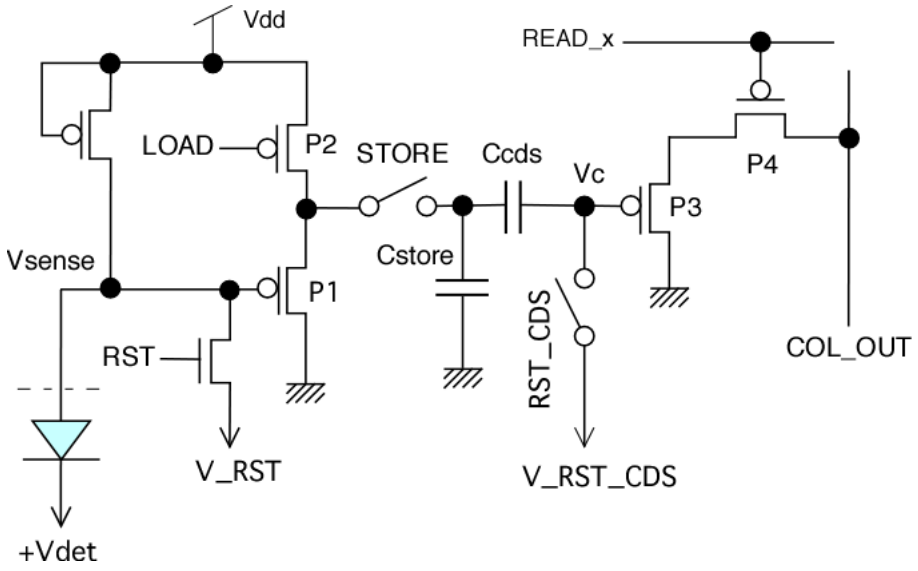

Figure 2: Block diagram of pixel in INTPIX4.

2.2 CNTPIX

The counting type detector counts the signal responses over the variable threshold. The first CNTPIX1 chip with 128×128 pixels had been developed in 2006. The latest CNTPIX5 chip is

72×216 arrays of a 64μm square pixel. The CNTPIX5 chip size is 5.0 mm × 15.4 mm. The chip has the double threshold V_{thH} and V_{thL} in each pixel to count a specific energy signal. The thresholds are common to all pixels with 3-bits adjustment for each pixel for fine turning. After the analog signal is discriminated, digital is counted by 9-bits × 2 counters. The counters also can be used 18-bits and combined 9-bits × 8 counters with adjacent 4 pixels.

The schematic of the CNTPIX5 is shown in Figure 3.

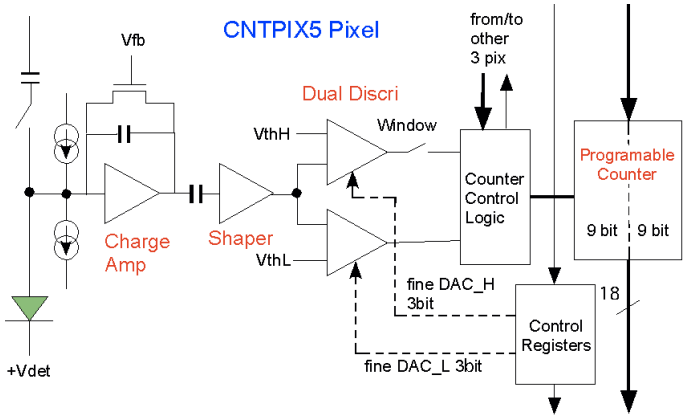

Figure 3: Schematic of pixel in CNTPIX5.

3. Progresses in SOI process and post-process.

The improvement of wafer level and both processing and post-processing had been attempting so far. In this section, we introduce major topic of the improvements.

3.1 High resistivity FZ wafer

The FZ wafer of 7 $k\Omega \cdot cm$ resistivity is newly introduced in the sensor wafer. The thickness of the INTPIX3e introduced FZ sensor is thinned down to the 500 μm and tested to measure the full depletion voltage with exposing the red laser from backside window. The full depletion voltage can be estimated from the saturation of output signals at an applied sensor bias. Calculated and measured value of the full depletion voltage is in good agreement and is about 80 V.

3.2 New mask

The size of the present reticule is 20.8 mm × 20.8 mm and limits the maximum chip size. A larger reticule (24.68 mm × 30.58 mm) will be available in the FY2011-2.

3.3 Buried p-well (BPW)

The SOI structure has the symmetrical structure flipping with gate and back gate (handle wafer) terminal. This causes the back gate can control channel between drain-source(back gate effect). Before introducing the buried p-well(BPW) in SOI detector, the back gate effect was the most critical problem since we couldn't apply big sensor bias voltage to deplete fully. The BPW is

fabricated with implantation through the BOX and the SOI layer without holes. The implant energy and flux was tuned not to affect the characteristics of transistor with simulation. Figure 4 shows the variation of $I_{ds}-V_{gs}$ characteristics of a transistor due to the sensor voltage (V_{back}). Without the BPW (a), the $I_{ds}-V_{gs}$ characteristic is largely affected by the V_{back}. However, by introducing the BPW (b), there is no change in the $I_{ds}-V_{gs}$ characteristic even applying 100 V to the sensor.

In addition , we found that the BPW relaxes the electric field at the edge of guard-ring. Resulting, the breakdown voltage is increased.

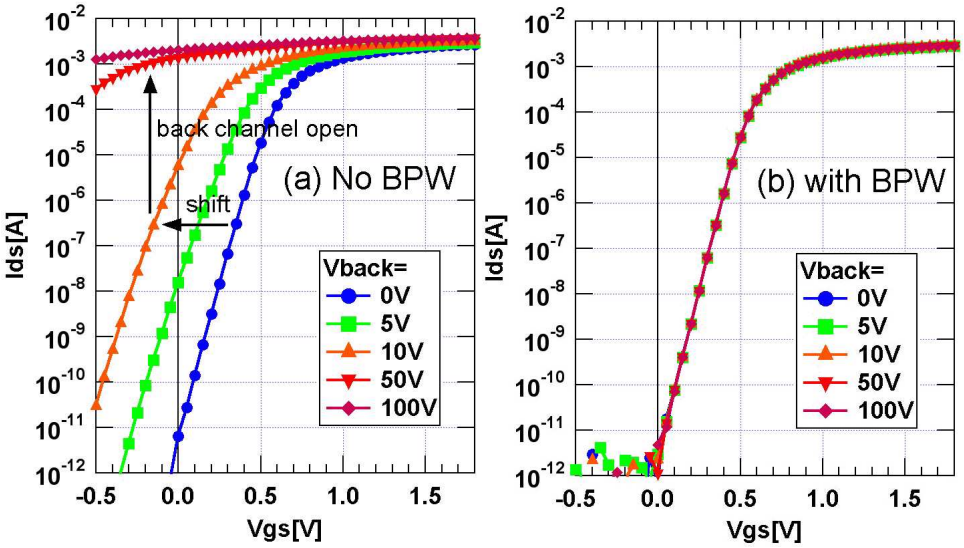

Figure 4: Suppression of backgate effect with and without BPW.

3.4 Wafer thinning

After the SOI processing of SOI wafer, the backside of the wafer was ground from 725 μm to typically 260 μm thickness and sputtered with aluminum for the backside contacts. Further thinning $\sim$100 μm was evaluated for low material budget from recent experimental request while maintaining an adequate signal to noise ratio for charged particle traversing the pixel detector.

The wafer was thinned commercially with the TAIKO process developed by DISCO. Co.. TAIKO is name of the grinding technology where the wafer is ground leaving an edge $\sim$3 mm from the outer most circumference of the wafer. Handling of thinned wafers becomes easier since the leaved edge reduces the warpage and increases the stiffness of wafer.

The thinned wafer was diced into INTPIX3b chips to evaluate the thinning quality. The leakage current, warp profile, and response to IR and RED laser test have been performed. The results show small increase in the leakage current, demonstrating a fully depleted pixel sensor at expected performance. The thinned INTPIX3b chips were tested in a 672 MeV/c positron beam at the Laboratory of Nuclear Science in Tohoku University. The detail is presented in Section 5.

4. Radiation tolerance

The radiation tolerance is one of the crucial performance issues as a particle detector. The SOI device is known as a radiation hard device for SEE. On the other hand, the total ionizing effect (TID) on the SOI device may be affected since its relatively thick silicon dioxide layer, BOX. We are evaluating both SOI transistor device level and detector level with various radiation sources: X-ray, γ-ray, electron and proton. Irradiated DUTs are INTPIX3 chips which contain transistor TEGs (TrTEG) in the peripheral region. The TrTEG consists of two groups of TrTEG with and without BPW. Each group contains 7 NMOS and 6 PMOS transistors having various W/L and body-tie types.

The ^{60}Co γ irradiation was performed at the JAEA Takasaki Advanced Radiation Research Institute. The 70 MeV proton irradiation was carried out at the Cyclotron Radio Isotope Center (CYRIC) of Tohoku University [7]. The $I_{ds}-V_{gs}$ curves were measured for the two groups with and without BPW in both irradiations. The transistors with BPW are stable up to $5kGy$ ^{60}Co γ. As for the proton irradiation, the $I_{ds}-V_{gs}$ curves are unchanged at 1.3×10^{12} $1-MeVn_{eq}cm^2$[9]. These two results are consistent that the BPW is effective up to several kGy[10].

The X-ray irradiation was performed in the KEK with the Rigaku XRD. During the irradiation, the sensor bias voltage was applied 100 V, the other transistor terminals and BPW being grounded. The $I_{ds}-V_{gs}$ curves were measured by the Agilent 4156C at the integrated radiation dose 0 krad(No irradiation), 30 krad and 100krad, respectively. The Figure 5, 6 shows the threshold voltage shifted according to the integrated radiation dose. On the other hand, transistor without BPW shows that the drain source terminals are conducted and the transistor characteristics were disappeared.

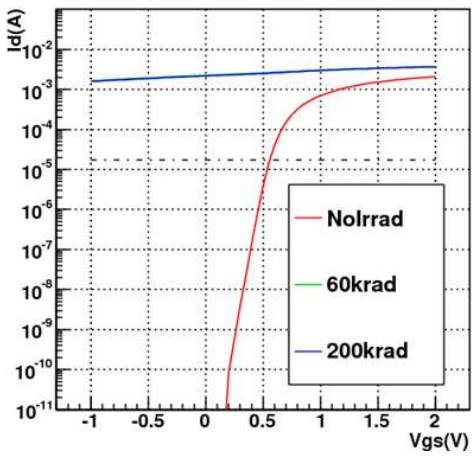

Figure 5: SOI NMOS $I_{ds}-V_{gs}$ curve without BPW.

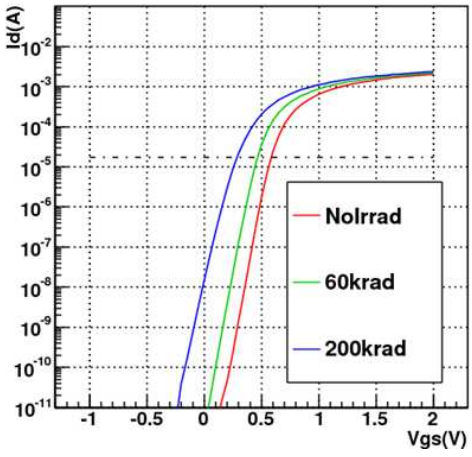

Figure 6: SOI NMOS $I_{ds}-V_{gs}$ curve with BPW.

5. Particle tracking

The MIP beam test at the Electron/Positron test beam line in Tohoku University[11] had been performed Oct. 2010. The incident γ's from STB ring using internal target wire are converted into the electron and positron pairs at the Tungsten target of 200 μm thickness. The generated positrons and electrons are bent by the magnet, and transported to the experimental hall through the $20mm\phi$

slit to choose semi-monochromatic momentum. Our SOI pixel telescope located at the positron beam line.

The SOI pixel telescope consists of three layers of INTPIX3b and two layers of CNTPIX4 detectors. Each detector is read out and controlled by SOI Evaluation Board with SiTCP (SEABAS)[12]. The telescope is sandwiched by three finger scintillator+PMTs to generate trigger timing signal. The INTPIX layers are periodically reset and integration at every $100\mu sec$. The CNTPIX layers are also periodically reset the counter at the same timing of INTPIX. The common clock and initialization signal are provided to all SEABASs from outer logic module. In addition, each triggered time from periodical reset in each SEABAS is recorded to assure that the triggered event data in each layer is in same time window.

Accumulated data is analyzed as follows procedure: pedestal subtraction for each pixel, noise rejection $< 5\,\sigma$ of pedestal distribution, clustering the adjacent pixel in 3×3 region, rough alignment correction, atrack finding, tracking, precise alignment correction, and final tracking. The residual distribution between fitted track and associated hit cluster position in detector plane is shown in Figure 7. We also exchanged the one of the INPIX3b chip to the thinned down to $100\mu m$ thickness with TAIKO process. The ADC distribution is shown in Figure 8. The both the plots behave like Landau distribution. These results are consistent with our expectation. Thus, we concluded MIP tracking is succeeded with SOI pixel telescope.

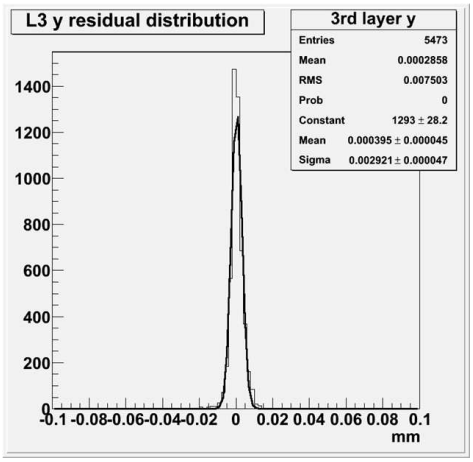

Figure 7: Residual distribution including multiple scattering

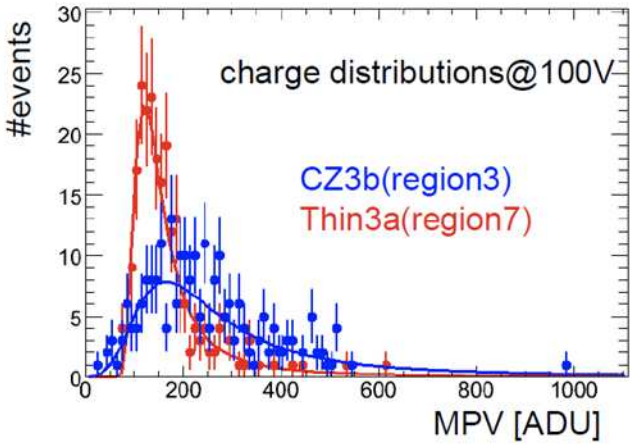

Figure 8: ADC distribution of INTPIX3b.

6. Summary

The SOI pixel detector is one of the novel technology to achieve the monolithic detector without bump bonding. The SOI pixel detectors are fabricated by the OKI Semiconductor Co. Ltd. $0.2\mu m$ CMOS fully depleted (FD-)SOI process, and developed by KEK and SOI collaboration. The current SOI pixel detector had been developped integration type and counting type detectors so far. Recent big progresses in SOI pixel detector were brough by introducing the BPW which helps to bias to the full depletion voltage. The FZ wafer of 7 $k\Omega\cdot cm$ resistivity is newly introduced in the sensor. We confirmed the sensor of 500 μm thickness was full depleted at about 80 V by

the measumrement of saturated output signals varing sensor bias. Furthermore, we had constructed SOI pixel telescope consists of 3 layer of INTPIX3e and achieved tracking for high energy positiron beam in 2010 with them. We, SOI collaboration, have been developing SOI pixel detectors, improving related processing technology and radiation tolerance for ideal radiation detector in future high energy experiments.

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