Basic research on SOI pixel detectors with internal gain based on avalanche multiplication

Bipin Subedi

Master's Program in Physics

Submitted to the Graduate School of

Pure and Applied Sciences

in Partial Fulfillment of the Requirements

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Abstract

Modern silicon detectors are required to have good recording efficiency of ionizing radiation, high response time, high spatial resolution, resistance to radiation, 2-dimensional readout, etc. but it is difficult to achieve them all using traditional detector technologies. Silicon-On-Insulator (SOI) technology has been shown to have those advantages including small pixel size, low power consumption, greater radiation tolerance, etc. Using SOI technology, monolithic pixel detectors can be fabricated by separating CMOS circuit and semiconductor detector layers with a Buried Oxide (BOX) layer in between.

New type of Avalanche Photodiode (APD) was designed at KEK, Japan using SOI technology. Currently, novel photodetectors with high response time and sensitivity with adequate gain are being sought and our SOIAPD is a potential candidate expected to achieve that quality. It is the first time in the world that SOIAPD was designed, fabricated and tested successfully. From this research, the SOIAPD has been shown to operate with gain of 10 times ~ 1000 times. Other characteristics of the SOIAPD like temperature dependence and radiation tolerance were also tested which showed versatility of its operation in various conditions. Although the current SOIAPD was tested for its electrical characteristics by direct contact from the sensor electrodes, the next step would be to integrate CMOS circuits like amplifier and shaper above the BOX layer to enhance the signals from sensor. Usable Double-SOI structures also could be implemented to enhance radiation tolerance. In the future, SOIAPD can be expected to be developed for use as detectors in high energy physics experiments as well as various industrial applications.

Contents

Chapter 1 Introduction of semiconductors

1.1 Electrical properties of solids and band theory

Electrical properties of materials can be explained properly with the help of band theory. According to the Pauli's exclusion principle, electrons in a single atom occupy discrete levels of energy, no two energy levels in an atom can have the same energy and each energy level can contain at most two electrons. When multiple atoms (N) come together to form a solid, the energy levels in individual atoms interact with the energy levels of the neighbouring atoms which causes shift in energy levels and since no more than two electrons can occupy the same energy level, N distinct energy levels with slightly different energy are created forming a broader band of energy levels or valence band as shown in fig1.

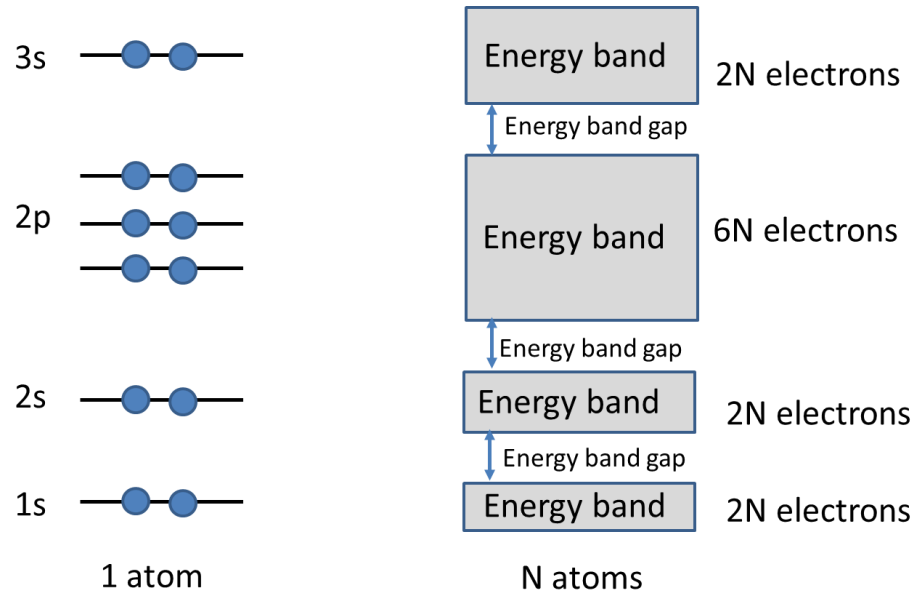


Figure 1 Energy levels and bandgap

Conductivity of a material is determined by whether free electrons are available in the conduction band or not. In insulators, there is a large energy gap (forbidden gap) between the valence band energy and conduction band energy level due to which the electrons can't move freely to the conduction band at room temperature. In case of conductors, the valence band overlaps with the conduction band and electrons can freely move to it causing the flow of electric current. However, for semiconductors, the forbidden energy gap between the two bands is sufficiently small to make it much easier for significant numbers of electrons to move across this gap and go from the valence band to the conduction band. This can happen if sufficient energy is supplied, for example if there is some thermal excitation. Thus, semiconductors exhibit increased conductivity with increasing temperatures. In many semiconductors, a temperature increase of 10 K will permit a doubling of the numbers of electrons in the conduction band.

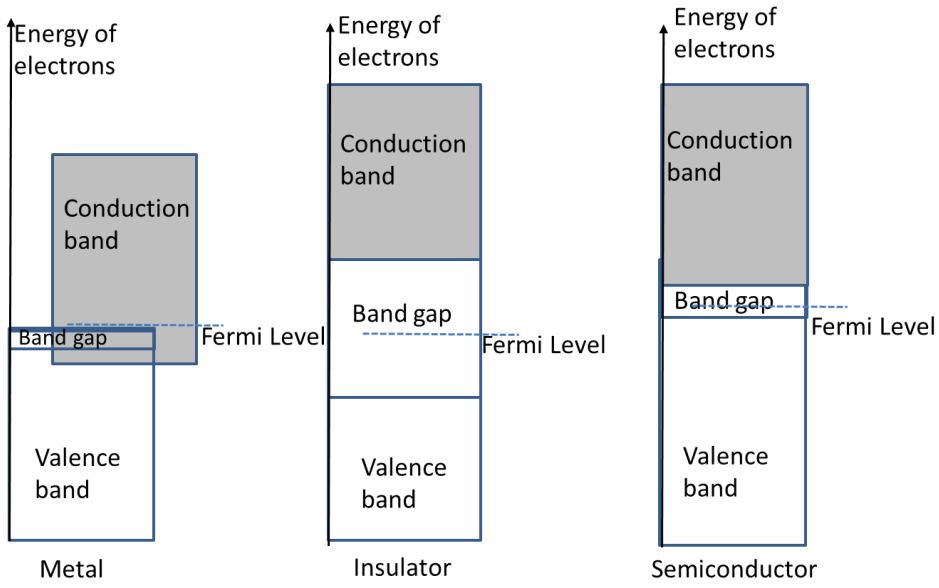


Figure 2 Conduction band, valence band and bandgap

Fermi function can be used to find the probability that an available energy level will be occupied by an electron at a given temperature. Fermi function (f(E)) is the probability that a level with energy E will be filled by an electron.

$$f(E) = \frac{1}{e^{(E-E_F)/kT} + 1}$$

In the equation above, k_B is Boltzmann's constant, $8.62\times10{-}5$ [eV/K], and T is the temperature in degrees Kelvin. E_F is called the Fermi energy or Fermi level. It is determined as the energy point where the probability of occupancy by an electron is exactly 50%, or 0.5. Using the Fermi function, it can be found that the higher the temperature, greater the chance that the electrons can bridge the band gap to participate in electrical conduction as shown in fig 3. The Fermi function gives a finite value in the bandgap but there the electron population density in the region is still 0 as electron population density is given by the product of Fermi function and the electron density of states. At 0K, the fermi Function is 0 (for $E > E_f$) and there are no electrons in the conduction band although energy levels are available. At higher temperatures, both the density of states and the Fermi function have finite values in the conduction band so electric conduction becomes possible.

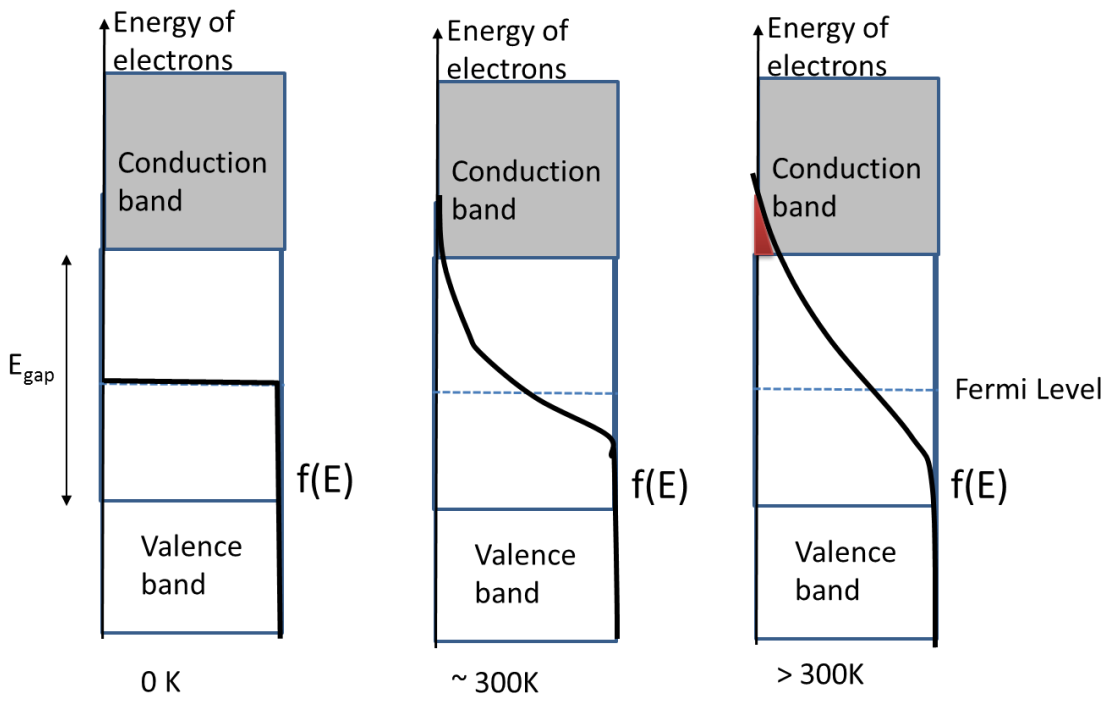


Figure 3 Mechanism of electrical conduction in semiconductors

1.2 Types of semiconductors

1.2.1 Intrinsic semiconductors

At low temperatures, pure or undoped semiconductors (intrinsic semiconductors) have very low electric conductivity. Each Si atom has four electrons in its valence shell and need four more electrons to achieve more stable state, so each Si atom makes covalent bonds with four surrounding Si atoms sharing 1 electron from each. As all the valence electrons are involved in forming covalent bonds, no free electrons are available, hence low conductivity of intrinsic semiconductors. But, since the energy band gap (1.09eV of Si) between valence band and conduction band in Si is smaller compared to insulators, relatively smaller excitation energy (in the form of heat etc.) is sufficient for pushing significant number of electrons to valence band for current flow.

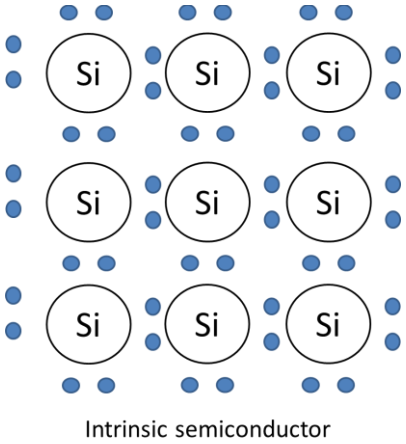


Figure 4 Intrinsic semiconductor

1.2.2 Extrinsic semiconductors

As explained in the above paragraph, intrinsic semiconductors have low conductivity and have no use as they are, but the trick to make them useful is by changing their electric properties by adding impurities. Adding impurities (dopants) in to intrinsic semiconductors is known as doping and it makes the semiconductor extrinsic. Two type of semiconductors can be manufactures by doping different types of dopants, n-type and p-type.

1.2.2.1 p-type semiconductor

Group-III elements in the periodic table such as Boron (B), Aluminium(Al) have 3 electrons in their valence shells. The 3 electrons make covalent bonds with 3 surrounding Si atoms but the dopant atom still wants one more electron (hence called acceptor), which causes a 'vacancy' of an electron, also called a hole. Such hole can attract electron from nearby Si atom, stabilizing itself but leaving hole in the Si atom and so on, thereby propagating the hole. Such hole can be considered as a positive charge that can travel through the valence band of the material. Such type of semiconductors (called p-type semiconductors) contain more holes in the valence band than electrons in the conduction band, so holes are the majority carriers and electrons are the minority carriers.

1.2.2.2 n-type semiconductor

However, if atoms of Group-V elements like Phosphorus(P) or Arsenic(As) to the intrinsic semiconductor, n-type semiconductor is formed. Such dopant elements contain 5 electrons in their valence shell and therefore have an excess electron when they make covalent bonds with 4 surrounding Si atoms. These kinds of dopants are called donors as they provide free electrons to the semiconductor. The extra free electrons can easily

jump to the conduction band and enable conduction of electric current since such electrons have energy level close to the energy level of the conduction band.

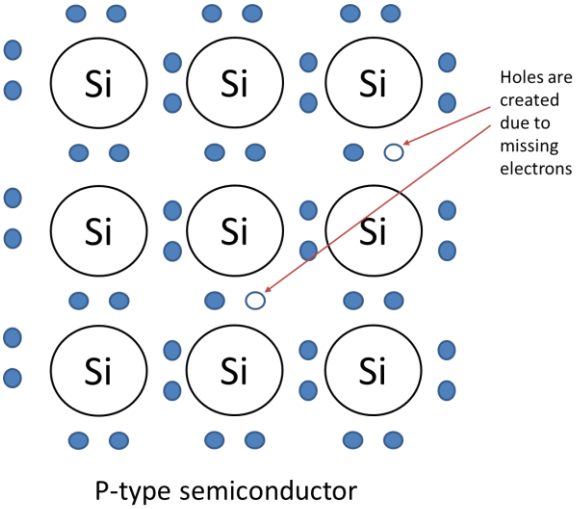


Figure 5 p-type semiconductor

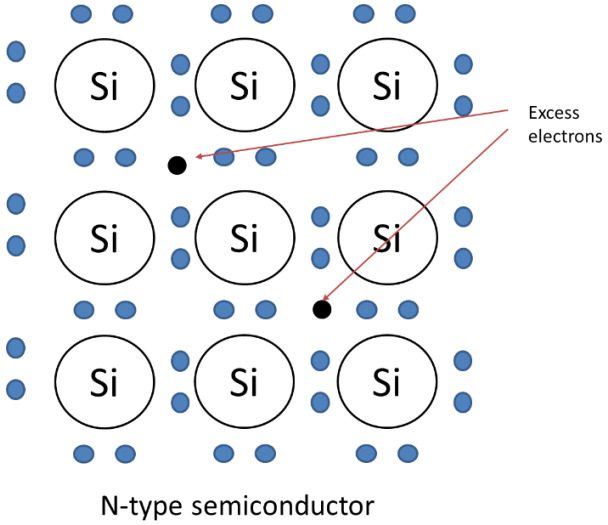


Figure 6 n-type semiconductor

1.3 p-n junctions

A p-n junction is the connection interface between two oppositely doped (n-type and p-type) ends of a semiconductor crystal and such semiconductor is called a p-n junction diode. When n-type and p-type regions come into contact, the electrons from n-doped side diffuse to the p-doped side and combine with the holes from the p-doped side creating a space charge region or depletion region around the p-n junction. An electric field is created in the space charge region in n-doped to p-doped direction. Electrons and holes in the junction move back and forth from p-doped to n-doped side and vice

versa (diffusion current) and an equilibrium is reached.

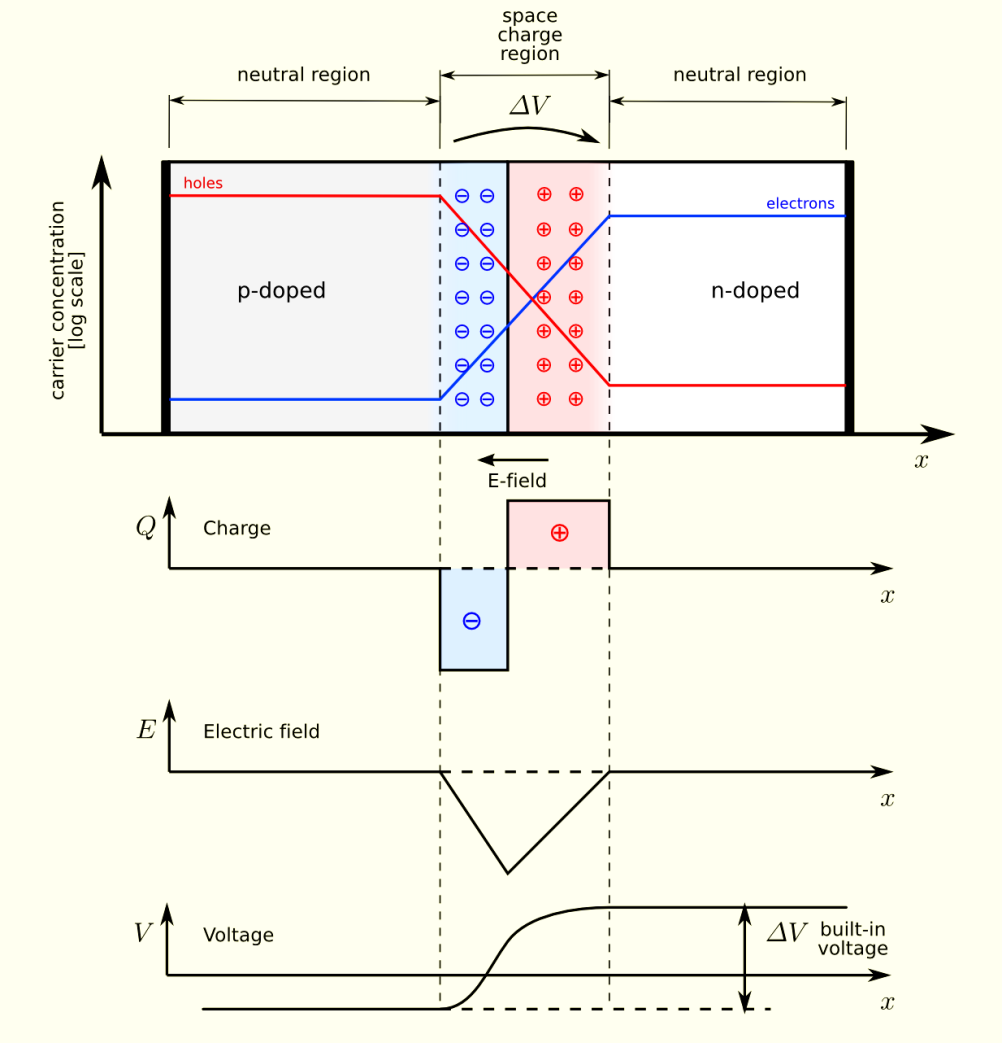


Figure 7 Operation of a p-n diode [17]

1.3.1 Forward and reverse bias of a p-n diode

If the n-type side of a p-n diode is connected to the negative terminal of a power supply and the p-type side is connected to the positive terminal of the power supply, the diode is said to be forward biased. In such condition, if the external voltage applied is greater than the potential difference across the depletion region (0.7V for Si), the electrons from n-type side are pushed across the depletion region and electric conduction occurs.

On the other hand, if the power supply is reversed from forward bias, any additional voltage applied goes into expanding the conduction barrier or depletion region further and further. Only a tiny current can flow in this bias condition (called leakage current) because of small number of holes and electrons present in the depletion region of the

semiconductor material. Since, leakage current is mostly undesirable, Si is preferred to some other semiconductors like Ge to operate in room temperature since Si has significantly smaller leakage current compared to Ge (due to larger energy gap between the valence and conduction bands in Si).

1.3.2 Junction breakdown

If the reverse bias voltage is further increased, at a specific voltage (reverse bias breakdown voltage), the electrons and holes break through the p-n junction resulting in a large flow of current. There are two different phenomena that cause such non-destructive p-n junction breakdown.

1.3.2.1 Avalanche breakdown

Avalanche breakdown occurs if p-n junction diodes are moderately doped and have wider depletion region. When a reverse bias is applied in such diode, the electric field across the p-n junction increases and after a certain voltage (avalanche breakdown voltage), the electrons start getting free off their covalent bonds and drift across the junction. The drifting electrons carry kinetic energy which collide and knock off electrons from other atoms generating more free electrons resulting in a rapid increase of electric current (avalanche mechanism). In avalanche breakdown, since the disturbance by atoms is smaller at lower temperatures, the avalanche multiplication becomes large by decreasing the temperature.

1.3.2.2 Zener breakdown

If a p-n junction diode is heavily doped, the electrons can tunnel through the thin junction. When the reverse bias voltage is increased across the diode, the electric field at the junction increases but still not enough so that the avalanche multiplication does not take place. The recombination of electrons and holes in the region cause a net drift current which increases rapidly with increase in reverse bias voltage.

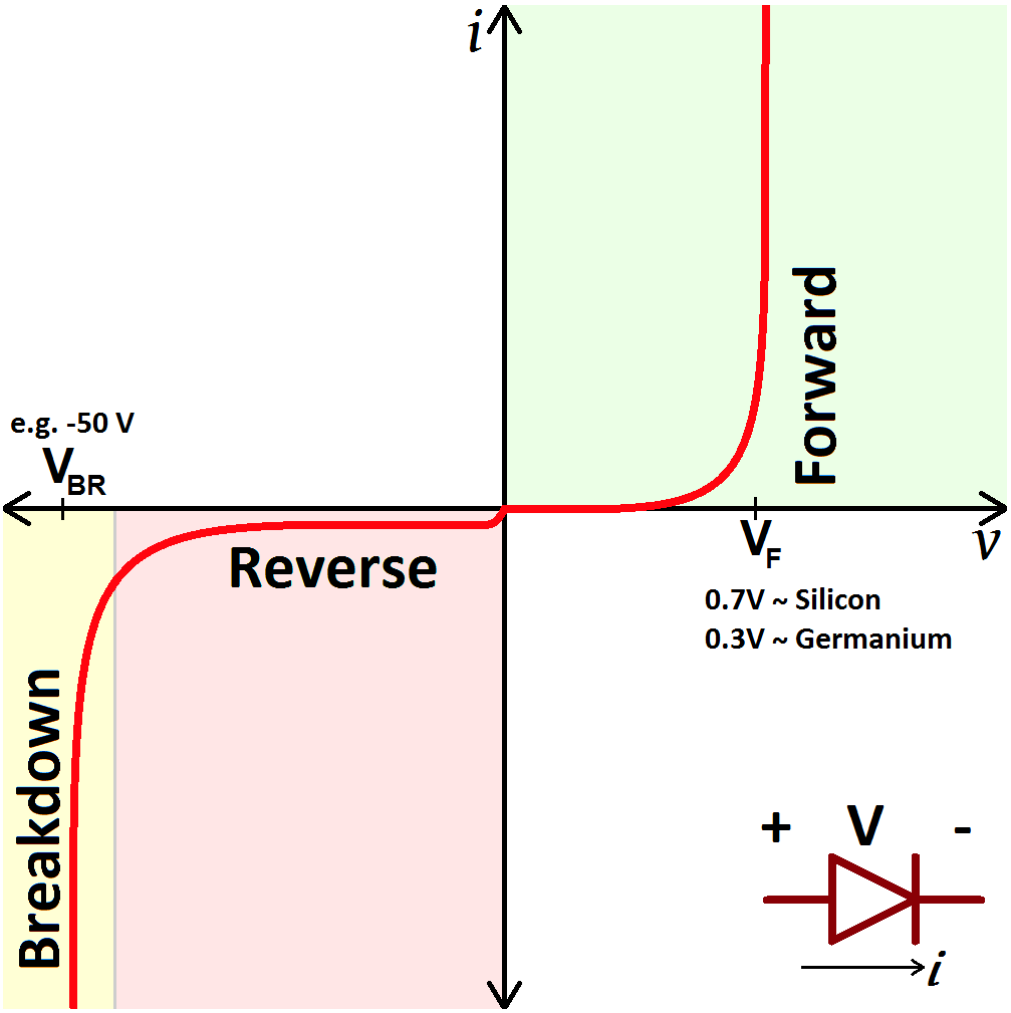
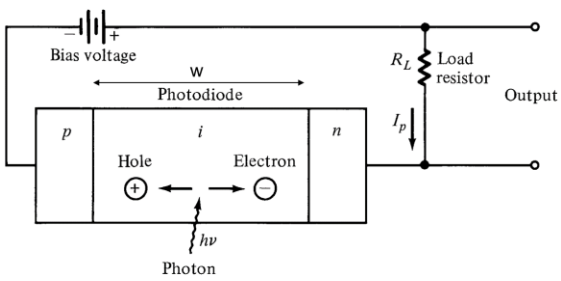


Figure 8 IV characteristics of a p-n junction diode

1.4 Photodiode

A photodiode is a p-n junction diode operated in reverse bias in which the electric current flowing through can be varied by using optical signals. As photons pass through the photodiode, the depletion region helps separate the photogenerated electron-hole pairs causing the flow of electric current. In a photodiode, higher quantum efficiency and higher response speed are desired. Quantum efficiency is the fraction of incident photons contributing to the photocurrent. Higher quantum efficiency requires the depletion region to be sufficiently wide for larger number of photons to be absorbed (along with other factors like wavelength, absorption coefficient, doping, geometry,etc) but response time is better with smaller depletion region width, so balance of the two parameters is important to achieve desired photodiode performance.

The basic structure and working of a pin photodetector is shown in fig 11.



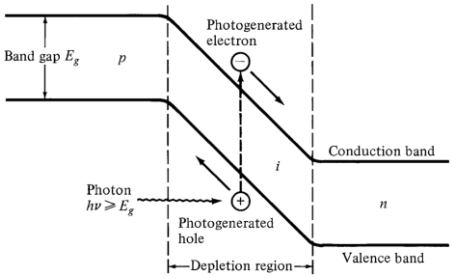


Figure 9 Basic structure of a pin photodiode **Figure 10 Basic working principle of a pin photodiode**

There are 3 regions in this type of photodiode, short heavily doped n and p regions are in either sides of a wider (wider than the space charge region) intrinsic region. In this case the photodiode is operated in the reverse bias voltage not enough to create electric field enough to start avalanche mechanism.

Few terms used in understanding photodiodes:

Quantum efficiency: Quantum efficiency is denoted by symbol R and is defined as the fraction of incident photons having energy enough to free electrons in the PD. Quantum efficiency depends both on wavelength of incident light as well as composing semiconductor material.

Responsivity: It is the measure of output current relative to the number of incident photons. Responsivity is defined as average output current divided by average incident optical power and its units are A/W.

Gain: Gain is the multiplication factor of the primary photon current. It is the ratio of output current at an operating voltage to the current at a low voltage where the gain is unity, i.e. no multiplication occurs.

Dark Current: Due to the leakage current in reverse biased photodiode, some small current flows even when there are no incident photons which is called dark current. Dark current in orders of less than 10^-10 A is usually considered to have insignificant effect in photodiode performance [20].

1.4.1 Avalanche photodiode (APD)

Avalanche photodiode (APD) is a photodetector that provide higher sensitivity due to the internal gain through avalanche multiplication of photogenerated electrons as shown in fig10. APD is operated in reverse-bias voltage sufficient to create electric field required for avalanche multiplication (impact ionization) to take place. Generally, higher the reverse voltage, higher the gain and normal APDs can show current gain in order of 10^2 but by varying doping concentration and other parameters APDs can be made to work in voltages over 1500V achieving gains in orders of 10^3. As the photocurrent in an APD is amplified by the gain factor due to avalanche effect, resulting current is much higher than in pin photodiode.

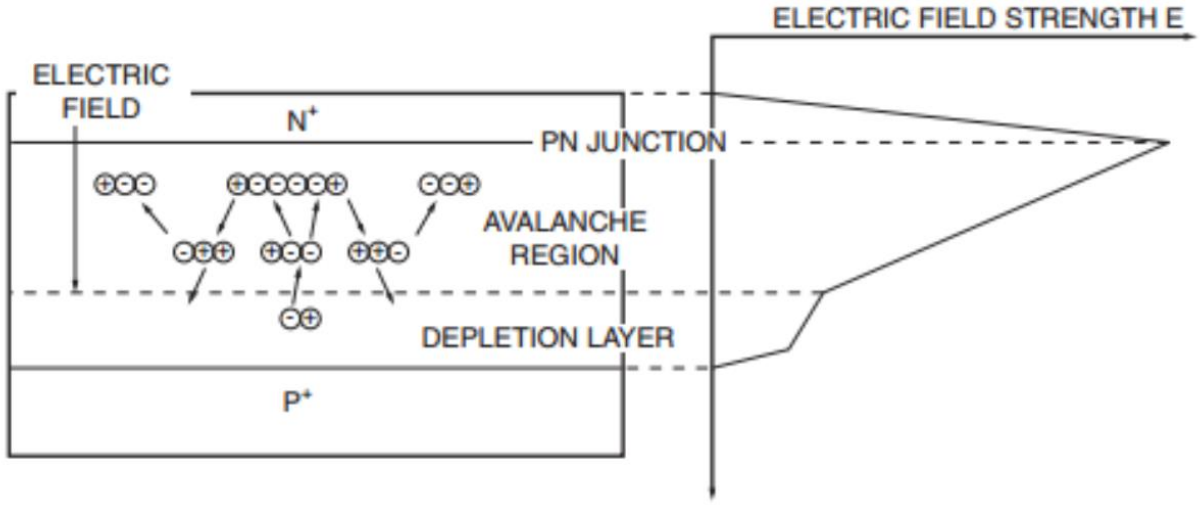


Figure 11 Avalanche mechanism in APD [10]

APDs can be operated in different voltage ranges as shown in fig 11

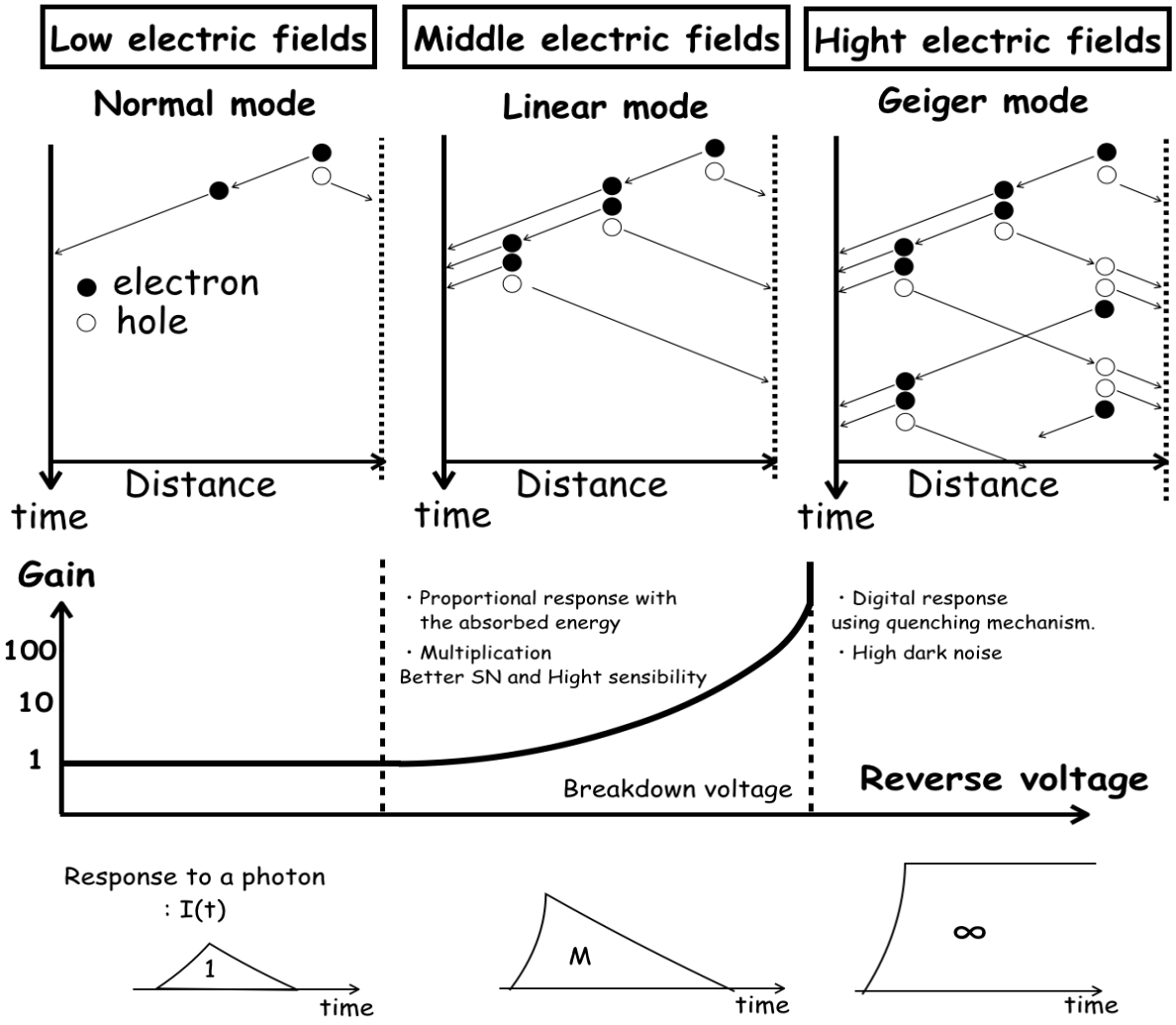


Figure 12 Various modes of operation of an APD [12]

At low voltages (Normal mode in the fig 12), when electric field is not strong enough to start avalanche mechanism, APDs are inoperable.

Once the electric field is strong enough to start avalanche mechanism, electron-hole pairs are generated and actively collected at the opposite terminals. At voltages below and near the breakdown voltage, collection dominates, causing the avalanche current to decay and ultimately stop. Since the gain is linearly dependent on applied reverse bias voltage in this mode, the gain is finite and largely predictable. This characteristic enables us to statistically calculate the number of photons absorbed by the photodetector. This voltage region is known as linear mode range and the APDs designed for test purpose in this thesis are operated in this range. Once the breakdown voltage is crossed, increase in electric current is very high in relation to the applied reverse bias voltage (Geiger mode range). In this mode, electron-hole pair generation exceeds collection speed which causes accumulation of electrons and holes at the n- and p-sides of the depletion region, respectively, creating an internal electric field in opposition to the applied bias limiting the growth of current. As long as the applied bias voltage is maintained, the photodetector remains in that state. Here, the gain is virtually infinite and an electrical event resulting

from a single photon or multiple photons arriving simultaneously is indistinguishable. Our APDs are inoperable in such voltages.

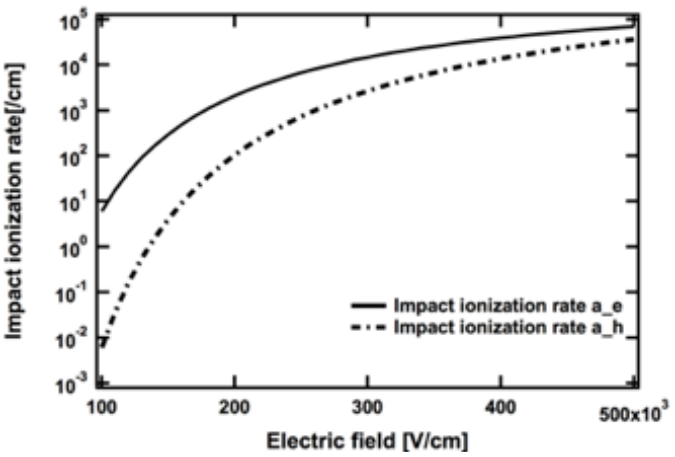


Figure 13 Impact ionization rate of electrons and holes [12]

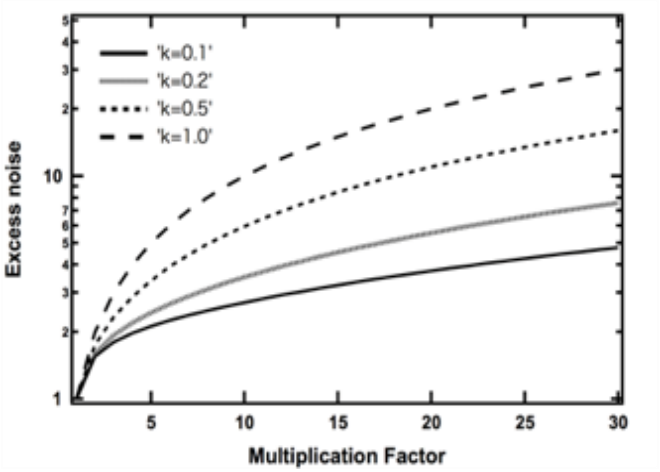


Figure 14 Excess noise in APD depending on gain [12]

The graph above in the left, fig 13, shows the difference in impact ionization rate of electrons(α_e) and holes(α_h). At low electric field strength (at smaller reverse bias voltages) impact ionization rate of electrons is significantly greater than that of holes and the difference closes as electric field strength is increased. In fig 14, Excess noise, F is plotted against the gain/Multiplication factor. The parameter k is the ratio of impact ionization rate of holes to electrons. Excess noise is plotted for k>0.1 i.e. in electric field strength greater than approximately 200V/cm. As can be seen in the graph, noise increases with increase in multiplication factor and that noise is smaller of smaller value of k, i.e. at smaller reverse bias voltage. The curves are parametrized by the following equations.

$$a_e(E) = \exp(A_e + \frac{B_e}{E})$$

$$a_h(E) = \exp(A_h + \frac{B_h}{E})$$

$$\mathbf{k} = \frac{\boldsymbol{\alpha_e}}{\boldsymbol{\alpha_h}}$$

$$F = M(1 - (1 - k)\frac{(M - 1)^2}{M^2})$$

1.5 Semiconductor Detectors

Semiconductor detectors are most commonly in modern high energy physics experiments. In semiconductor detectors, the fundamental information carriers are electron-hole pairs, which are produced along the path taken by the charged particle (primary or secondary) through the detector. By the movement of electrons and holes, the detection signal is induced on the readout electrode. Of the available semiconductor materials, silicon is mainly used for charged particle detectors and soft X-ray detectors while germanium is widely used for gamma-ray spectroscopy. As shown in figure 15, the electron hole pairs created in the Si-bulk due to incident radiation, drift towards the opposite poles producing a signal of detection. The energy needed to produce an electron-hole pairs is independent of energy of radiation, type of radiation and temperature. The average needed is same as ionization energy which is about 3.62eV for Si and 2.96eV for Ge.

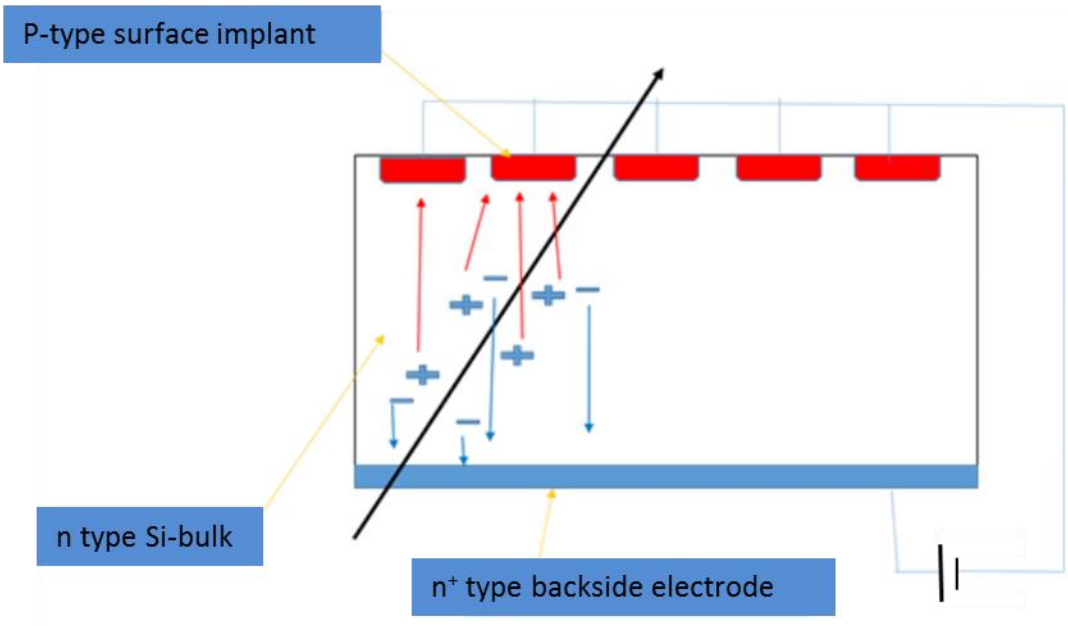


Figure 15 Working of a basic silicon detector

1.5.1 Large Hadron Collider (LHC)

The Large Hadron Collider (LHC) is the world's largest and most powerful particle collider in the world. Its aim is to test the predictions of different theories of particle physics like the Standard Model, and particularly prove or disprove the existence of the theorized Higgs boson (which was detected in 2013) and of the large family of new particles predicted by supersymmetric theories. It contains four major detectors ALICE, ATLAS, CMS, LHCb and smaller detectors each designed for certain kinds of research.

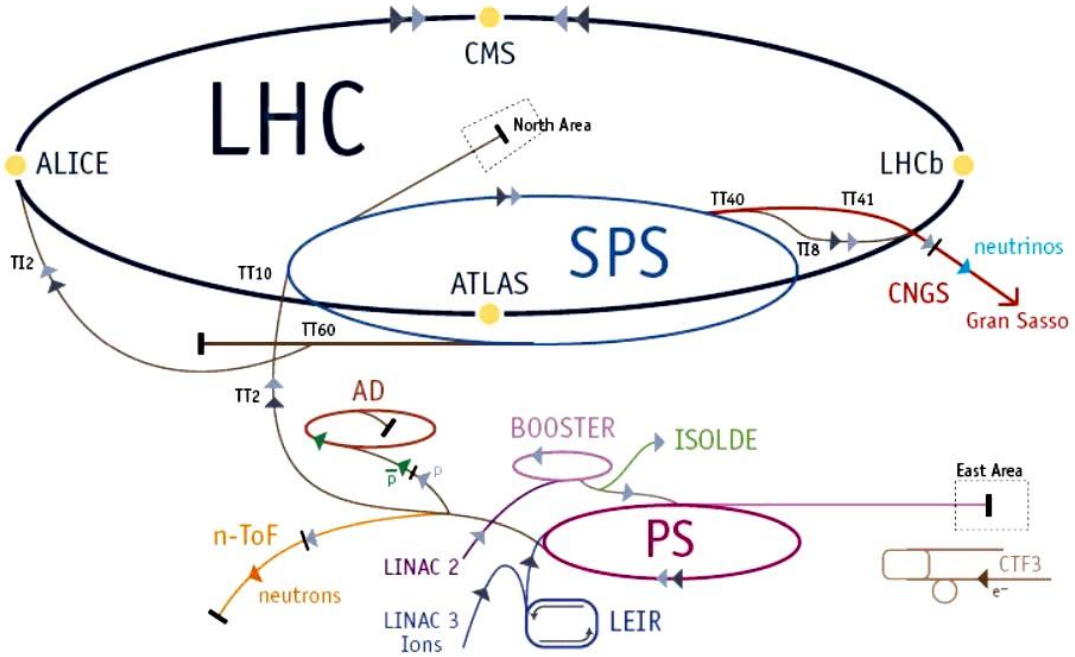


Figure 16 Components of Large Hadron Collider [19]

ATLAS is one of the two versatile detectors designed to study Higgs phenomenon, making use of semiconductor detectors to make measurements of collision of proton beams at high energies.

Silicon-Conductor Tracker (SCT) is a silicon micro strip detector at the heart of the ATLAS experiment at the CERN Large Hadron Collider. Together with the rest of the ATLAS Inner Detector it provides vital precision tracking information of charged particles. This detector is constructed from silicon wafers 6cm in diameter. Particles are detected by strips 0.080mm apart running along the beam pipe (z-axis). Alternate layers have strips running at 40mrad with respect to z axis, allowing to reconstruct the hit positions three dimensionally. The path of the particle is measured with a point precision of ~0.02mm perpendicular to the strips.

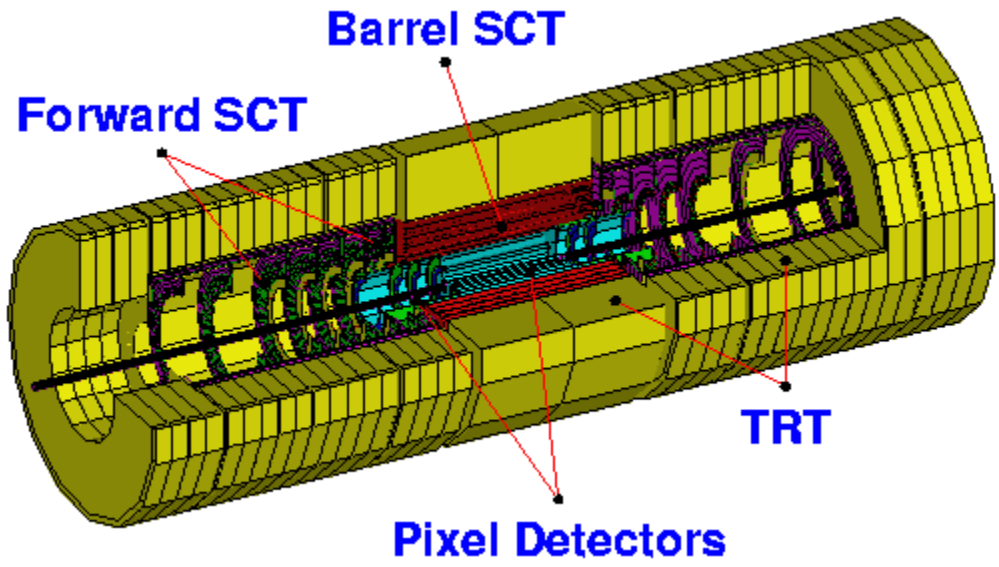


Figure 17 ATLAS inner detector showing SCT, Pixel detector and TRT [18]

In order to perform higher precision particle detection, ATLAS has pixel detectors places in the inner side of SCT. This detector has high space-point resolution (≈12μm in r φ, ≈90μm in z) and greater radiation hardness (50MRad or $10^{15}/cm^2$ neutron-equivalent). The sensor part of it has an active area of 2×6 cm2 and 250μm thickness. It has 41984 normal pixels (50μm ×400μm) and 5284 long pixels (50μm ×600μm).

1.5.2 ILC (International Linear Collider)

The International Linear Collider (ILC) is a proposed linear particle accelerator. It is planned to have a collision energy of 500 GeV initially, with the possibility for a later upgrade to 1000 GeV. Two detectors ILD (International Large Detector) and SiD (Silicon Detector) are being developed for the project. The radiation dose at the vertex detector inside ILD is supposed to be about 1kGy/year.

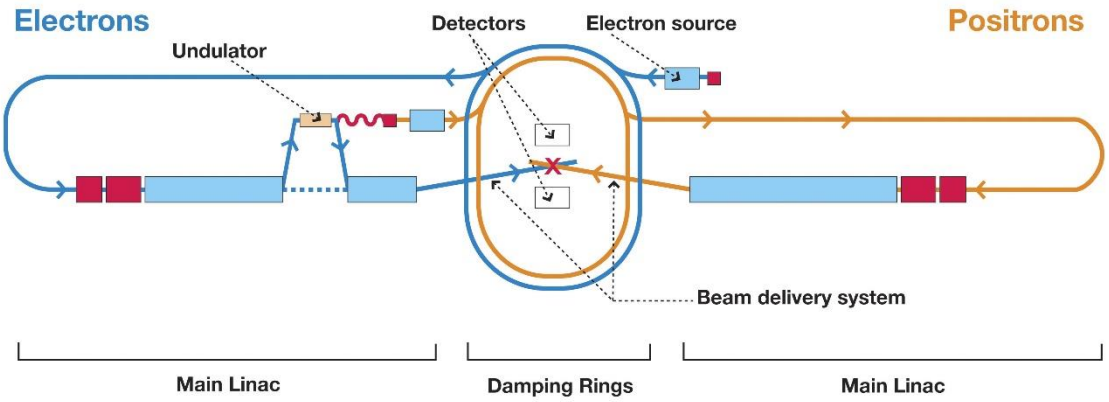


Figure 18 Schematic layout of the International Linear Collider (ILC) [21]

Chapter 2 SOI Pixel Detectors

2.1 Introduction to SOI pixel detectors

SOI(Silicon-On-Insulator) is a semiconductor manufacturing technology in which transistors are formed in thin layers of silicon that are isolated from the main body of the wafer by a layer of electrical insulator, usually silicon dioxide. By bonding two silicon layers in which the lower Si layer of high resistivity acts as detector of charged particles and upper SOI layer is for readout circuit, integrated SOI pixel detector with readout circuit is realised which is shown in figure 19. The sensor layer can vary in thickness from 50~500μm and the Buried Oxide (BOX) layer which lies between the upper electronic layer and sensor layer is about 200nm thick. Pixels are formed by appropriately implanting heavily doped ions below the BOX layer. As a reverse bias voltage is applied to create a depletion zone, the electron-hole pairs liberated by the charged particles passing through the depletion zone in the sensor are collected in the sensor electrodes which are then passed through the metal vias to the circuit which is treated as detected signals at that point and can be passed on to the electronic circuitry for amplification and processing.

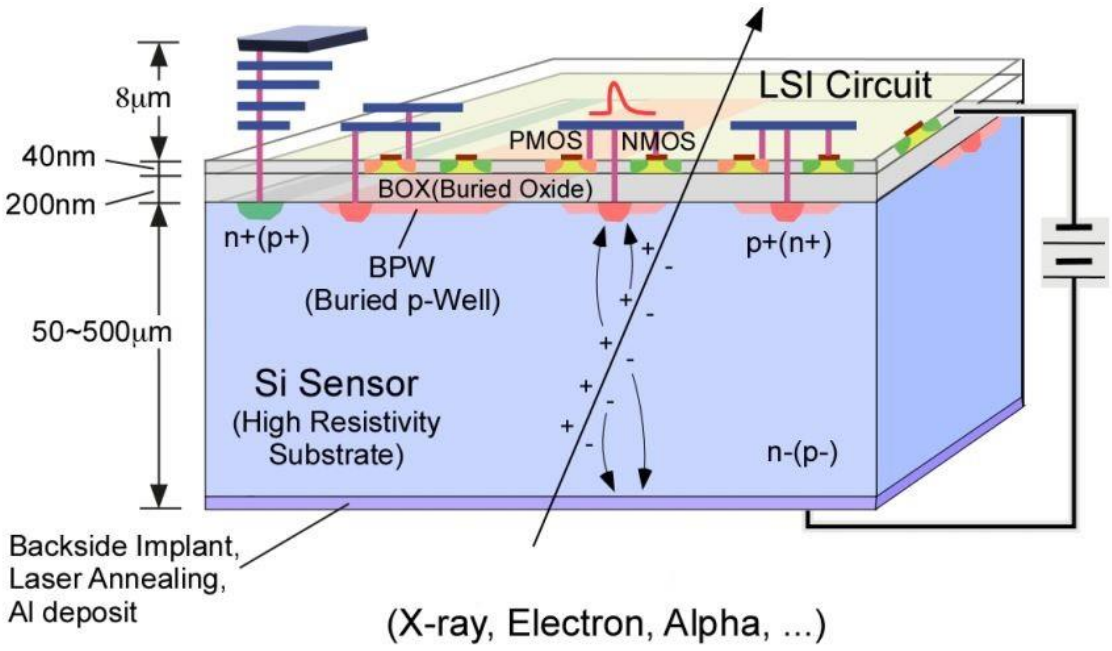


Figure 19 General SOI structure

2.2 SOI Manufacturing process

Development of SOI monolithic pixel detectors was started as a project at KEK Detector Technology Project (KEK DTP) since 2005. Currently, Silicon On Insulator PIXel detectors (SOIPIX) projects are being carried out since 2005, led by KEK and supported by Japan Society for Promotion of Science (JSPS). [12]

Table 1 SOI process details [22]

Process (Lapis Semiconductor Co. Ltd.)	0.2mm Low-Leakage Fully-Depleted (FD) SOI CMOS 1 Poly, 5 Metal layers (MIM Capacitor and DMOS option) → Total thickness above top Si (SOI layer) ~ 9 mm Core (I/O) voltage : 1.8 (3.3) V
SOI wafer (200 mm ϕ =8 inch)	Diameter: 200 mmϕ, 720 μm thick Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick
Sensors	CZn ~ 700 Ω-cm, thickness~300μm (Default) FZn~ > 3 k Ω-cm, thickness~500μm (2009-) FZp ~ 25 kΩ-cm, thickness~500μm (2010-) Double SOI (CZn) (2012-) and (CZp) (2015-)
Backside process	Mechanical Grind →Chemical Etching →Back side Implant →Laser Annealing → Al plating

Silicon-on-insulator (SOI) technology is based on 0.2μm low-leakage fully-depleted SOI CMOS technology. High-resistivity substrate as sensing part and a thin low-resistivity Si layer for CMOS circuits are integrated into a single unit in a SOI wafer. KEK organizes MPW (Multi Project Wafer) runs twice a year in which the mask is shared among SOI projects in different Universities and institutions to reduce the cost of design and production. [13]

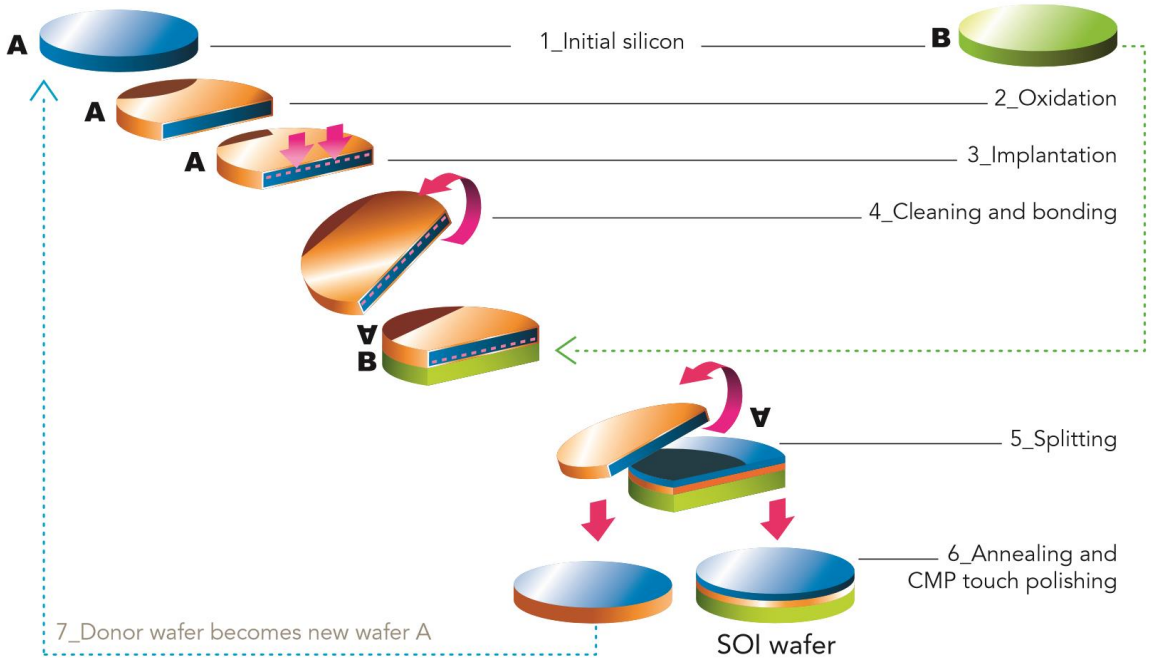


Figure 20 SOITEC SOI process [14]

2.3 SOI-CMOS

In traditional Bulk-CMOS, transistors are separated by making p-n junction inside the wafer structure. On the other hand, in SOI-CMOS each transistor is separated completely by the buried oxide (BOX) layer as shown in figure 22. The separation by insulating layer prevents electrical contact between the transistors which gives the following advantages over the bulk type.

a) Very low leakage current due to the insulating BOX layer, which contributes to the lower power consumption, ability to operate in low voltages.
b) Transistors are better isolated having small capacitive couplings to neighbours, which contributes to better speed at lower noise.
c) Better latch-up tolerance due to absence of parasitic device inside transistor.

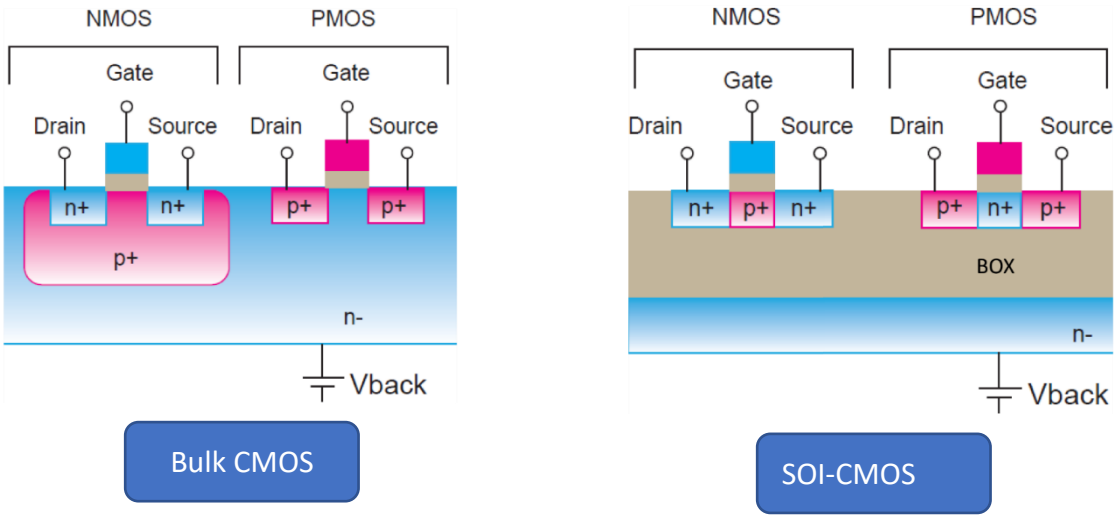


Figure 21 Bulk CMOS vs SOI-CMOS

2.3.1 Monolithic-type SOI detector

In traditional hybrid silicon pixel detectors, the sensor part and the readout circuit part are connected by metallic bump bonding. But in SOI monolithic detectors the two parts are constructed together into one integrated detector connecting using metal vias.

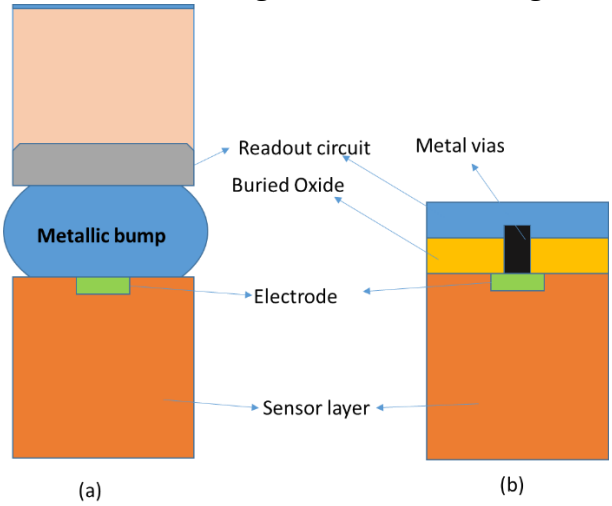


Figure 22 (a) Hybrid type silicon detector (b) Monolithic type SOI detector

The monolithic type SOI detector has following advantages over the traditional hybrid type silicon detector.

a) Since no mechanical bonding is required due to it being monolithic, it helps minimize multiple scattering, smaller pixel size is achievable and amount of materials and cost can be reduced. [11]

b) Due to the decrease of parasitic capacitance, high speed and low power consumption, high S / N ratio of reading can be achieved.
c) Leakage path from CMOS circuitry to signal detection part is absent, which allows greater temperature range of operation. [15]

d) Problems of latch-up effect and Single Event Effect (SEE) are eradicated due to the isolation of CMOS circuitry from the sensor layer by SiO_2 layer (BOX layer).
e) 3-D integration possibility using μ -bump technology is another advantage of SOI technology being monolithic type and high miniaturization. [16]

2.4 Problems with SOI detectors

Due to the many advantages of SOI detectors over traditional silicon detectors, it is being considered as the pixel detector of future. But, there have been a few problems that needed to be addressed with the original SOI detectors.

2.4.1 Back-gate effect

Since the readout circuit part and the sensor part are integrated together in SOI pixel detectors, the reverse bias (back-bias voltage) applied in the sensor affects the transistor operation parameters including its threshold voltage. This effect is called back-gate effect.

In order to remove this effect, BPW (Buried P-Well) structure was introduced in SOI process. The BPW which controls the electric potential is formed by adding p-type impurities to the n-bulk sensor part immediately below the BOX layer. The BPW is often connected to the pixel nodes, which usually enhances the charge collection. This, however increases the detector capacitances and reduces the signal height. The design of the BPW is thus carefully carried out.

2.4.2 Crosstalk

Because of miniaturization of the detectors, the sensor part and readout circuit part are separated only by thin layer of buried oxide (BOX) (~200nm) and they can interfere electrically. This phenomenon is known as crosstalk. Crosstalk can originate between the adjacent pixels as well. This effect leads to errors in precision position measurements because of which circuits free of crosstalk need to be designed.

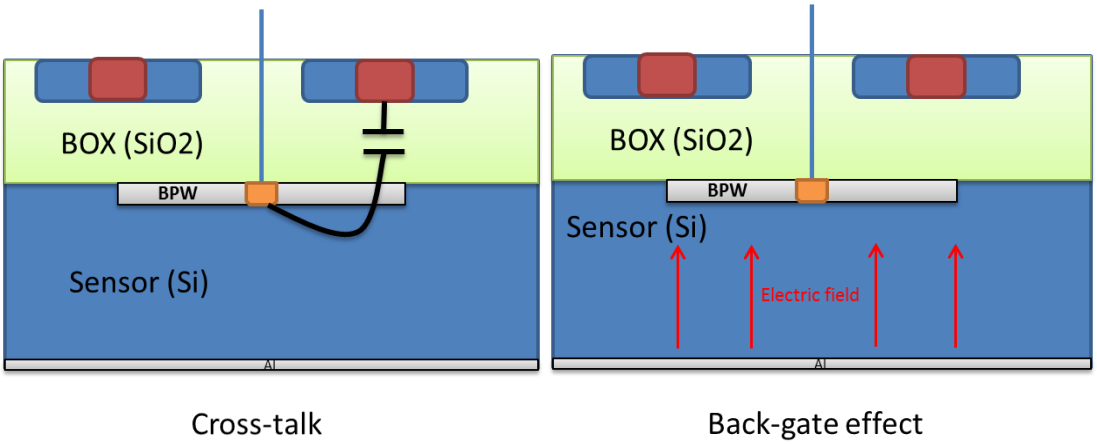


Figure 23 Crosstalk mechanism

Figure 24 Backgate effect

2.4.3 Radiation tolerance

Detectors in high energy experiments are exposed to very high doses of radiation because of which they made to be tolerant to those conditions. The Pixel detector which lies at the centre of ATLAS detector in LHC is exposed to 158kGy/yr of radiation at distance of 4.3 cm from the beam. This value is expected to go up 10 times for the planned HL-LHC (High Luminosity LHC). Similarly, in ILC (international Linear Collider), silicon detectors will be exposed to 1.5kGy of radiation in 3 years. Therefore, SOI detectors need to meet the required radiation tolerance if they are to be used in high-energy experiments.

Effects of ionising radiation on SOI detectors can be classified in the following two types.

2.4.3.1 SEE (Single Event Effect)

When radiation like heavy charged particles pass through the SOI detectors, many electron-hole pairs are produced because of which breakdown and latch-up phenomenon may be observed. This effect is called SEE effect. In case of SOI-CMOS, since the sensor part is separated by the buried oxide layer, and since the thickness of active silicon layer is also about 40nm, chance of breakdown occurrence is less. Similarly, as transistors are also separated completely, occurrence of latch-up is also prevented. Hence, SOI pixel detectors are highly tolerant to single event effect.

2.4.3.2 TID (Total Ionizing Dose) effect

When the detector is irradiated, electron-hole pairs are produced not only in the Si layer but also in the BOX (buried oxide) and gate oxide layer. The drift velocity of holes is much slow than that of electrons in these layers because of which holes get trapped and a positive charge is developed and affects the transistor parameters. This effect is called TID effect. Different to that in Bulk CMOS, transistors lie close to the

buried oxide later in SOI CMOS due to which its effect in SOI pixel detectors is to be carefully studied.

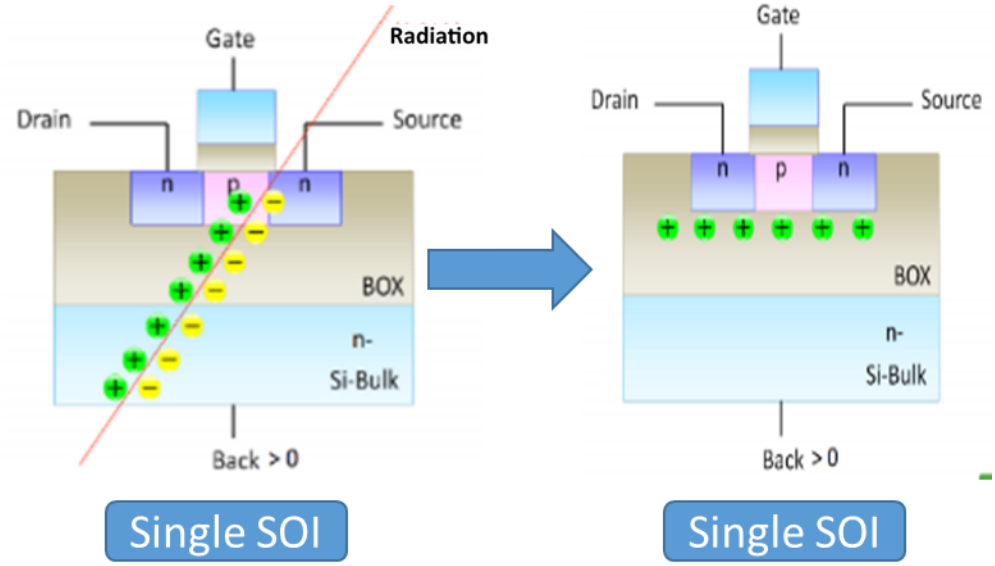


Figure 25 TID effect in SOI-CMOS

2.5 Double SOI

Double-SOI pixel detector technology was introduced to solve the problems found with normal single SOI pixel detectors. Double-SOI structure consists of two layers of buried oxide with thin middle Si layer in between (shown in fig 26) of which electric potential can be varied as required to recover transistor properties. Introduction of middle Si layer also has other advantages like acting as an insulating layer between sensor and circuit layer, which helps in reduction of cross-talk, back-gate effect, etc.

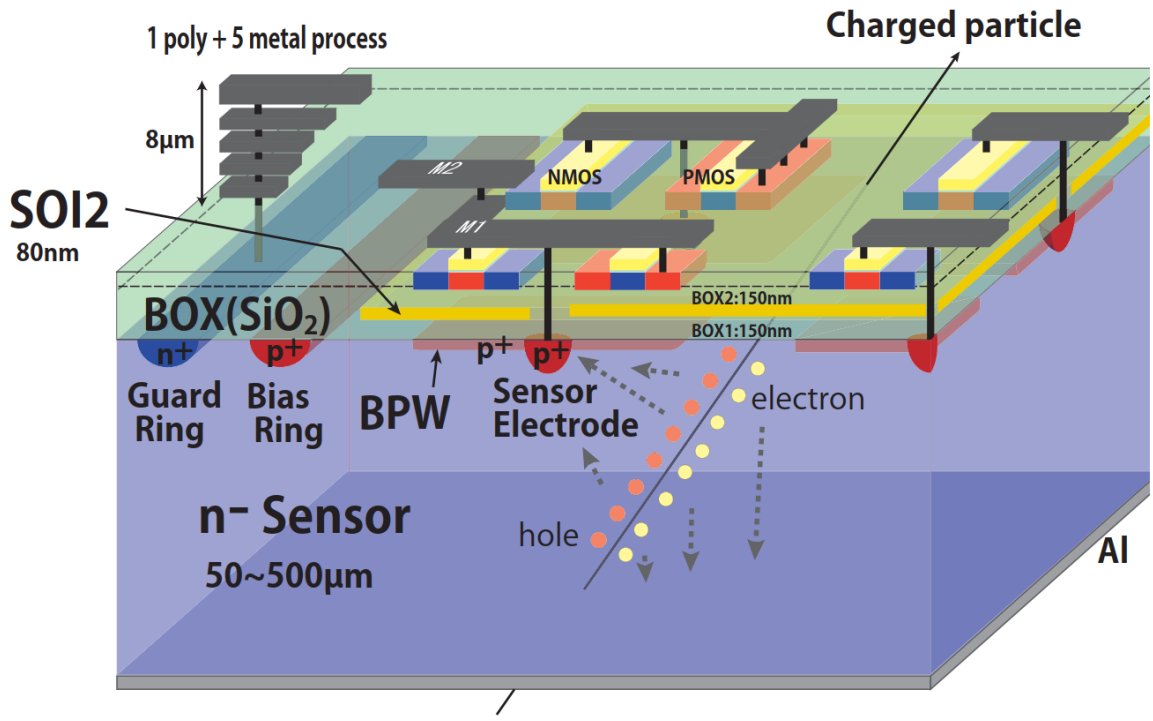


Figure 26 Structure of double-SOI pixel detector

Double SOI process involves performing the normal single SOI manufacturing process twice as shown in fig 27.

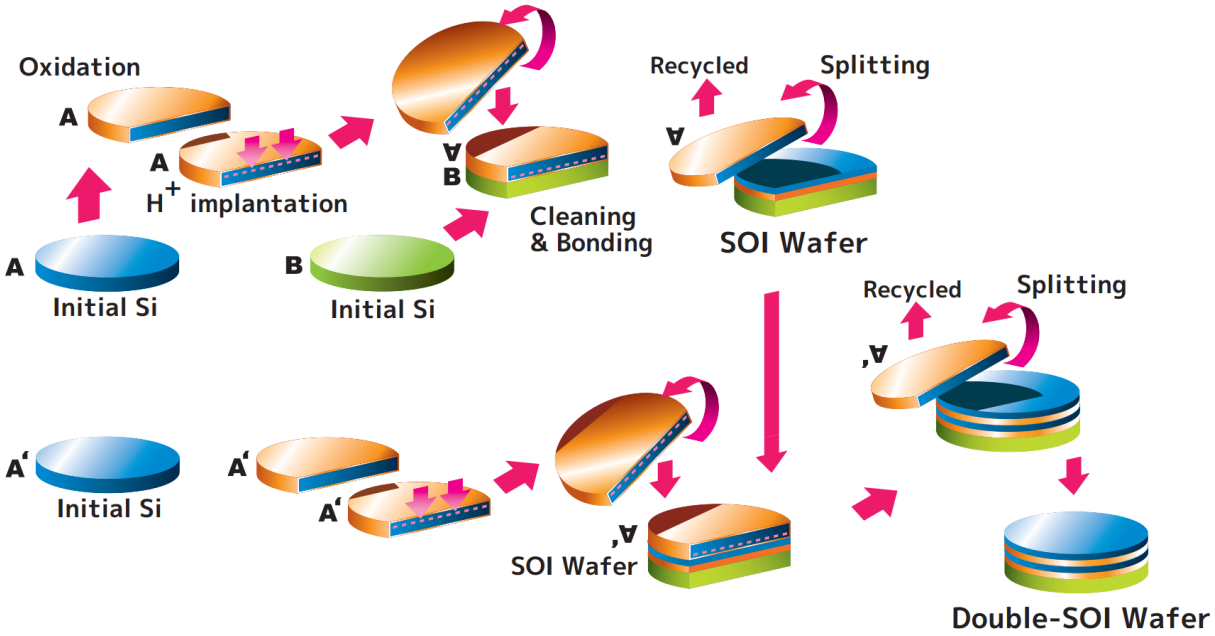


Figure 27 Double-SOI process (SOITEC)

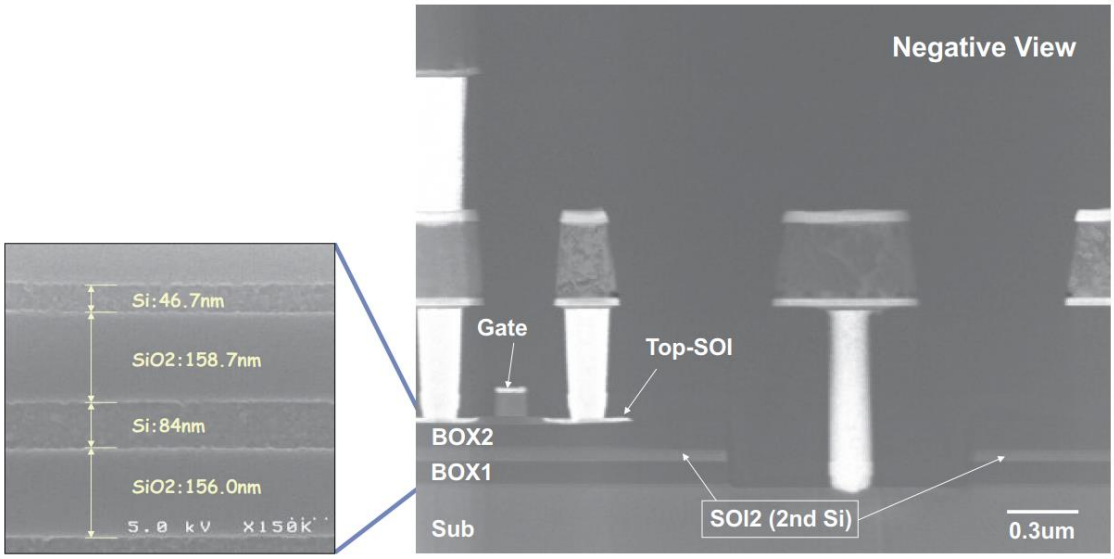


Figure 28 Cross-section view of Double SOI structure using SEM (Courtesy of Lapis Semiconductor)

Fig 28 shows the cross-sectional image of first successfully manufactured Double-SOI structure taken using SEM (Scanning Electron Microscope). The wafers use for evaluation in this thesis were manufactured by SOITEC.

Chapter 3 SOI-APD

SOI APDs are designed to take advantage of both the internal gain available from avalanche mechanism and the benefits from using SOI process technology mentioned in the previous chapter. By integrating SOIPixel sensor part with avalanche photodiode structure, SOIAPD with internal gain and high sensitivity can be achieved which is not possible with bulk CMOS technology [23].

Advantages of SOIAPD over normal APD and PPD (Pixelated Photon Detector) can be summarized is the table below.

	APD	PPD	SOIAPD
Avalanche Gain	10~100	105~106	10~100
Conversion circuit gain	-	-	5-10
Random Noise Rate	Low	High	Low
Size / pixel	~ mm sq.	~ mm sq.	~10 umsq.
No. of Pixel	1 pixel	Usually 1 pixel	~million pixels
Incidence side	Front side	Front side	Front and back side
On-chip signal processing	No	No	possible
Energy measurement	No	No	Possible is X-ray region

Table 2 Advantages of SOIAPD over APD and PPD

Basic design and structure of our test SOIAPD chip

In SOIAPD, the high resistivity Si sensor part in SOI structure is replaced with APD structure as shown in fig 29.

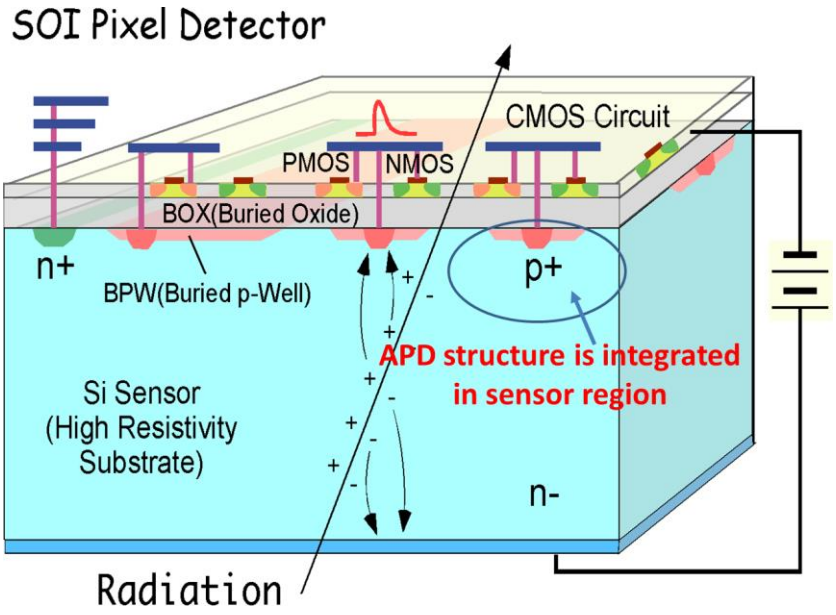


Figure 29 SOI structure

Our test chip was APDTEGh (model: MX1850-IK15) manufactured in 2015 KEK MPW run. Based on the requirement of MPW run mask at the time, Double Photodiode structure of Interrupted finger type (fig 30) with N+/PWell/Nsubstrate or P+/Nwell/Psubstrate was implemented. SOI Avalanche Double Photodiode and SOI reach-through APD are other typed of SOIAPD designs currently not implemented.

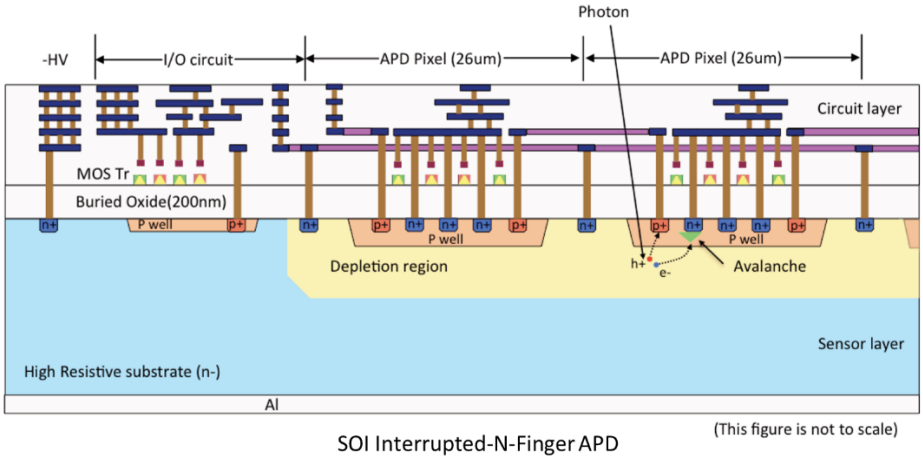


Figure 30 SOI Interrupted-N-Finger APD

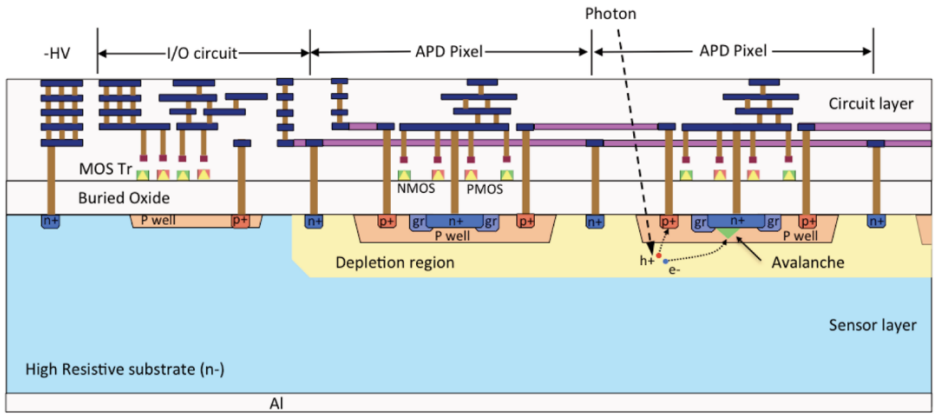


Figure 31 SOI Avalanche Double Photodiode

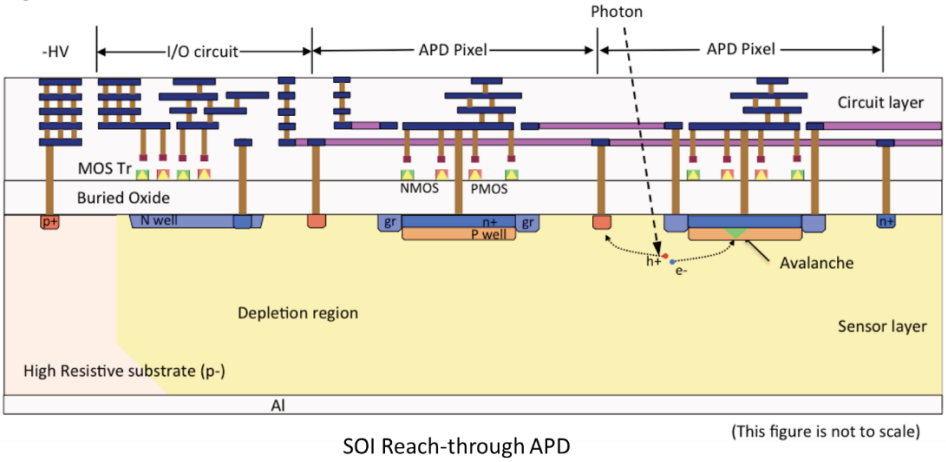


Figure 32 SOI Reach-through APD

8 types of SOIAPD structures with varying well size and polarity of electrodes were designed and fabricated in CZn, FZn, FZp and DSOI wafers. SOIAPD with structure shown in fig 33 (apd4_retype2_4pixel) was one tested more extensively for this thesis.

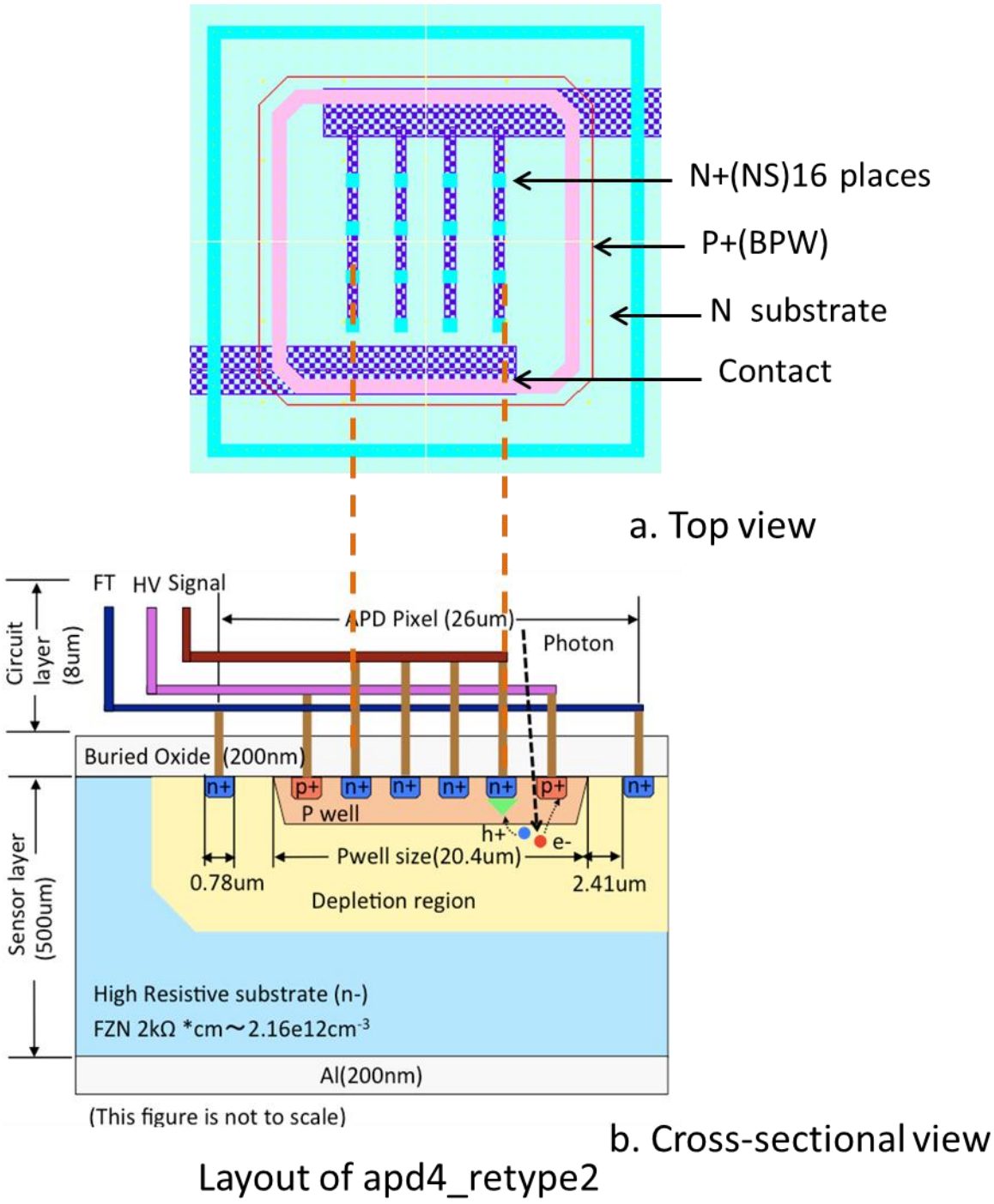


Figure 33 a. Top view of a single pixel of SOIAPD b. cross-sectional view of the same

The structure Fig 33 shows the pixel structure of our test SOIAPD. P-well and n+, p+ electrodes are implanted on top of n- substrate in the pixel. The substrate is set as floating, p+ as ground and the potential at n+ electrode is varied in the reverse bias voltages. Each of these structures is read out as a single pixel. Our test chips contain such single pixels as well as integrated super pixels

of 10*10 array of single pixels. Each pixel is 26μm *26μm size and array size is 260μm *260μm. The size of APDTEGh chip is 2.9mm*2.9mm and it contains many single pixels and arrayed pixels.

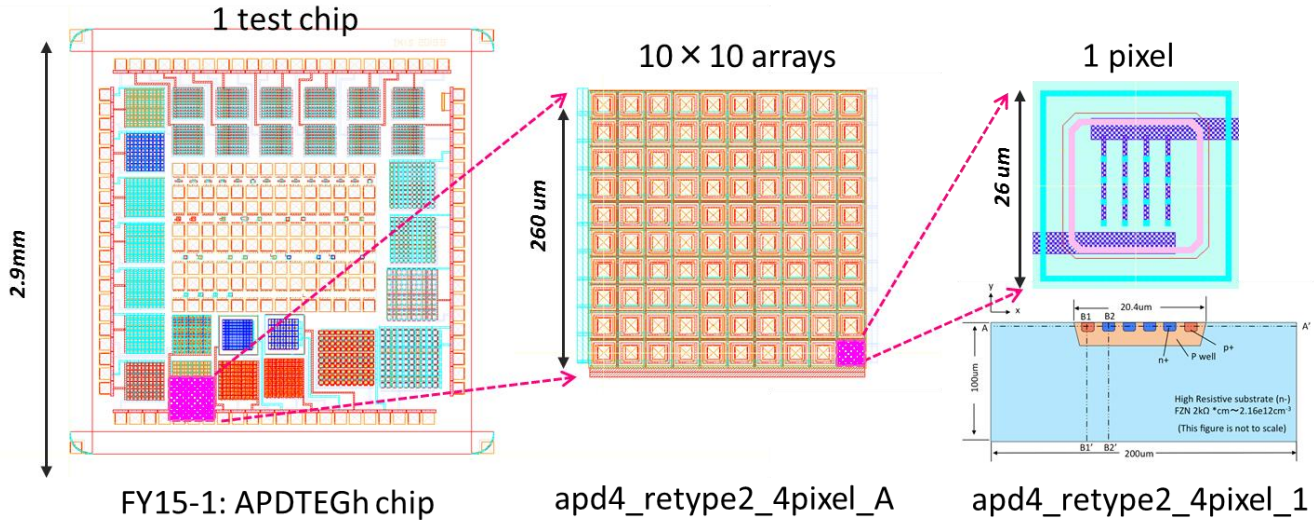


Figure 34 SOIAPD test chip APDTEGh

3.1 SOIAPD TCAD simulation

TCAD simulations were performed for prediction of our SOIAPD test chip characteristics. TCAD (Technology Computer-Aided Design) refers to the use of computer simulations to develop and optimize semiconductor processing technology and devices. It can be used to understand process of the device and the device physics. Various parameters that are otherwise very difficult or impossible to measure with fabricated device can be virtually measured using TCAD tools. By performing TCAD simulations, problems and potential issues under various conditions can be determined so that they can be fixed before fabrication which saves time and money. TCAD simulation software was first developed at Stanford University in 1977 and now different tools are available among which ENEXSS is the tool used in our simulations since it supports the manufacturing process used to fabricate SOI detectors. There are three tools that can be used in ENEXSS TCAD simulator:

3.1.1. Process simulator (Hyper Synthesised Process Simulator (HySyProS))

The process involved in fabrication like deposition, etching, implantation,etc of SOI detector are virtualized in the simulator using Simulation Control language(SCL). Impurities doping profile is predicted by solving diffusion equation in 3D environment using different models in HySyProS.

The impurities available for doping in ENEXSS are Boron(B) and Indium(In) from group III and Phosphorus(P) and Arsenic(As) from group V. Impurities are homogeneously doped by default but can also be manually varied using Gaussian or linear distributions. The generated 3D impurity profile is then used in device simulator.

3.1.2. Device simulator (HyDeLEOS)

Several electrical, mechanical, thermal and optical properties of the semiconductor device can be modelled using device simulator. HyDeLEOS is a device simulator tool available in ENEXSS which can be used to solve drift diffusion equation, quantum mechanical calculations and optical modes computations. HyDeLEOS is used for single device (threshold voltage, saturation and leakage current, capacitance, etc.), circuit design (wire resistance and capacitance, propagation delay), and the defect analysis (Electro Static Discharge (EDS) and latch-up). The behavior of the device is predicted by providing the geometry, characteristics, and internal operation conditions of the device to HyDeLEOS. It consists of three sections. First, in the preprocessing section (deleos_shell), the device structure, dopant distribution, electrode name and position, and mesh methods are defined and the generated file is then used in the calculation section "deleos". In calculation section (deleos) the basic equations of a semiconductor like drift diffusion equation, Poisson's equation, continuity equation, heat and electrical conduction equation, etc are solved using the device structure (defined in deleos_shell), boundary conditions, and electrical characteristics such as terminal current (defined in deleos). Finally, the post-processing section (deleos_extrac) parameters of the device like threshold voltage, drain current, scaling factor, etc are extracted and used for optimization function and prepared for extraction of characteristic values from electrodes.

Basic equations used in device simulation:

Poisson Equation

$$\nabla\left(\varepsilon\,\nabla\psi\right) = -\mathrm{q}(\mathrm{H_D} - \mathrm{N_A} - \mathrm{n} + \mathrm{p})$$

ψ : static potential, n: electron density, p: hole density

ε : dielectric constant, q: elementary charge

N_D: donor impurity concentration, N_A: acceptor impurity concentration

Equation of continuity of electron current

$$\frac{\delta n}{\delta t} = \frac{1}{q}\nabla J_n + G - R$$

$$J_n = -qn\mu_n\nabla\psi + \mathrm{qD}_n\nabla\mathrm{n} \qquad \text{(drift diffusion approximation)}$$

t: time, J_n: electron current, G: generation term, R: recombination term

μ_n: electron mobility, D_n: electron diffusion constant

Equation of continuity of hole current

$$\frac{\delta p}{\delta t} = \frac{1}{q}\nabla J_p + G - R$$

$$J_p = -qp\mu_p \nabla \psi + \mathrm{qD}_p \nabla \mathrm{p}$$

t: time, J_p: hole current, G: generation term, R: recombination term

μ_p: hole mobility, D_p: hole diffusion constant

3.1.3. Plotting tool (SGraph)

The results from above steps can be plotted using SGraph in 1D,2D or 3D as required. Useful features like bird's eye view of physical values, multiple graph, cross sectional view and 3D view of device structure, dopant distribution, potential distribution, etc are available with SGraph.

TCAD simulation and results

Electron density and electric field distribution of apd4_retype2_4pixel_1 pixel was predicted using the TCAD simulation tools explained above.

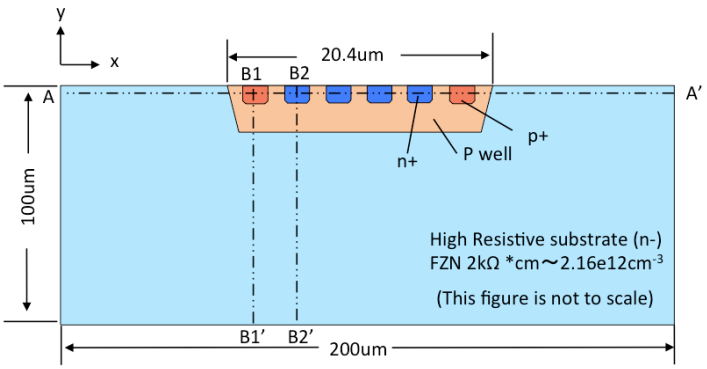


Figure 36 apd_retype2_4pixel structure

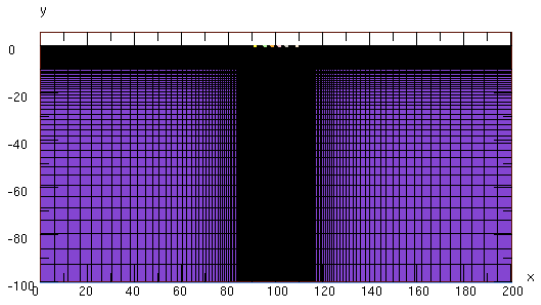


Figure 35 TCAD mesh creation for pixel on the right

First virtual substrate of thickness 100µm and width 200µm is created as shown in fig 35. Photo-resistors of width 5µm and SiO2 layer of width 248nm are deposited and etching is done. P well is then implanted and photo-resistors are removed. p+(PS) and n+(NS) are implanted in that area in concentrations as shown in fig37. After that, annealing is performed at 1050℃ for 10 seconds.

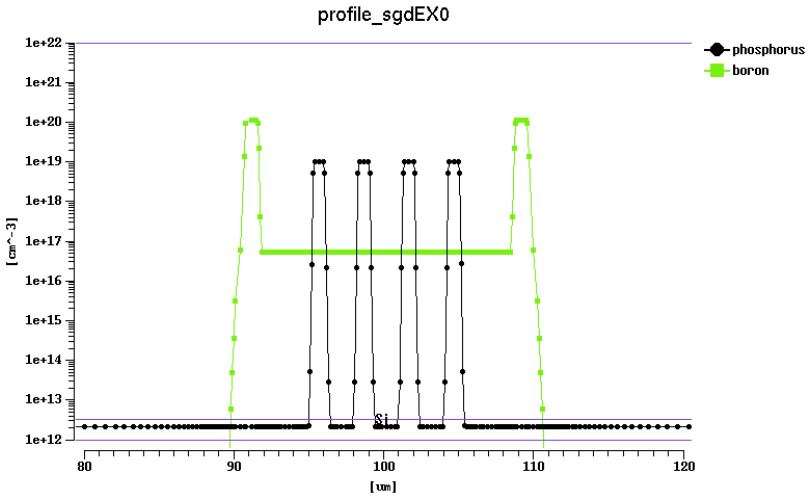


Figure 37 Impurity concentration (depth=-0.2µm)

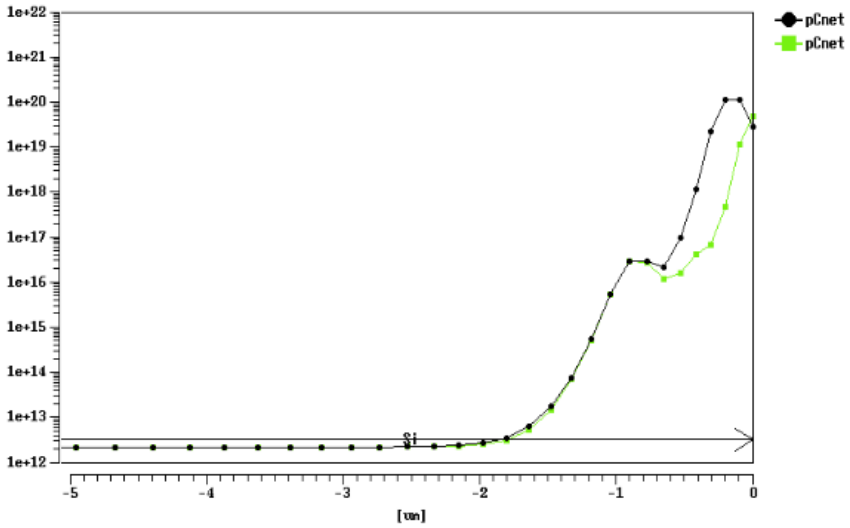


Figure 38 . Impurity concentration (Center.NS,PS)

As reverse bias is applied between p+(PS) and n+(NS) in the created TCAD model, following results were seen. In the first row of fig 40 below, reverse bias was varied from 0V to -20V and expansion of depletion region was plotted in 2D figure. In the second row, change in electron density in depth-wise direction from the center of the detector is visualized. As can be seen in figure 40, at higher reverse bias voltage, depletion region expands sweeping away the electrons decreasing the electron density.

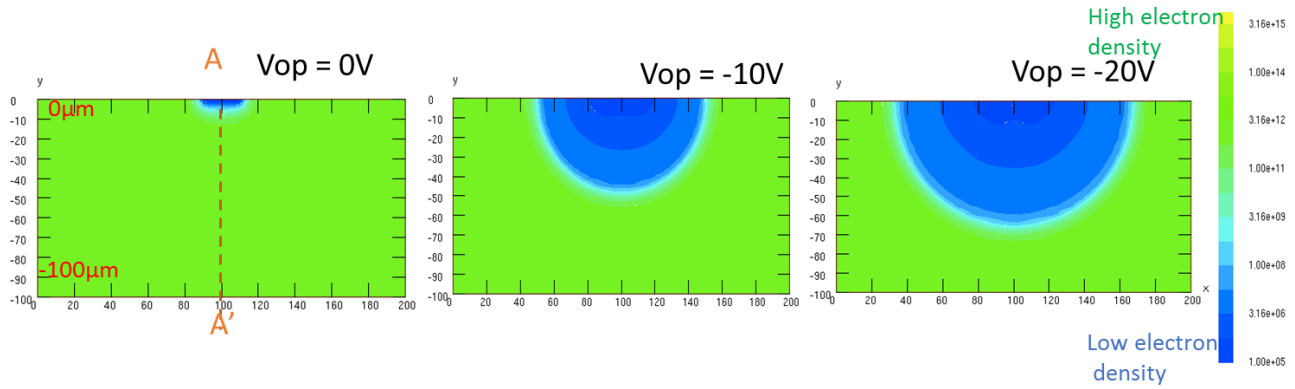


Figure 39 Electron density profile at different voltages

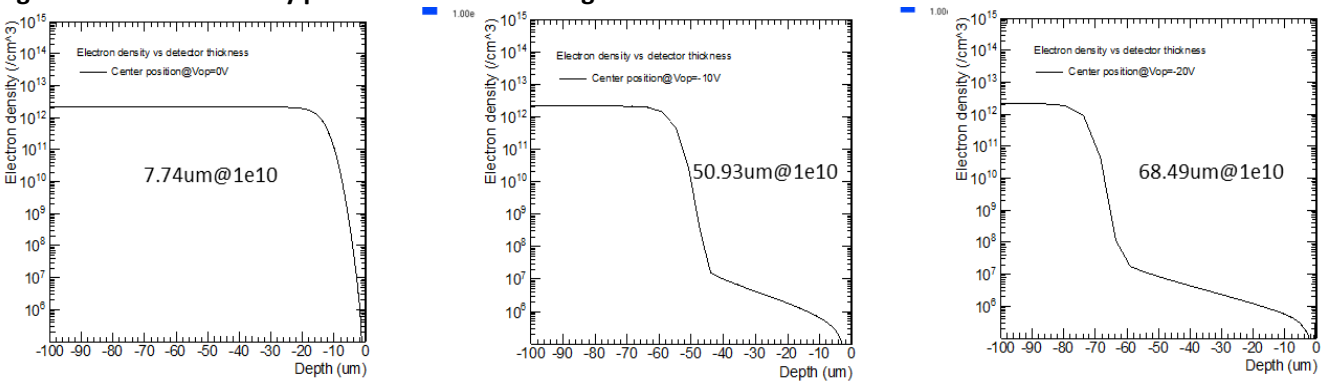


Figure 40 Electron density at different depths of the pixel

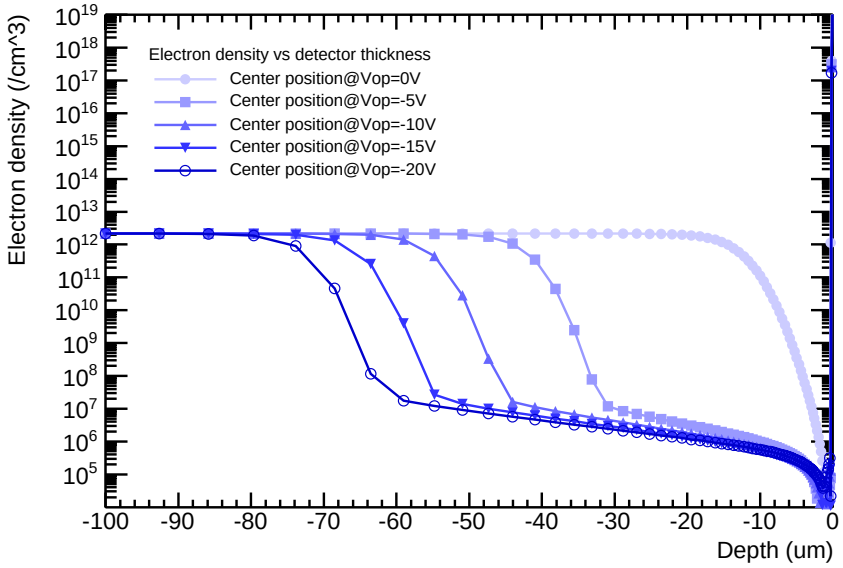


Figure 41 Electron density at different depths from the top (at different reverse voltages)

Simulation results of electric field (fig 42) in the whole of pixel is shown in the plots below. The second-row plots show magnified view of upper part of pixel with n+ (NS) and p+(PS). Avalanche mechanism occurs in this region where electric field strength is high.

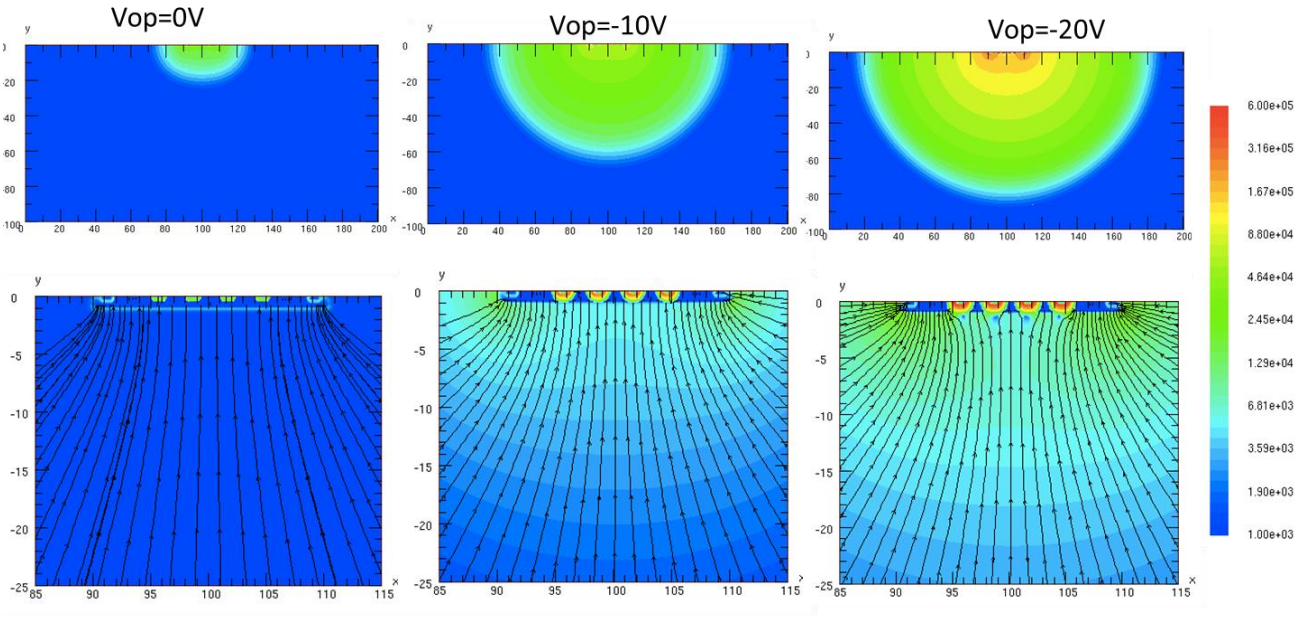


Figure 42 Electric field intensity at different regions of SOIAPD pixel

Fig 35 shows plotted values of electric field of the region above and different operation voltages. Large electric field (~10^6 V/cm) appears to be concentrating around the edges of n+. The flat region shows electric field of about 10^4 V/cm. Avalanche breakdown takes place in linear mode at electric field strengths of about 300kV/cm ~ 800kV/cm. SOIAPD is operated at k factor < 0.2 range since Geiger mode multiplication starts above that which is not desired for SOIAPD.

Fig 34.

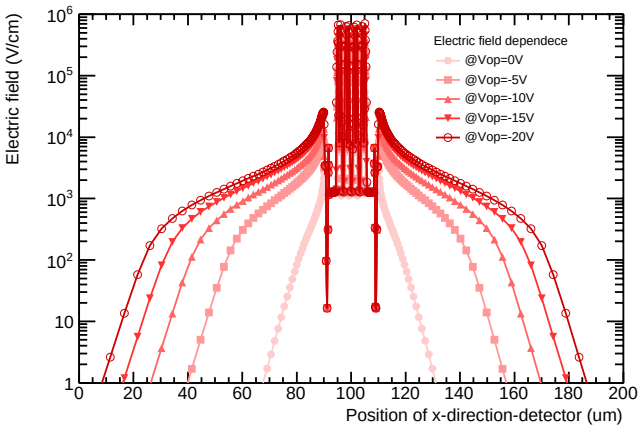


Figure 43 Electric field intensity variation across different regions of SOIAPD (at y=-0.2µm)

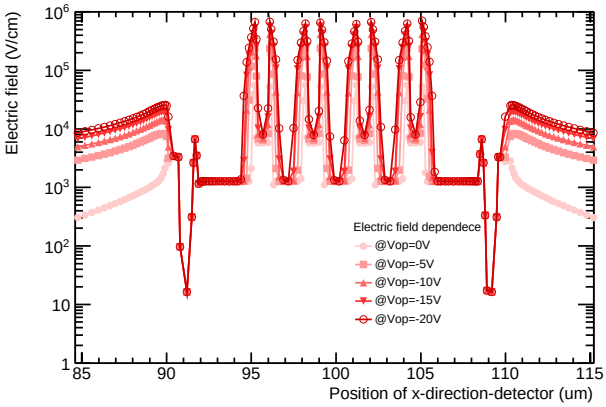


Figure 44 magnified view of the previous figure to show the region near n+, p well

Chapter 4 SOIAPD Measurements

4.1 IV and CV Measurement

IV and CV measurements were made using bare APDTEGh (our SOIAPD) chips fabricated in CZn, FZn, FZp and DSOI wafers. FZ (Float-zone silicon) and CZ (Czochralski silicon) are two growth techniques for mono-crystalline silicon. Majority of the commercially grown silicon is Czochralski silicon due to the better resistance of the wafers to thermal stress, the speed of production, the low cost and the high oxygen concentration that offers the possibility of Internal Gettering. Float-zone silicon is a high-purity alternative to crystals grown by the Czochralski process. The concentrations of light impurities, such as carbon and oxygen, are extremely low. Another light impurity, nitrogen, helps to control microdefects and brings about an improvement in mechanical strength of the wafers, and is now being intentionally added during the growth stages [26]. Double SOI wafers are based on CZn and since 2014 production of double SOI wafers based on CZp have also started.

Table 3 Basic data of different wafer types

Wafer type	CZN	FZN	FZP	DSOI
resistivity	700Ω·cm	2kΩ·cm	25kΩ·cm	1kΩ·cm
Wafer thickness	510 um	510 um	510um	310um

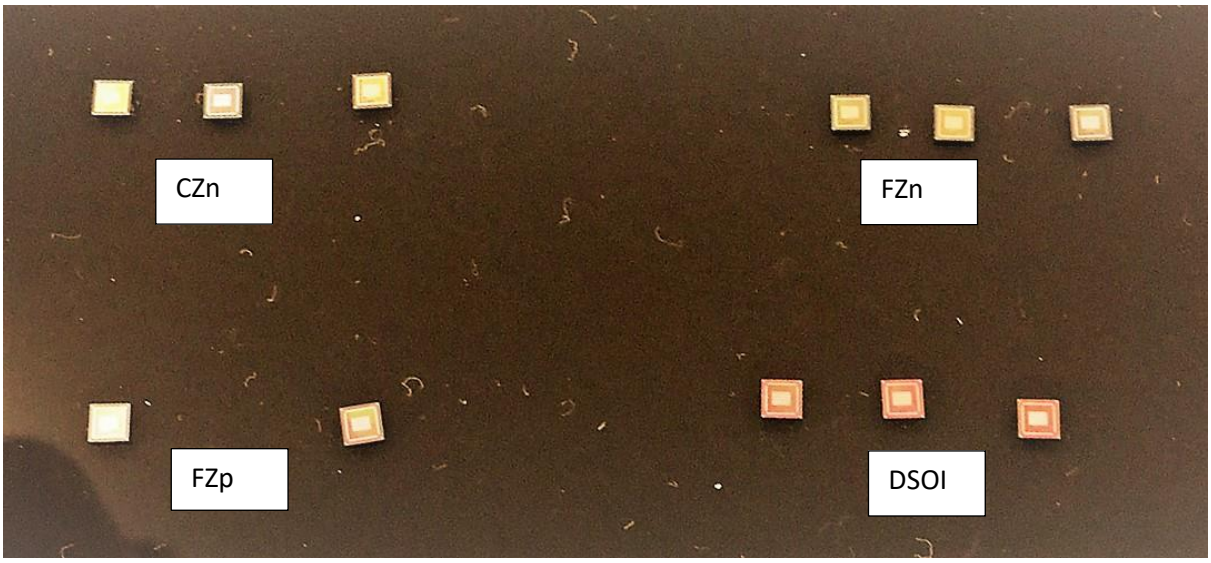


Figure 45 Test SOIAPD chips

Measuring device used was Keithley 4200-Semiconductor Characterization System. This device can provide voltage range of up to 210V with minimum resolution of 1μV. And with measurable current resolution is up to 100aA (10^{-18}A), it is a very sensitive machine. Probers pins are used to make connection with the terminal contacts as shown in fig 46 and 47.

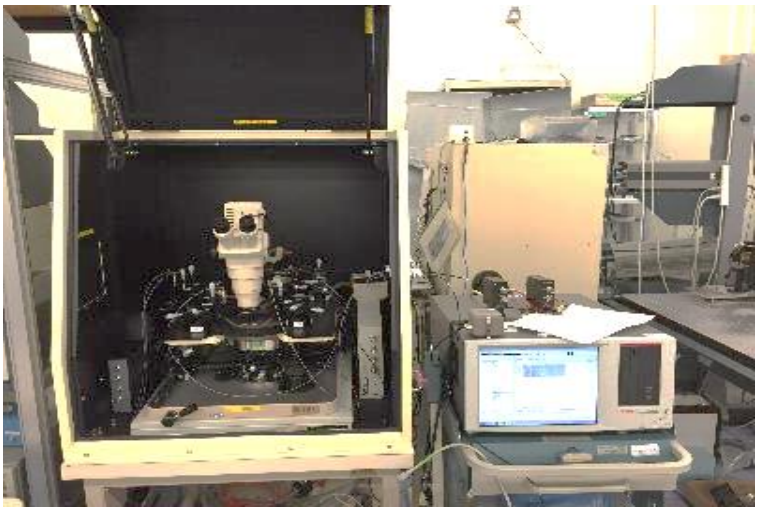


Figure 46 Kiethley 4200-SCS Semiconductor Characterization System

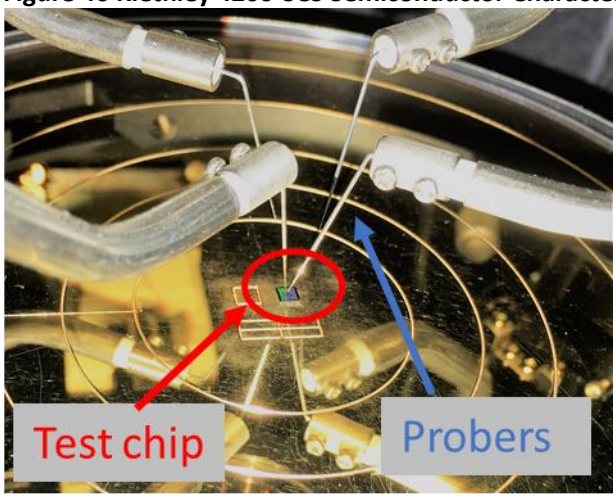


Figure 47 Test chip during measurement using Kiethley-4200-SCS

In each of the measurements of dark current fig 48 , low leakage current (~1^{-14} A for single pixels and ~1^{-12}A for 10*10 array pixel) was seen and breakdown voltage was about 18V for all.

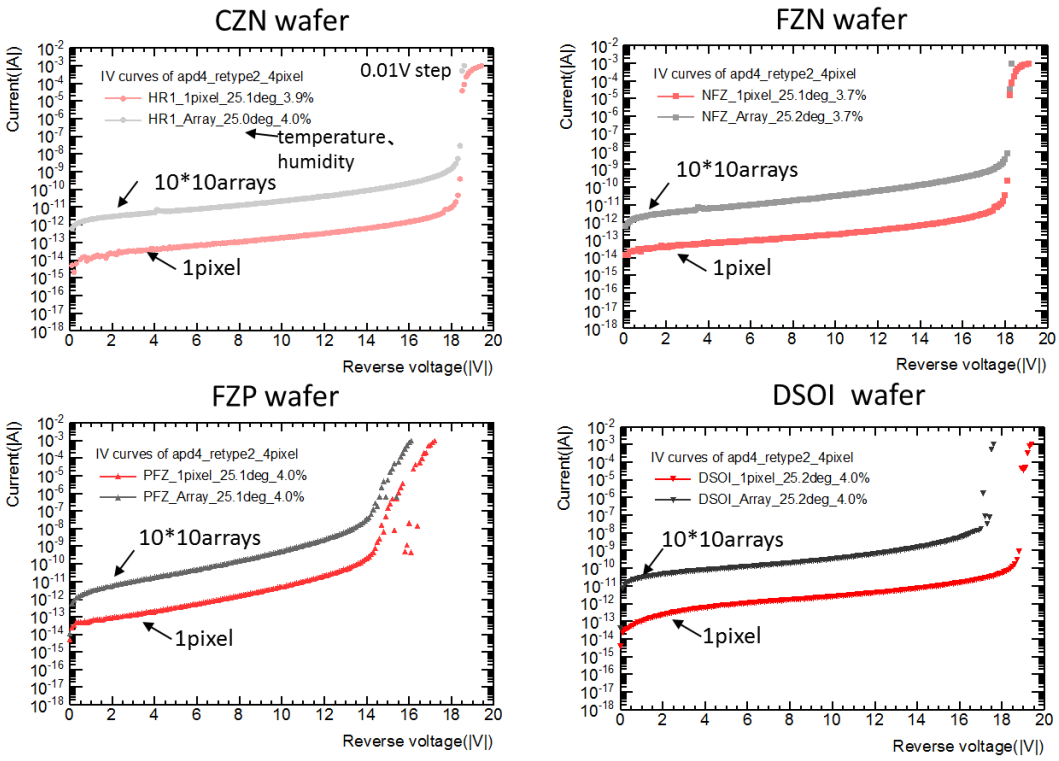


Figure 48 Dark current from 10*10-pixel array and single pixel

Figure 49 shows the ratio of dark current between array and single pixel. Leakage current of 10*10 array pixels is found to be about 10^2 times that of single pixels as expected which confirms the operation of SOIAPD in linear multiplication mode.

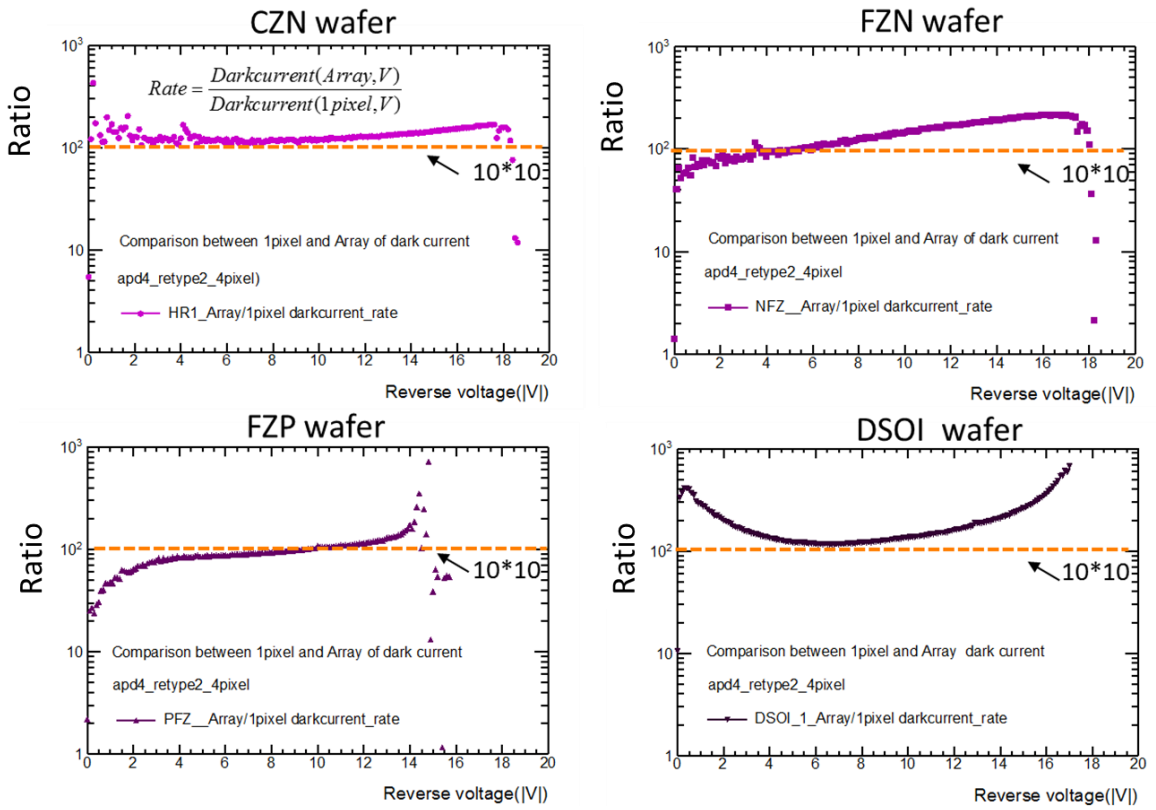
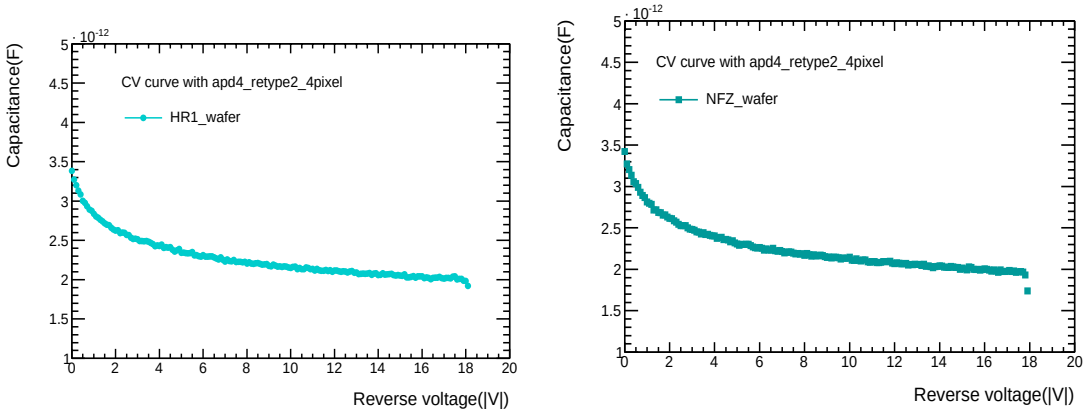


Figure 49 Ratio of dark current from 10*10-pixel array to that from a single pixel

CV measurments show that the SOIAPD has very low capacitance of about 3pF which is good for APD.



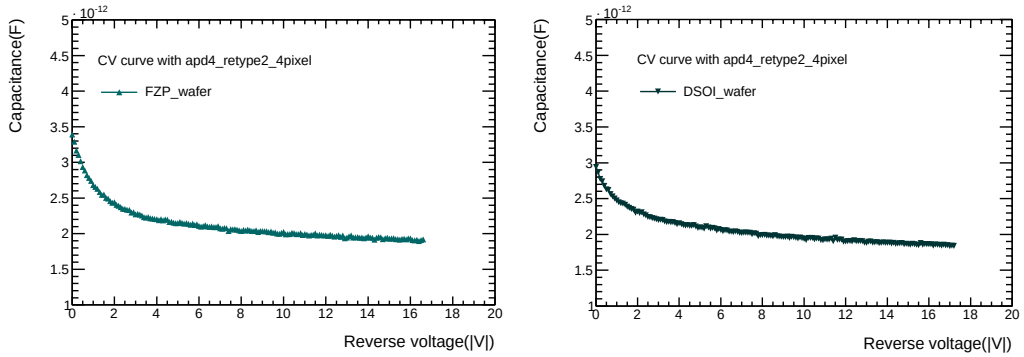


Figure 50 Capacitance versus reverse bias voltage for different wafer type samples

1/C^2 versus Reverse voltage plots are shown in figure 51. Doping profile of the SOIAPD can be calculated using these plots.

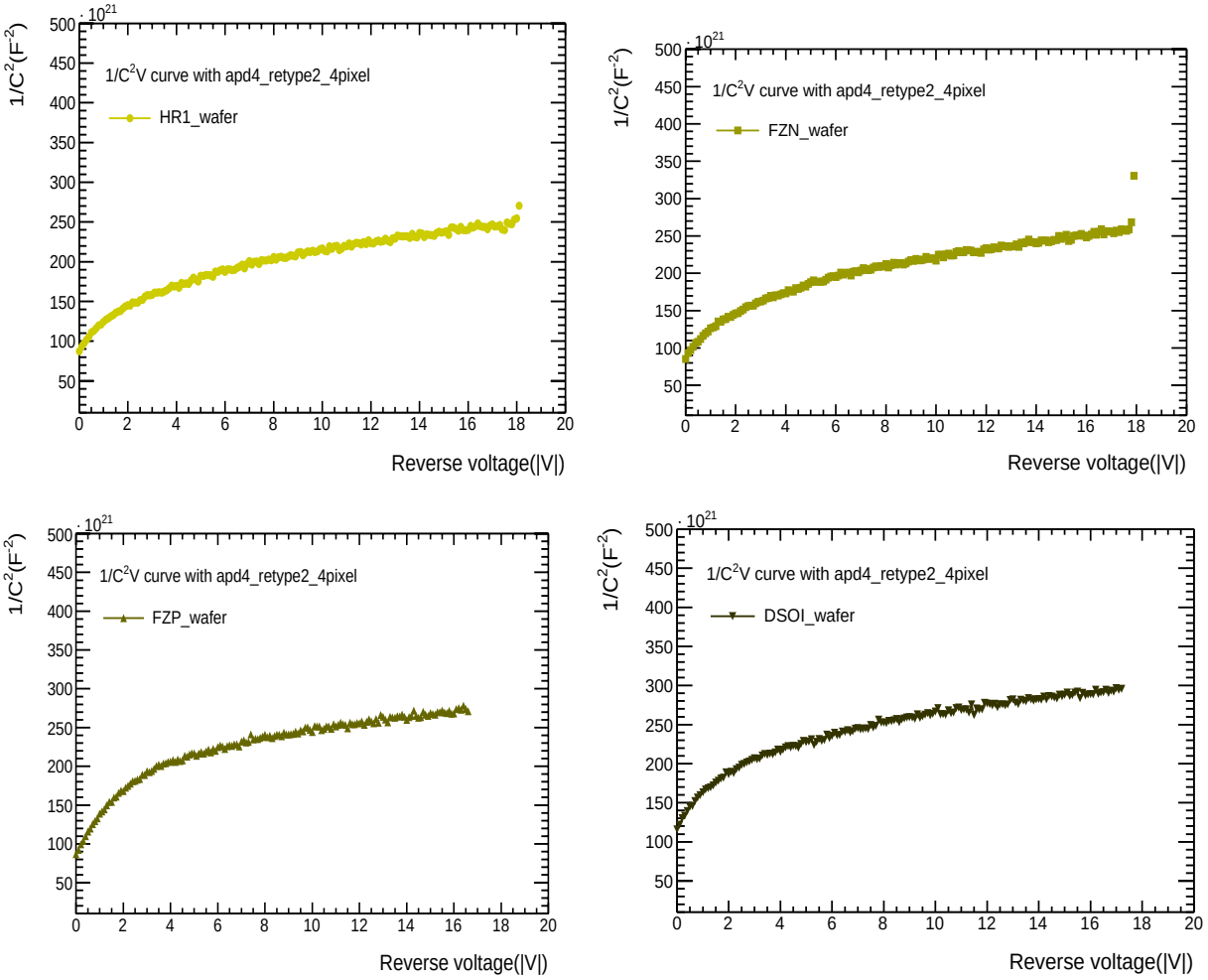


Figure 51 $1/C^2$ versus reverse bias voltage

4.2 Temperature dependence of SOIAPD

Figure 52 Temperature chamber

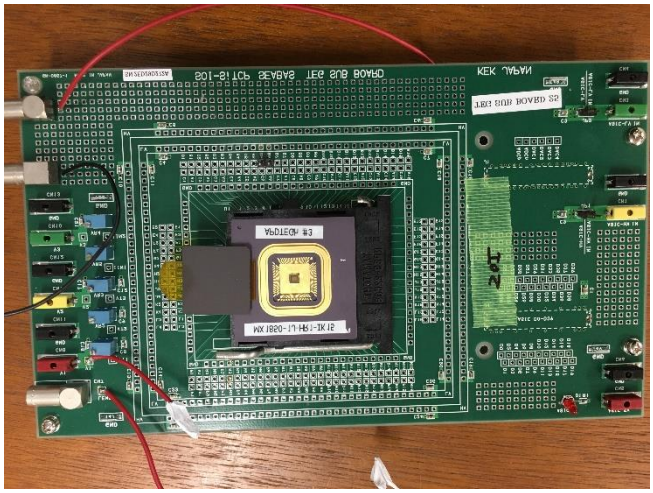


Figure 53 Sub-board for testing

Temperature dependence was measured by setting up the wire bonded APDTEGh chip in a custom manufactured board and varying temperature using temperature chamber (figure 53). Measurements were made by cooling down the chip to 20^0C, 0^0C, -20^0C, -40^0C and -60^0C temperatures.

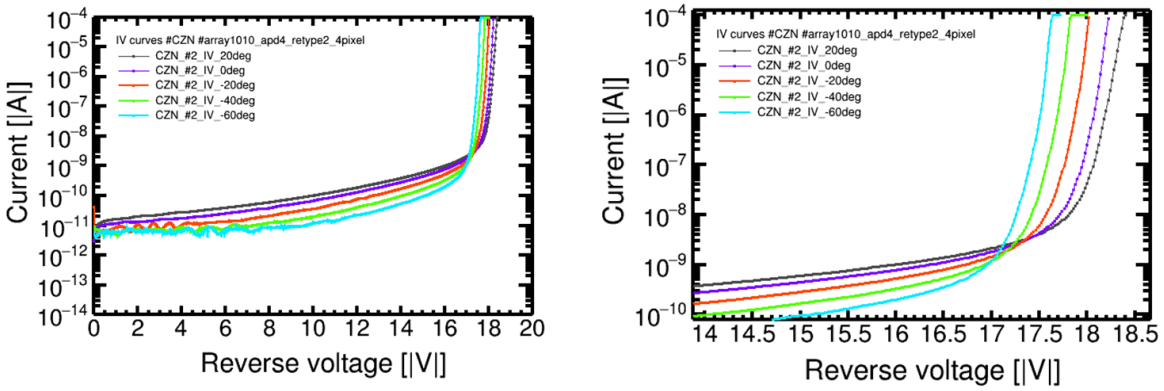


Figure 54 Dark current vs reverse voltage curves at varying temperatures (CZN wafer), original graph on the right, same graph magnified in near breakdown voltage region on the right

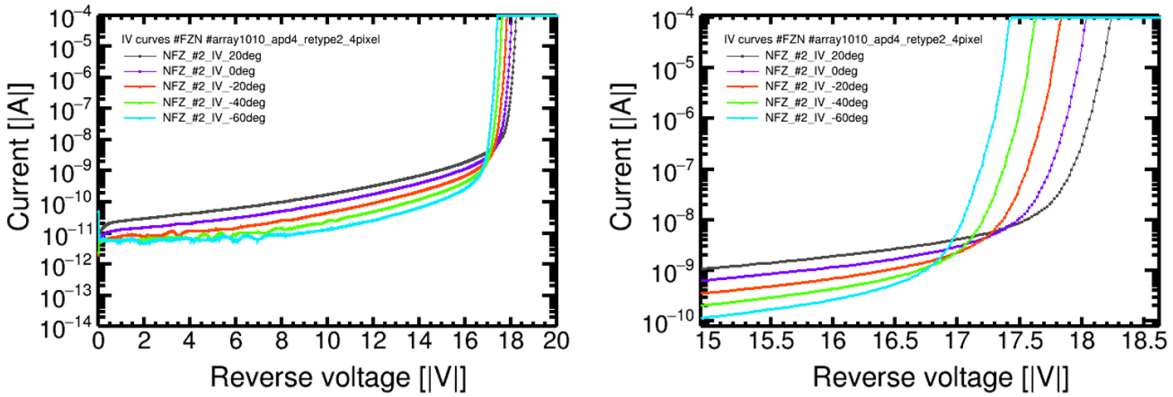


Figure 55 Dark current vs reverse voltage curves at varying temperatures (FZN wafer), original graph on the right, same graph magnified in near breakdown voltage region on the right

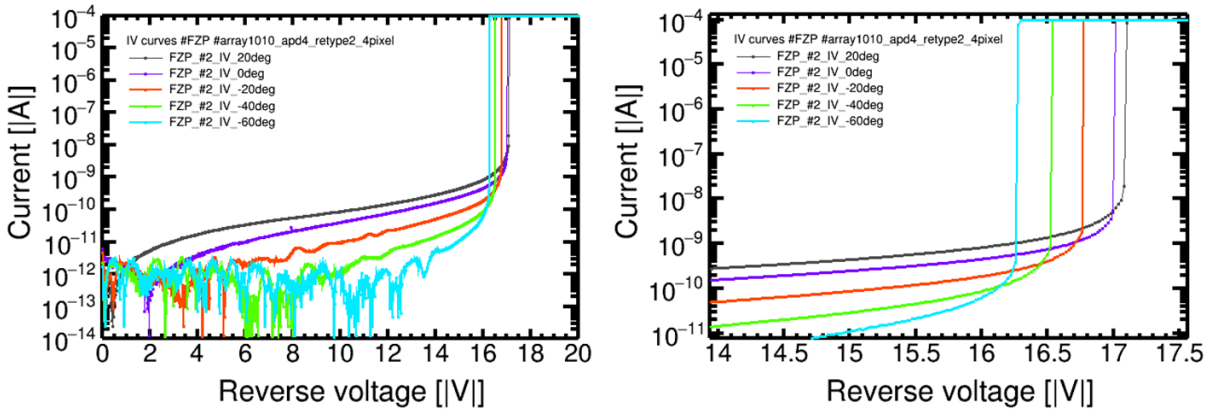


Figure 56 Dark current vs reverse voltage curves at varying temperatures (FZP wafer), original graph on the right, same graph magnified in near breakdown voltage region on the right

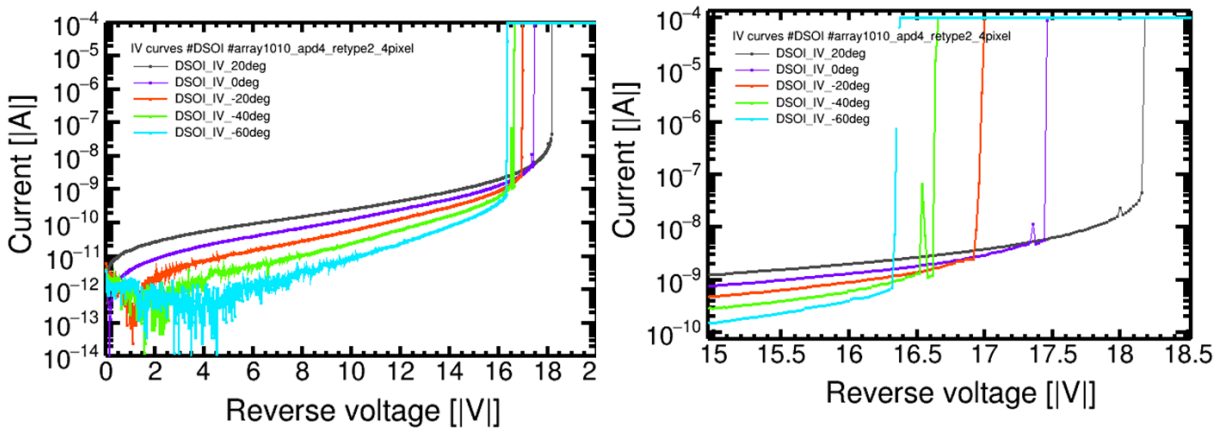


Figure 57 Dark current vs reverse voltage curves at varying temperatures (DSOI wafer), original graph on the right, same graph magnified in near breakdown voltage region on the right

Temperature (^{0}C)	CZN	FZN	FZP	DSOI
20	17.1V	17V	16.2V	16.4V
0	17.3V	17.2V	16.4V	16.6V
-20	17.5V	17.4V	16.7V	16.9V
-40	17.7V	17.6V	16.9V	17.5V
-60	17.9V	17.9V	17V	18.2V

Table 4 Breakdown voltages (here taken as voltage where current exceeds 10^5A) at different temperatures

Due to the increase in vibration of crystal lattice with increase in temperature, accelerated carriers collide with the lattice before reaching sufficient energy level to trigger impact ionization. Therefore, greater reverse bias voltage is required (increasing reverse bias voltage results in more carriers having sufficient initial energy to trigger avalanche mechanism) to trigger avalanche mechanism at higher temperature (as the availability of carriers with sufficient energy reduces with increase in temperature) as seen in the figures 54 to 57, where breakdown voltage increases with increase in temperature. Again, greater dark current seen in the measurements at higher temperature is because of availability of more heat generated electrons and holes which can be explained as follows.

In a one sided abrupt P+/N junction, reverse bias saturation current can be expresses as follows as the sum of diffusion current in the neutral region and current generated in the depletion region.

$$I_R \cong q\sqrt{\frac{D_p}{\tau_p}}\frac{n_i^2}{N_D} + \frac{qWn_i}{\tau_g} \qquad (1)$$

D_p: Hole diffusion current, τ_p：Hole lifetime, τ_g：generation time,

N_D：donor density（N side） n_i：Intrinsic carrier density,W：depletion region width,

k：Boltzmann constant, T：Temperature, q：unit electric charge

It can be expressed as follows using bandgap of intrinsic carrier density Eg (1.12 eV in case of Si), state density of valence and conduction bands Nc, Nv.

$$n_i = \sqrt{N_c N_V} \exp\left(-\frac{E_g}{2kT}\right) \propto \exp\left(-\frac{E_g}{2kT}\right) \quad (2)$$

Using the equation for avalanche mechanism and mobility of holes μ h , diffusion coefficient can be expressed as follows.

$$D_p = \frac{\mu_h kT}{q} \quad (3)$$

Using equations (1) and (3), in case when diffusion current is dominant, considering the effect of only the term n_i^2,

$$I_R \cong \sqrt{\frac{q\mu_h kT}{\tau_p}} \frac{n_i^2}{N_D} \propto \exp\left(-E_g \frac{1}{kT}\right) \quad (4)$$

From equation (4) it is seen that current flow increases with increase in temperature, which was also seen from the results of temperature dependence of dark current of SOIAPD.

4.3 LED response of SOIAPD

LED output from standard fiber coupled LED (model M530F-1, light wavelength: 53nm) was used along with LED driver (model: DC2200). LED output could be varied by changing the current from 0.1mA to 1000mA. Before measuring the LED response of SOIAPD, standard photodetectors were used as reference. HPK S1787-12 was one of those and it had light sensitivity of 0.27A/W at 530nm wavelength. It was operated at 9V (max operation voltage: 10V).

Figure 58 LED device (M530F-1)

Table 5 LED device specifications

Specification	Value
Color	Green
Nominal Wavelength	530 nm
Test Current for Typical LED Power	1000 mA
Maximum Current (CW)	1000 mA
Bandwidth (FWHM)	30 nm
Electrical Power	3100 mW
Typical Lifetime	>50 000 h
Operating Temperature (Non-Condensing)	0 to 40 °C
Storage Temperature	-40 to 70 °C
Emitter Size	1 mm x 1 mm
Risk Group[a]	RG0 - Exempt Risk Group

a. According to the standard IEC 62471:2006, Photobiological Safety of Lamps and Lamp Systems

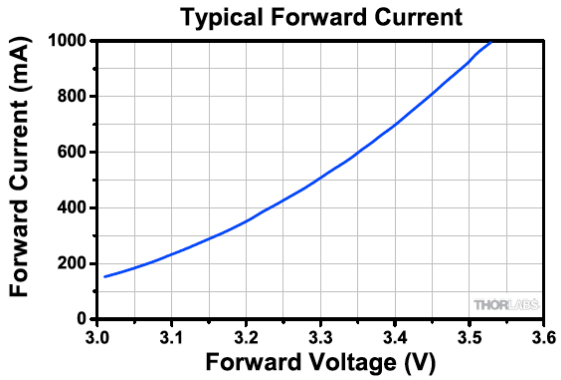


Figure 59 Forward current vs forward voltage of LED device [Hamamatsu Photonics HPK]

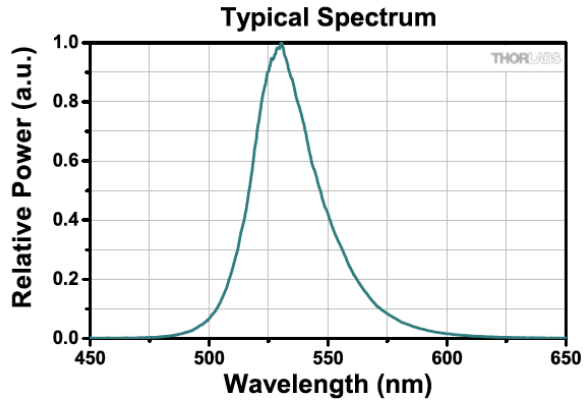


Figure 60 wavelength distribution of output LED light [HPK]

A photodetector (model: S1787-12) was use as reference to calculate the power output from the LED.

■ 一般定格／絶対最大定格

型名	窓材 *	受光面サイズ (mm)	有効受光面積 (mm^2)	絶対最大定格 逆電圧 V_R Max. (V)	絶対最大定格 動作温度 Topr (°C)	絶対最大定格 保存温度 Tstg (°C)
S1787-04	V	2.4 × 2.8	6.6	10	-10 ～ +60	-20 ～ +70
S1787-08	R					
S1787-12	I					

* 窓材 R: 樹脂コーティング, V: 視感度補正フィルタ, I: 赤外カットフィルタ

■ 電気的および光学的特性 (指定のない場合は Typ. Ta=25 °C)

型名	感度波長範囲 λ (nm)	最大感度波長 λp (nm)	受光感度 S (A/W) λp	GaP LED 560 nm	He-Ne レーザ 633 nm	赤外感度比 (%)	短絡電流 Isc 100 lx (μA)	短絡電流の温度係数 (%/°C)	暗電流 I_D V_R=1 V Max. (pA)	暗電流の温度係数 T_{CID} (倍/°C)	上昇時間 tr V_R=0 V R_L=1 kΩ (μs)	端子間容量 Ct V_R=0 V f=10 kHz (pF)	並列抵抗 Rsh V_R=10 mV Min. (GΩ)	並列抵抗 Rsh V_R=10 mV Typ. (GΩ)
S1787-04	320～730	560	0.3	0.3	0.19	10	0.65	-0.01	10	1.12	2.5	700	10	100
S1787-08	320～1100	960	0.58	0.33	0.38	-	5.6	0.1						
S1787-12	320～1000	650	0.35	0.3	0.34		2.3		20		0.5	200	1	10

Figure 61 Specifications of reference photodetector [HPK]

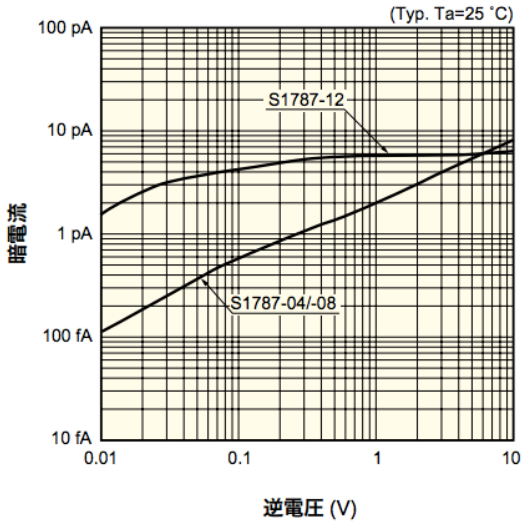


Figure 62 Dark current of reference photodetector as given by production specification [HPK]

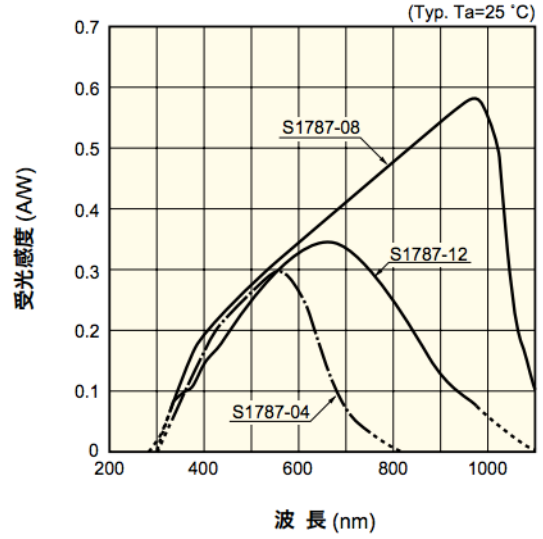


Figure 63 light sensitivity of reference photodetector versus wavelength of flight [HPK]

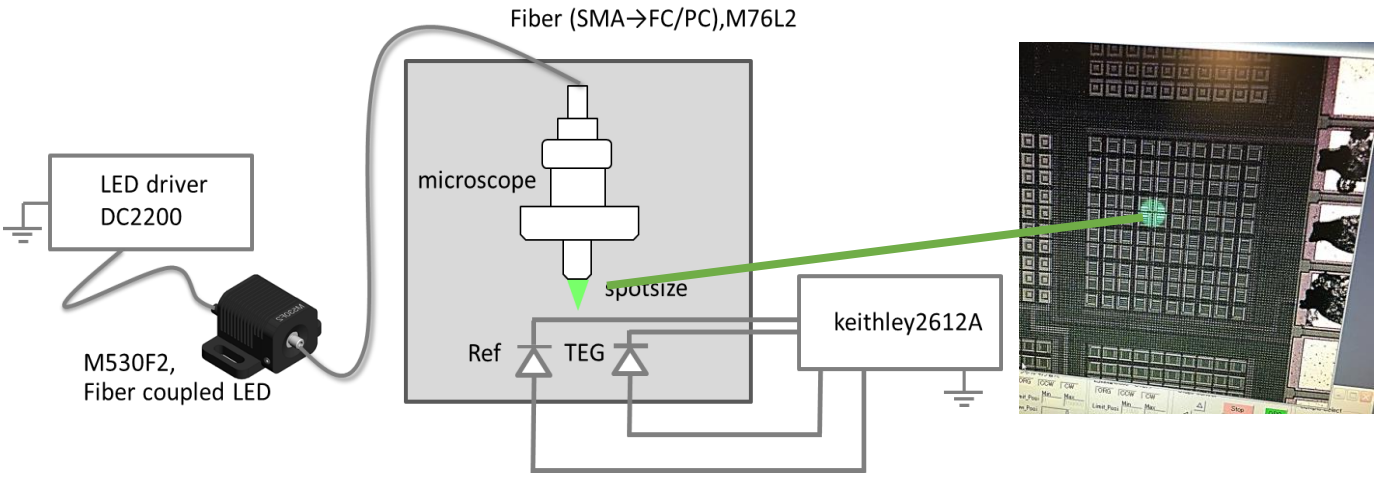


Figure 64 Setup for LED response measurement

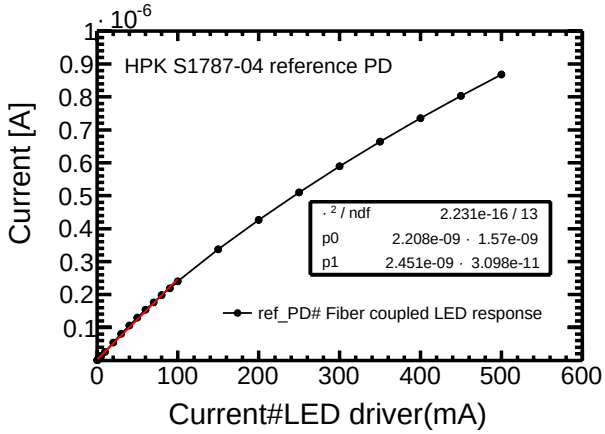


Figure 65 LED response of reference photodetector

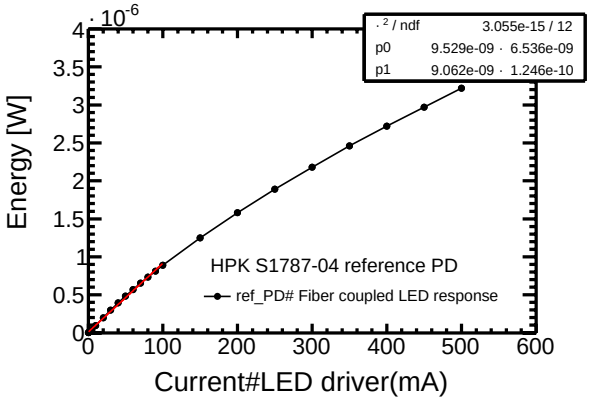


Figure 66 LED response of reference photodetector in terms of power

In figure 65, current from photodetector is plotted against output power of LED in mA. In the figure 66, current from photodetector is changed to energy absorbed by the photodetector per second. It was found that for incident LED power below 100mA, detected number of photons increased linearly, but above 100mA sensitivity of the photodetector seems to decrease.

Next, LED response of SOIAPD was measured. For better sensitivity, due to more pixels and minimizing error during LED irradiation, 10*10 array (26µm* 26µm size) was used. LED output power of ranging from 50mA to 500mA with wavelength 530nm was used. Keithley 2612A was used for this IV measurement.

From fig 67, increase in current can be seen with increase in input LED power. The fig 68,. is adjusted to show the current from SOIAPD per unit input LED power and all the curves appear to coincide with each other (except at breakdown voltage) confirming the photodetective characteristic of the SOIAPD.

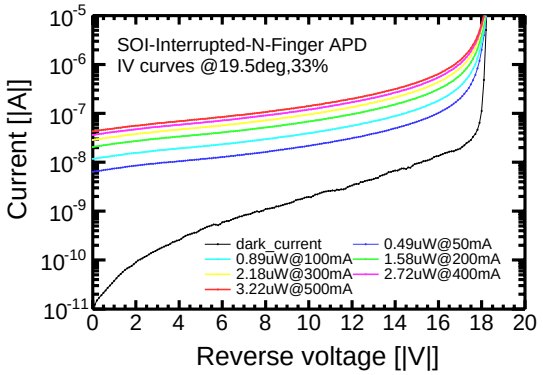


Figure 67 LED response at different incident led powers versus breakdown voltage

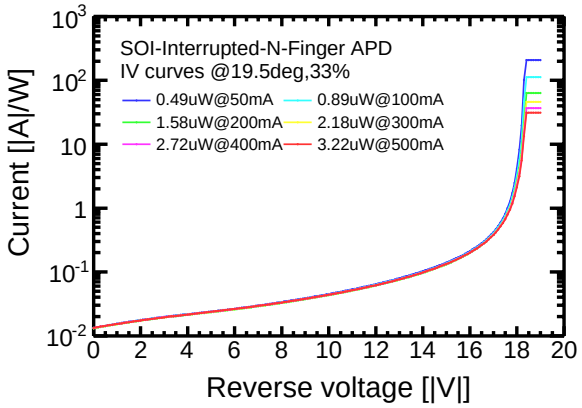


Figure 68 LED response per watt of incident led power, measured at different led intensities

In the fig 69, gain is plotted against reverse bias voltage. From this graph, it can be inferred that it can produce internal gain of up to 100 times as well as it is also confirmed that gain per reverse voltage increase is constant. From fig 70 it is seen that the multiplication factor or gain is low below 17V and above 17V to breakdown voltage, gain increase is very high. This characteristic is due to the difference in k factor as explained in previous chapters.

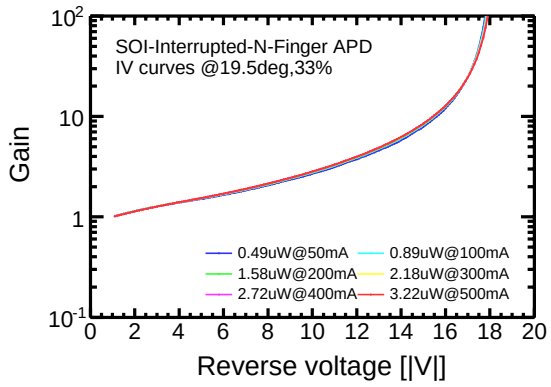


Figure 69 Change in gain with reverse bias voltage

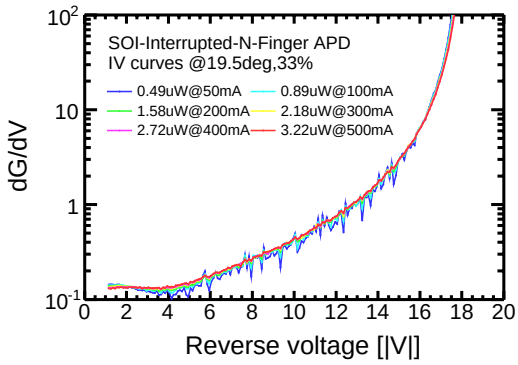


Figure 70 rate of change of gain at different bias voltages

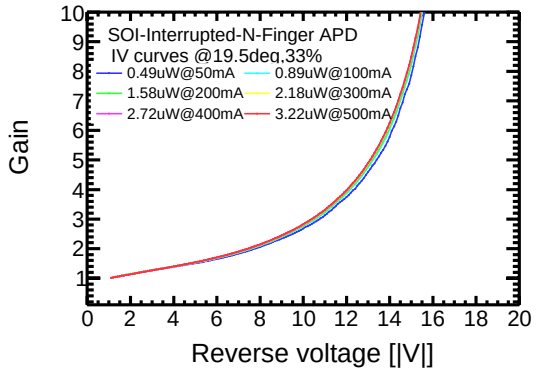


Figure 71 change in gain with reverse voltage: alternative measurement

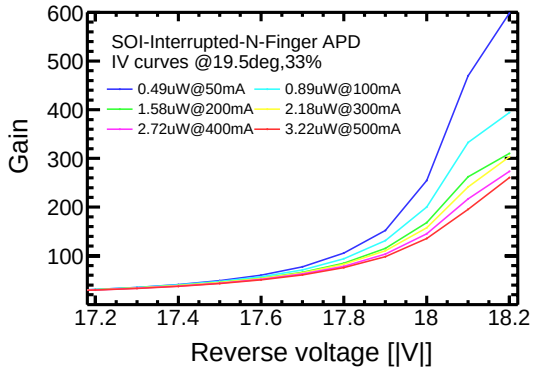


Figure 72 change in gain with reverse voltage: alternative measurement

Operation of SOIAPD in as a detector with internal gain was successfully demonstrated. By identifying suitable voltage range for operation in linear multiplication mode SOIAPD could be used in future high performance detectors. As seen in figure 72, gain of more than 200~600 times is also possible without quenching resistor.

4.4 Co-60 γ irradiation

We performed ɤ-ray irradiation at food irradiation building, Takasaki Advanced Radiation Research Institute, Japan Atomic Energy Agency from 2017/01/06 to 2017/01/08. SOIAPD chips each of CZn, FZn , FZp and DSOI wafer were subjected to radiation. Each sample was irradiated up to 200kGy except 1MGy for DSOI based chip.

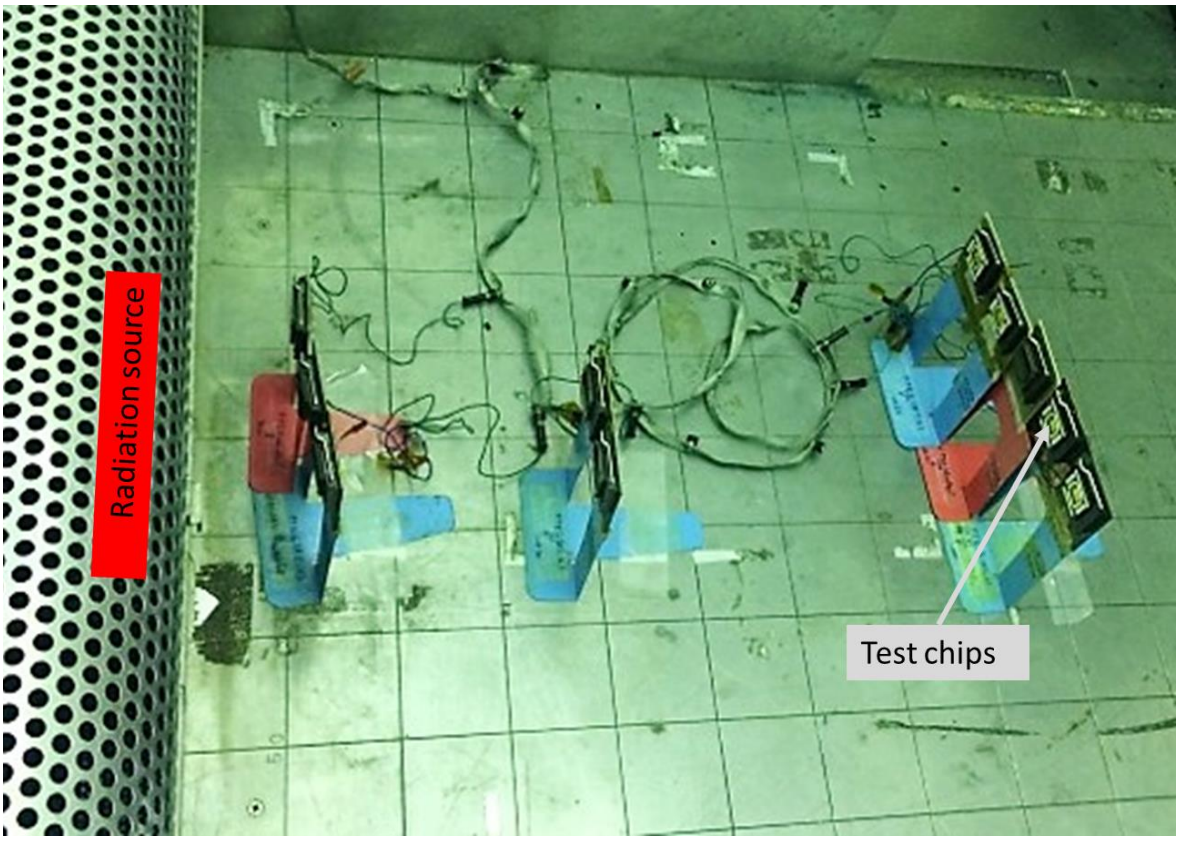


Figure 73 γ ray irradiation setup at Takasaki irradiation facility

The samples were positioned for irradiation based on the provided radiation dose distribution curve below.

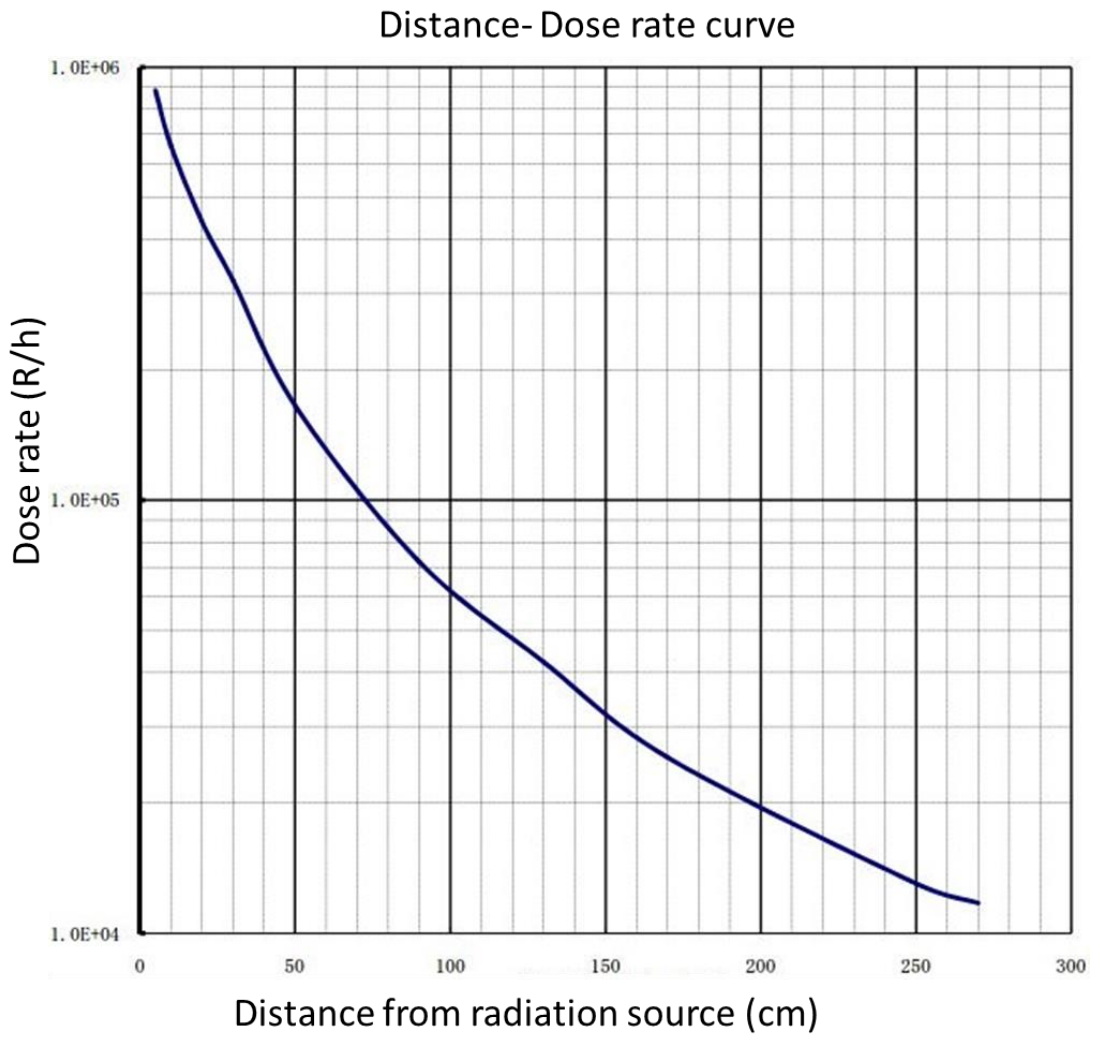


Figure 74 Radiation dose rate to distance curve

Distance from the radiation source (cm) Height of measurement point 22.5cm

	0	20	40	60	80	100		
5	8.83E+05	7.44E+05	4.75E+05	2.32E+05	1.42E+05	7.38E+04		
10	6.59E+05	5.98E+05	4.07E+05	2.18E+05	1.37E+05	7.32E+04		
20	4.39E+05	4.07E+05	3.04E+05	1.91E+05	1.26E+05	7.44E+04		
30	3.22E+05	2.96E+05	2.34E+05	1.60E+05	1.06E+05	7.26E+04		
50	1.65E+05	1.57E+05	1.36E+05	1.12E+05	8.65E+04	6.47E+04		
90	7.20E+04	7.02E+04	6.71E+04	5.80E+04	4.91E+04	4.22E+04		
130	4.23E+04	4.01E+04	3.92E+04	3.57E+04	3.27E+04	2.93E+04		
170	2.55E+04	2.50E+04	2.43E+04	2.32E+04	2.12E+04	2.03E+04		
250	1.30E+04	1.28E+04	1.26E+04	1.25E+04	1.22E+04	1.16E+04		
270	1.17E+04	1.17E+04	1.16E+04	1.13E+04	1.09E+04	1.05E+04		

Figure 75 radiation dose distribution table

IV measurements for dark current and led response were made to investigate any changes before and after irradiation.

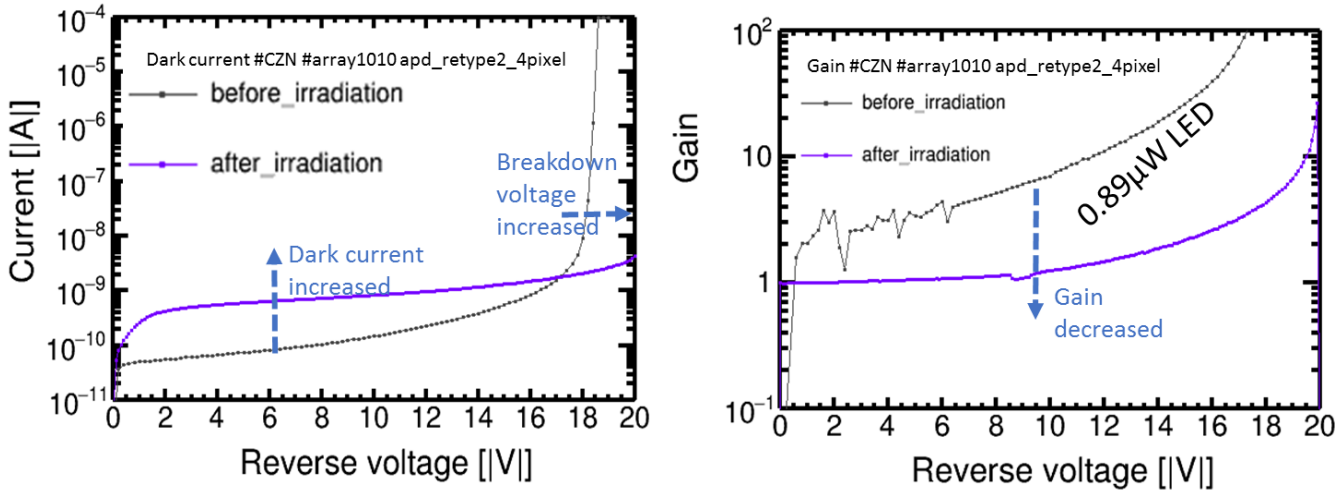


Figure 76 Change in dark current (left) and gain (right) before and after 200kGy irradiation in CZn based APTTEGh pixel

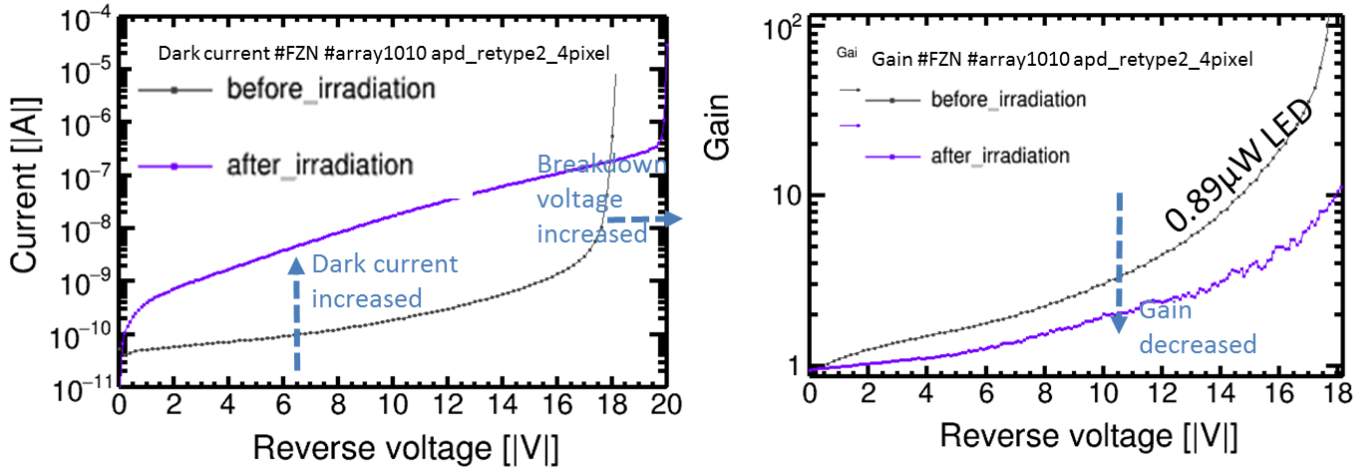


Figure 77 Change in dark current (left) and gain (right) before and after 200kGy irradiation in FZn based APTTEGh pixel

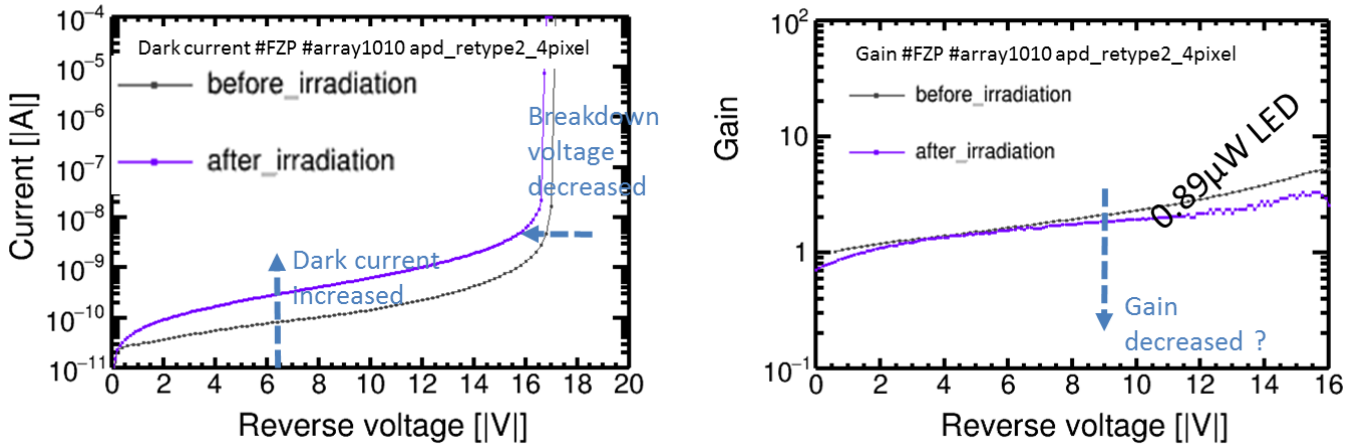


Figure 78 Change in dark current (left) and gain (right) before and after 200kGy irradiation in FZp based APTTEGh pixel

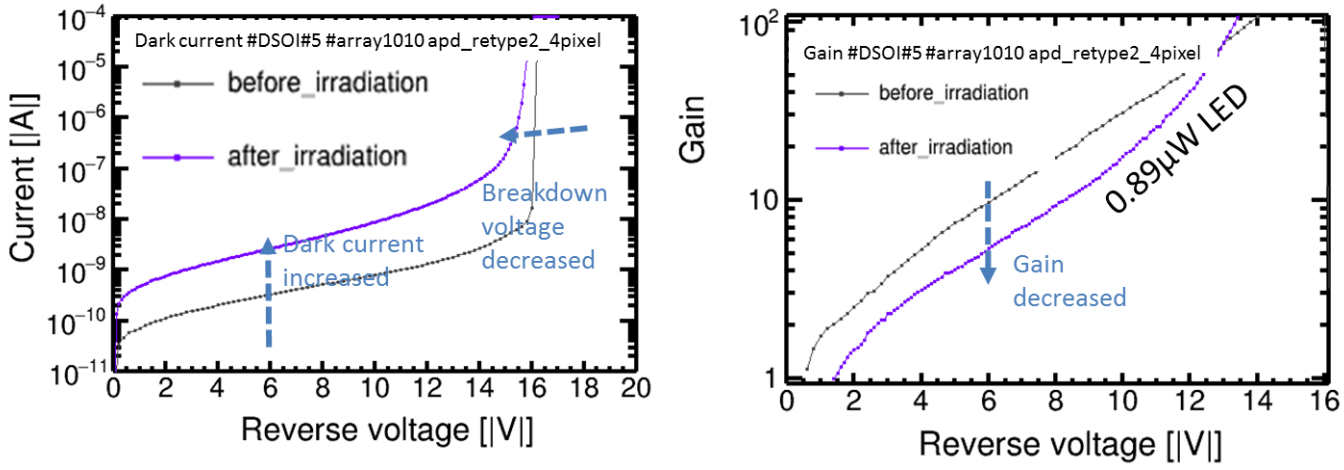


Figure 79 Change in dark current (left) and gain (right) before and after 1MGy irradiation in DSOI based APTTEGh pixel

Figures 76 to 79 show the graphs of change in dark current and gain measured before and after γ ray irradiation. It is clearly seen that dark current is increased across each sample which can be attributed to the increase in surface charge due to trapped holes. Breakdown voltage increased in samples of CZn and FZn wafers while decreased in case of FZp and DSOI wafers. Gain was observed in the SOIAPD samples even after irradiation but was decreased in value.

Chapter 5 Summary and Conclusion

Currently, novel photodetectors with high precision and sensitivity are being sought. A new type of Avalanche Photodiode (APD) designed and fabricated using SOI technology at KEK, Japan. This SOIAPD is expected to have high gain, response time and good S/N ratio as well as all other advantages of using SOI like small size, low energy consumption, greater radiation tolerance, etc.

SOIAPD test chip APDTEGh was used for evaluation. Of the four types of wafers (CZn, FZn, FZp, DSO) used to fabricate APDTEGh, all of them showed response as APDs. The dark current was measured to be very low (in order of 10^-14A) for single pixels of SOIAPD and 10^2 times as much for 10*10-pixel array. Similarly, in C-V curve measurements, capacitance of SOIAPD in APDTEGh was found to be as low as 3pF which is ideal for APD. In temperature dependence measurements, increase in dark current and breakdown voltages were observed with increase in temperature as expected. This phenomenon of increased dark current is supposed to appear due to higher production of electron hole pairs because of increased heat energy and shift in breakdown voltage I supposed to be due to collision of carriers before initiating avalanche mechanism with vibrating lattice suppressing impact ionization. Radiation hardness test of SOIAPD test samples showed that while dark current was observed to rise and breakdown voltages were shifted, internal gain was still available (although in reduced value and greater incosistancy) after γ-ray irradiation upto 1MGy.

Internal gain (multiplication factor from avalanche mechanism) as high as 100 times was achieved with the APDTEGh test chip. By identifying suitable voltage range for operation in linear multiplication mode SOIAPD could be used in future high performance detectors. Although the current SOIAPD was tested for its electrical characteristics by direct contact from parts in the sensor layer, the next step would be to integrate CMOS circuits like amplifier and shaper above the BOX layer to enhance the signals from sensor. Similary, introduction of Double-SOI with adjustable middle Si voltage could be used to enhance radiation hardness. In the future, SOIAPD can be expected to be developed for use as detectors in high energy physics experiments as well as various industrial applications.

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Appendix 1

TCAD source code.

```
<process simulator>
###############################################################################
### ====Variables=== ###
DP1=40
DP2=0.78 #PS 0.78
DP3=0.78 #NS 0.78
DW1=0.8  #0.81
DW2=3.72
DW3=2.22
xDL=0
Zmask=2.0
zSUB=100
rmax1=1e10
dxmin=0.1
dxmax=0.3
nx=1
dzmin=0.2
nz=3

##Direction
xDL=0
xWL=DP1
xP1L=xWL+DW1
xP1R=xP1L+DP2
xP2L=xP1R+DW2
xP2R=xP2L+DP3
xP3L=xP2R+DW3
xP3R=xP3L+DP3
xP4L=xP3R+DW3
xP4R=xP4L+DP3
```

```
xP5L=xP4R+DW3
xP5R=xP5L+DP3
xP6L=xP5R+DW2
xP6R=xP6L+DP2
xWR=xP6R+DW1
xDR=xWR+DP1

xC1=(xWL+xP1L)/2
xC2=(xP1L+xP1R)/2
xC3=(xP1R+xP2L)/2
xC4=(xP2L+xP2R)/2
xC5=(xP2R+xP3L)/2
xC6=(xP3L+xP3R)/2
xC7=(xP3R+xP4L)/2
xC8=(xP4L+xP4R)/2
xC9=(xP4R+xP5L)/2
xC10=(xP5L+xP5R)/2
xC11=(xP5R+xP6L)/2
xC12=(xP6L+xP6R)/2
xC13=(xP6R+xWR)/2

y01=0
y02=1.0
z01=-zSUB
z02=-10
z03=0
z04=z03+Zmask

grid.x.add(loc=xDL,  tag="xDL")
grid.x.add(loc=xWL, tag="xWL")
grid.x.add(loc=xC1, tag="xC1")
grid.x.add(loc=xP1L, tag="xP1L")
grid.x.add(loc=xC2, tag="xC2")
grid.x.add(loc=xP1R, tag="xP1R")
grid.x.add(loc=xC3, tag="xC3")
grid.x.add(loc=xP2L, tag="xP2L")
```

```
grid.x.add(loc=xC4, tag="xC4")
grid.x.add(loc=xP2R, tag="xP2R")
grid.x.add(loc=xC5, tag="xC5")
grid.x.add(loc=xP3L, tag="xP3L")
grid.x.add(loc=xC6, tag="xC6")
grid.x.add(loc=xP3R, tag="xP3R")
grid.x.add(loc=xC7, tag="xC7")
grid.x.add(loc=xP4L, tag="xP4L")
grid.x.add(loc=xC8, tag="xC8")
grid.x.add(loc=xP4R, tag="xP4R")
grid.x.add(loc=xC9, tag="xC9")
grid.x.add(loc=xP5L, tag="xP5L")
grid.x.add(loc=xC10, tag="xC10")
grid.x.add(loc=xP5R, tag="xP5R")
grid.x.add(loc=xC11, tag="xC11")
grid.x.add(loc=xP6L, tag="xP6L")
grid.x.add(loc=xC12, tag="xC12")
grid.x.add(loc=xP6R, tag="xP6R")
grid.x.add(loc=xC13, tag="xC13")
grid.x.add(loc=xWR, tag="xWR")
grid.x.add(loc=xDR,  tag="xDR")
grid.x.refine(from="xWL",to="xDL", start=dxmin,end=dxmax*20, rmax=rmax1)
grid.x.refine(from="xWL",to="xC1", start=dxmin,end=dxmax,rmax=rmax1)
grid.x.refine(from="xP1L",to="xC1",start=dxmin,end=dxmax,rmax=rmax1)
grid.x.refine(from="xP1R",to="xC2",start=dxmin,end=dxmax,rmax=rmax1)
grid.x.refine(from="xP1R",to="xC3",start=dxmin,end=dxmax,rmax=rmax1)
grid.x.refine(from="xP2L",to="xC3",start=dxmin,end=dxmax,rmax=rmax1)
grid.x.refine(from="xP2L",to="xC4",start=dxmin,end=dxmax,rmax=rmax1)
grid.x.refine(from="xP2R",to="xC4",start=dxmin,end=dxmax,rmax=rmax1)

grid.x.refine(from="xP2R",to="xC5",start=dxmin,end=dxmax,rmax=rmax1)
grid.x.refine(from="xP3L",to="xC5",start=dxmin,end=dxmax,rmax=rmax1)

grid.x.refine(from="xP3L",to="xC6",start=dxmin,end=dxmax,rmax=rmax1)
grid.x.refine(from="xP3R",to="xC6",start=dxmin,end=dxmax,rmax=rmax1)
grid.x.refine(from="xP3R",to="xC7",start=dxmin,end=dxmax,rmax=rmax1)
```

```
grid.x.refine(from="xP4L",to="xC7",start=dxmin,end=dxmax,rmax=rmax1)
grid.x.refine(from="xP4L",to="xC8",start=dxmin,end=dxmax,rmax=rmax1)
grid.x.refine(from="xP4R",to="xC8",start=dxmin,end=dxmax,rmax=rmax1)
grid.x.refine(from="xP4R",to="xC9",start=dxmin,end=dxmax,rmax=rmax1)
grid.x.refine(from="xP5L",to="xC9",start=dxmin,end=dxmax,rmax=rmax1)
grid.x.refine(from="xP5L",to="xC10",start=dxmin,end=dxmax,rmax=rmax1)
grid.x.refine(from="xP5R",to="xC10",start=dxmin,end=dxmax,rmax=rmax1)
grid.x.refine(from="xP5R",to="xC11",start=dxmin,end=dxmax,rmax=rmax1)
grid.x.refine(from="xP6L",to="xC11",start=dxmin,end=dxmax,rmax=rmax1)
grid.x.refine(from="xP6L",to="xC12",start=dxmin,end=dxmax,rmax=rmax1)
grid.x.refine(from="xP6R",to="xC12",start=dxmin,end=dxmax,rmax=rmax1)
grid.x.refine(from="xP6R",to="xC13",start=dxmin,end=dxmax,rmax=rmax1)
grid.x.refine(from="xWR", to="xC13",start=dxmin,end=dxmax,rmax=rmax1)
grid.x.refine(from="xWR",to="xDR", start=dxmin,end=dxmax*20, rmax=rmax1)
grid.y.add(loc=y01,tag="y01")
grid.y.add(loc=y02,tag="y02")
grid.z.add(loc=z01,tag="z01")
grid.z.add(loc=z02,tag="z02")
grid.z.add(loc=z03,tag="z03")
grid.z.add(loc=z04,tag="z04")
grid.z.refine(from="z02",to="z01",start=0.5,end=(z02-z01)/(4*nz),rmax=rmax1)
grid.z.refine(from="z03",to="z02",start=dxmin,end=0.5,rmax=rmax1)
grid.z.refine(from="z03",to="z04",num=Zmask/nz)



#---SUB--##
region.substrate(
xmin="xDL",xmax="xDR",
ymin="y01",ymax="y02",
zmin="z01",zmax="z03",
orient="100",imp="P",conc=2.16e12)
init_sypros()
save.sgraph("00_mesh.sg2",posy="min")
oxi_ctrl.set(force_oxidation=true)

#--WELL(BP2+BP3+BPW)##
```

```
deposit(mat="resist",model="planar",thick_from_top=5.0)
WELL=[[xWL,y01],[xWR,y01],[xWR,y02],[xWL,y02]]
etch(mat="resist",thick=5.0,mask_pattern=WELL,mask_type="nega")
deposit(mat="SiO2",thick=0.248)
implant(ion="B",energy=500,dose=1.0e12)
implant(ion="B",energy=220,dose=1.0e12)
implant(ion="B",energy=100,dose=1.0e12)
etch(mat="SiO2",model="remove_all")
etch(mat="resist",model="remove_all")
save.sgraph("01_well.sg2",posy="min")

#--PIX--##
P1=[[xP1L,y01],[xP1R,y01],[xP1R,y02],[xP1L,y02]]
P2=[[xP2L,y01],[xP2R,y01],[xP2R,y02],[xP2L,y02]]
P3=[[xP3L,y01],[xP3R,y01],[xP3R,y02],[xP3L,y02]]
P4=[[xP4L,y01],[xP4R,y01],[xP4R,y02],[xP4L,y02]]
P5=[[xP5L,y01],[xP5R,y01],[xP5R,y02],[xP5L,y02]]
P6=[[xP6L,y01],[xP6R,y01],[xP6R,y02],[xP6L,y02]]

deposit(mat="resist",model="planar",thick_from_top=5.0)
etch(mat="resist",thick=5.0,mask_pattern=[P2,P3,P4,P5],mask_type="nega")
implant(ion="P",energy=30,dose=5.0e15)
etch(mat="resist",model="remove_all")
deposit(mat="resist",model="planar",thick_from_top=5.0)
etch(mat="resist",thick=5.0,mask_pattern=[P1,P6],mask_type="nega")
implant(ion="B",energy=40,dose=5.0e15)
etch(mat="resist",model="remove_all")
save.sgraph("02_PIX.sg2",posy="min")

#--DIFF--##
diffuse(amb="nitrogen",temp=1050,time=10/60)
save.sgraph("04_diff.sg2",posy="min")
#####output_file######
save.sgraph ( file = "profile.sg2",posy="min")
save.deleos ( file = "profile.geo", x =500, y =0.5)
save.deleos ( file = "profile_2D.geo", posy = "min")
```

```
#print1d(value = "field_data",field="B_ac",file="profile_B_ac",x="xC2",y=0.0)

#print1d(value = "field_data",field="P_ac",file="profile__P_ac",x="xC2",y=0.0)

#####finish#####

end_sypros()
```

<structure simulation>

```
#!variable
profile="profile_2D.geo"
Width=1.0

DP1=40
DP2=0.78 #PS 0.78
DP3=0.78 #NS 0.78
DW1=0.8  #0.81
DW2=3.72
DW3=2.22
zSUB=100
xDL=0
xWL=DP1
xP1L=xWL+DW1
xP1R=xP1L+DP2
xP2L=xP1R+DW2
xP2R=xP2L+DP3
xP3L=xP2R+DW3
xP3R=xP3L+DP3
xP4L=xP3R+DW3
xP4R=xP4L+DP3
xP5L=xP4R+DW3
xP5R=xP5L+DP3
xP6L=xP5R+DW2
xP6R=xP6L+DP2
xWR=xP6R+DW1
xDR=xWR+DP1

#!structure
dimension(dimension=2,width=Width)
mesh(file_name=profile)
region(material="all",file_name=profile)
doping(type="B",file_name=profile)
doping(type="P",file_name=profile)
electrode(name="Back",x_min=0,x_max=xDR,y_min=-zSUB-0.1,y_max=-zSUB)
electrode(name="P1",   x_min=xP1L,x_max=xP1R,y_min=0,y_max=0.1)
electrode(name="P2",   x_min=xP2L,x_max=xP2R,y_min=0,y_max=0.1)
electrode(name="P3",   x_min=xP3L,x_max=xP3R,y_min=0,y_max=0.1)
electrode(name="P4",   x_min=xP4L,x_max=xP4R,y_min=0,y_max=0.1)
electrode(name="P5",   x_min=xP5L,x_max=xP5R,y_min=0,y_max=0.1)
electrode(name="P6",   x_min=xP6L,x_max=xP6R,y_min=0,y_max=0.1)
outfile ( dst = "profile.dst", sgn = "profile.sgd", )
structure ( )
```

<Device simulator>

```
#####variables####
bias_start = 0.0
bias_end = -22
bias_step = 0.5
dc_temp=300
dc_reset=10

#!analysis
```

```
set_method(damp=ON)
set_method(mtx_solver=SUPERNODAL)
set_method(ej_mob=false)
set_method(ej_others=true)
set_method(minpsi=1.0,minele=1e18,minhol=1e18)
set_method(errpsi=1e-2,errele=1e-1,errhol=1e-1)
set_method(conv_cond=CONV_EQUATION_AND_CURRENT,errbdc=1e-2,resbdc=1e-2)
initial_guess("Linear")
set_mobility(lattice=ON,coulomb=MASETTI,surface=OFF,vsat=SCHARFETTER)
set_grrate(srh=ON,aug=ON,ii=ON,btbt=ON,sur=OFF)
set_quantum(model=OFF)
set_output(cur_filename="iv.cur")
set_output(dis_filename="iv.dis",
dis_out=ALL,
dis_vars=[Psi,E,Hole,Elec,II,SRH,Jn,Jp])
set_bias(name="P2",0)
set_bias(name="P3",link="P2")
set_bias(name="P4",link="P2")
set_bias(name="P5",link="P2")
set_bias(name="P1",v0 = bias_start, v1 = bias_end, dv = bias_step,)
set_bias(name="P6",link="P1")
run_dc(temp=dc_temp,reset=dc_reset,cont=true)
ds_exit()
```

Appendix 2

Carrier generation/recombination models

Carrier generation/recombination U can be expressed using Shockley-Read-Hall's generation/recombination term U_{SRH}, surface recombination term U_{SUR}, Inter-band tunneling term U_{BTBT}, Auger recombination term U_{AUG} and Impact Ionization term U_{IMPACT} as follows:

$$U = U_{SRH} + U_{SUR} + U_{BTBT} + U_{AUG} + U_{IMPACT}$$

Surface recombination model and impact ionization model can be expressed below:

1. Surface recombination model,

$$U_{SUR} = \frac{n_i^2 - pn}{\frac{n+n_i}{s_p} + \frac{p+n_i}{s_n}} \delta(y)$$

n_i: intrinsic carrier density
n, p: electron or proton density
N: impurity concentration (donor and acceptor)
s_n,s_p: model parameter

2. Impact ionization model

$$\alpha_n = \alpha_{n0}[1 + \beta_{n0}(T_L - T_{L0}) \exp\left[\frac{E_{n0}(1 + \beta_{n1}(T_L - T_{L0}))}{|\boldsymbol{E}_n|}\right]$$

$$\alpha_p = \alpha_{p0}[1 + \beta_{p0}(T_L - T_{L0}) \exp\left[\frac{E_{p0}(1 + \beta_{p1}(T_L - T_{L0}))}{|\boldsymbol{E}_p|}\right]$$

$$|\boldsymbol{E}_n| = \frac{|\boldsymbol{J}_n \bullet \boldsymbol{E}_n|}{|\boldsymbol{J}_n|}$$

$$|\boldsymbol{E}_p| = \frac{|\boldsymbol{J}_p \bullet \boldsymbol{E}_p|}{|\boldsymbol{J}_p|}$$

T_L: lattice temperature
T_{L0}: surrounding temperature
J_n, J_p: electron/hole current vector
A_{n0}, β_{n0}, E_{n0}, β_{n1}: model parameters (electrons)
A_{p0}, β_{p0}, E_{p0}, β_{p1}: model parameters (holes)