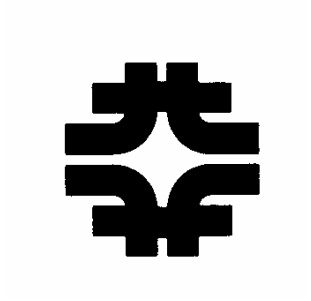


Future Pixel Detectors

Fermilab 3D and SOI Technology Developments

KEK
June 25, 2007

Marcel Demarteau
For the Fermilab Detector & Physics R&D Group

Tsukuba, Japan
June 25, 2007

Vertex Detectors

- **Vertex Pixel detectors are very difficult**
  - **Good angular coverage with many layers close to the interaction point**
  - **Excellent point resolution (< 4 μm)**
  - **Superb impact parameter resolution (5μm ⊕ 10μm/(p $\sin^{3/2}\theta$))**
  - **Transparency (~0.1% X_0 per layer)**
  - **Robust pattern recognition (track finding in vertex detector alone)**
  - **Integration over small number of bunch crossings for ILC**
    - <150 = ~50 μs
  - **Electromagnetic Interference (EMI) immunity**
  - **Power Constraint (< ~100 Watts) with gas cooling**
  - **Radiation hard for LHC experiments**

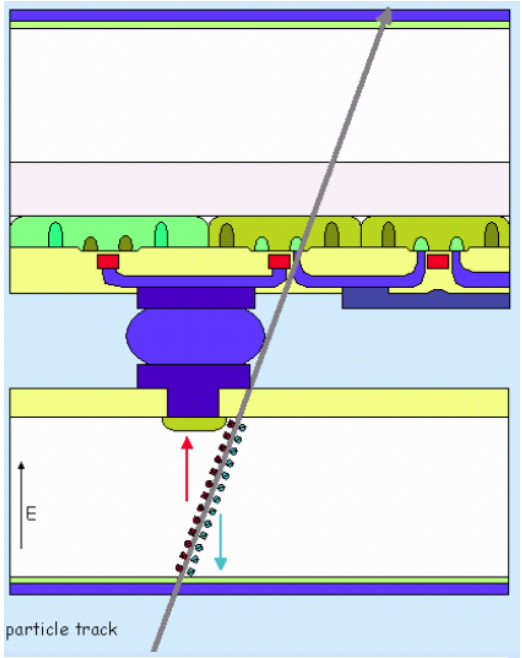
- **The physics drives the design of HEP pixel electronics and detectors to ever more stringent requirements in all these areas**

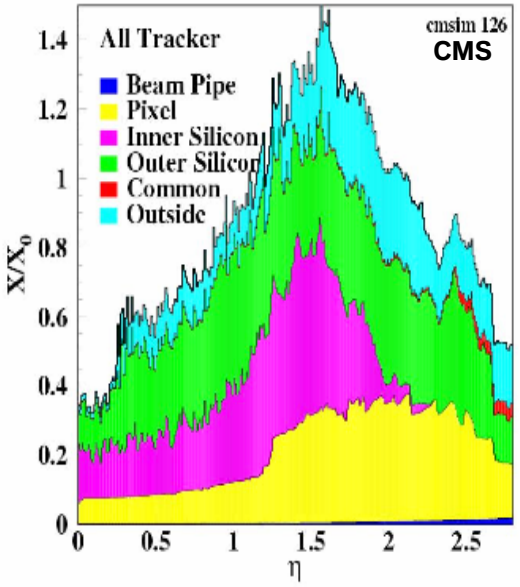
- **As an example, a pixel detector for the LHC and ILC**

LHC Pixel Detectors

- **All LHC pixel detectors are hybrid pixel detectors: Separate detector and readout chip, connected by bump bonds**
  - **sensor and read-out chip (roc) can be optimized separately**

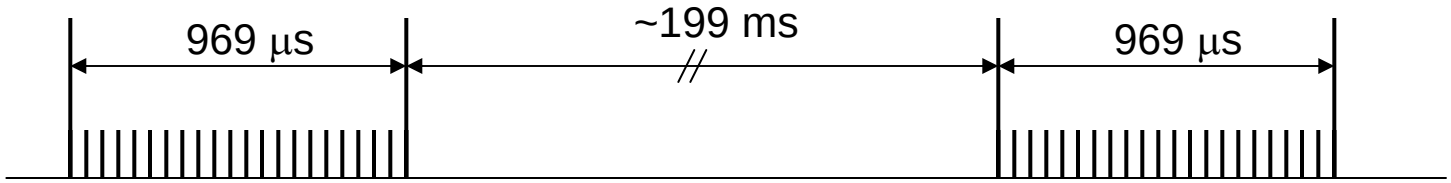
- **Issues with this technology:**
  - **At least twice the mass of the detector since the readout chip is as thick as the silicon sensor**
  - **Power consumption in the chip is high**
  - **Need active cooling of detectors**
  - **Bump bonding is very expensive**
  - **Pixel size is too large**
    - CMS pixel size is 100x150μm^2 = 15,000 μm^2
    - Atlas pixel size is 50x400μm^2 = 20,000 μm^2
    - ILC need ~ 20x20μm^2 = 400 μm^2
    - Area LHC/ILC = 50





ILC Pixel Detectors

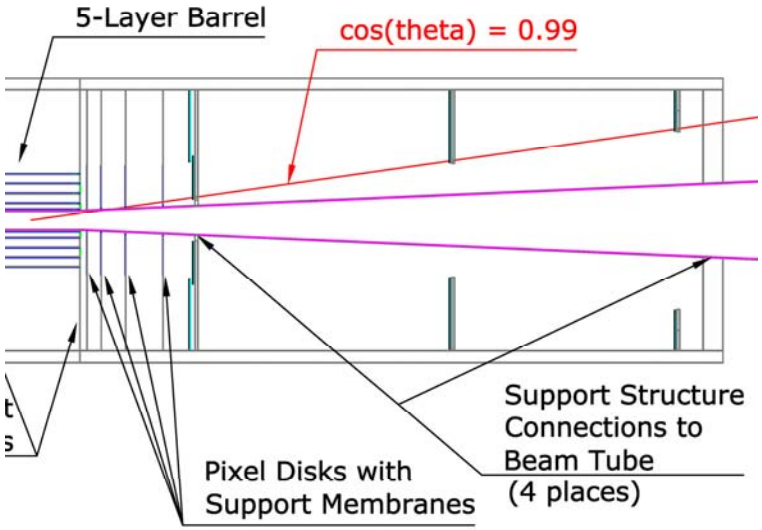
- **Vertex detector requirements**
  - **Very low mass: 0.1% X_0 per layer (equivalent of 100 μm of Si)**
    - Low mass requires no active cooling, hence low power
  - **High resolution: impact parameter resolution of ~ 5 μm**
    - Requires smaller pixels which increases the readout circuit density
  - **Good and robust pattern recognition, integrated design**
    - Low occupancies, bunch crossing time stamp
  - **Modest radiation tolerance for ILC applications**

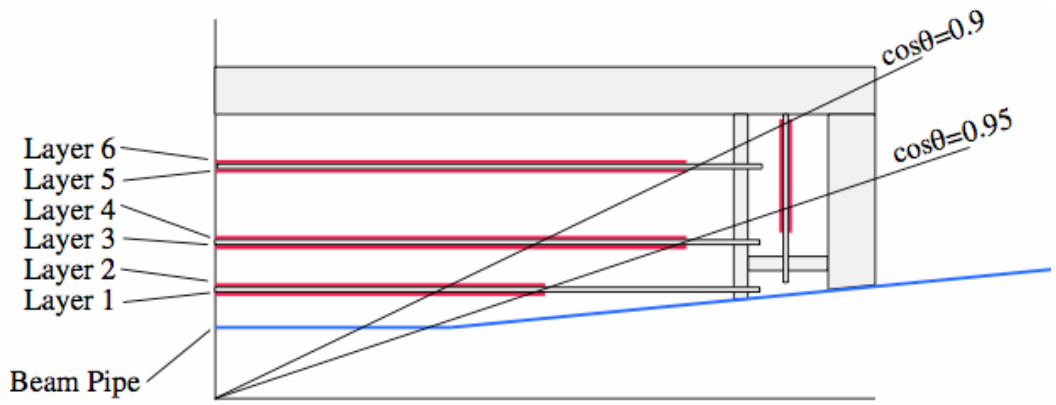


- **ILC beam structure**
  - **Five trains of 2625 bunches per second**
  - **Bunch separation of 369.2 ns**
- **ILC Maximum hit occupancy**
  - **Assumed to be 0.03 particles/crossing/mm²**
  - **Assume 3 pixels hit/particle (obviously this depends somewhat on pixel size, hit location, and charge spreading)**
  - **Hit rate = 0.03 part./bx/mm² x 3 hits/part. x 2625 bx/train gives 252 hits/train/mm²**

ILC Detector Geometry

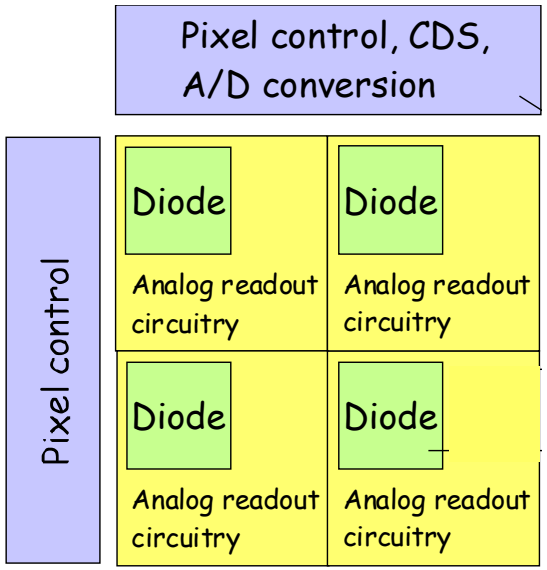
- At an e^+e^- linear collider there is a premium on the small angle region
  - more events are in the forward/backward regions than in the central regions
- Detector configurations
  - Short barrels with disks
    - Barrels: five layers, Longitudinal coverage: ± 62.5 mm, Radial coverage: 14<R<61 mm
    - Disks: Four disks, z = ± 72, ± 92, ± 123, ± 172 mm, Radial coverage: R<71 mm
  - Long barrels, limited disk coverage
- Extraction of signals, power distribution, cable plant non-trivial





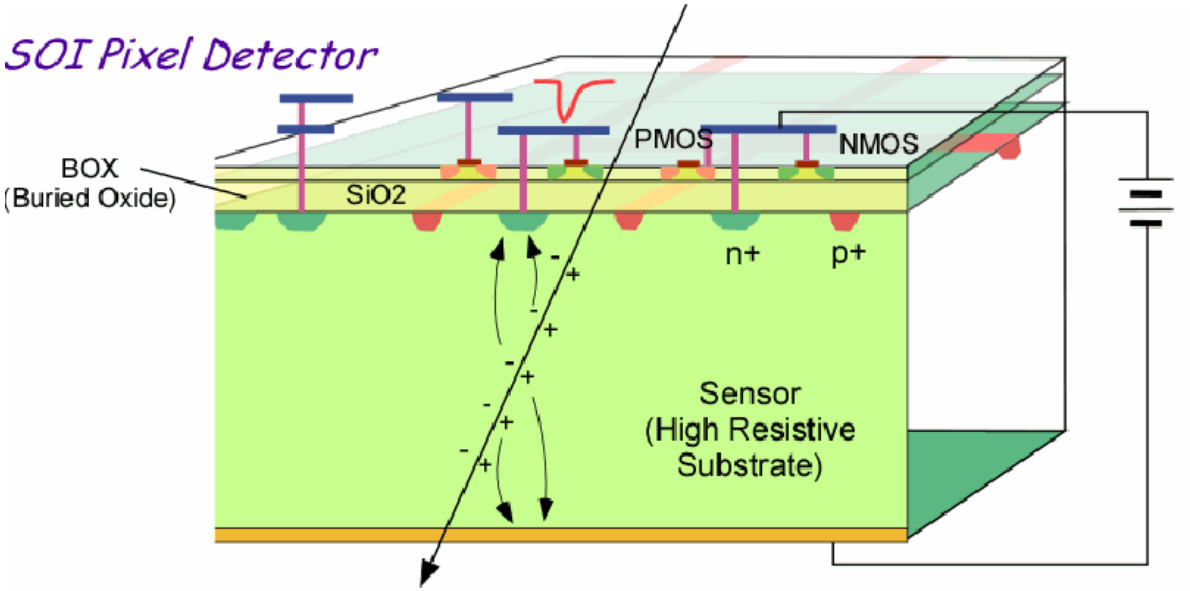
Pixel Detectors

- **As mentioned, pixel detectors are very difficult**
  - **Many competing requirements**
  - **All projects will benefit from advances in any area**
  - **New technologies are applicable to many areas of science**
- **Significant progress has been made to address these issues by integrating sensors and front end electronics within the pixel cell: Monolithic Active Pixel Sensors (MAPS)**
  - **Fundamental limitations**
    - Small signal dependent on epi thickness
    - Most designs are limited to NMOS transistors
    - Not 100% fill factor
    - Slow rise time set by diffusion
- **Fermilab is pursuing alternatives:**
  - **SOI (Silicon On Insulator) Pixel Sensors**
    - Offers improvements over MAPS
  - **3D integrated circuits**
    - Also SOI process, but offers improved performance over SOI pixel sensors.



Conventional MAPS 4 Pixel Layout

SOI Detector Concept



Advantages

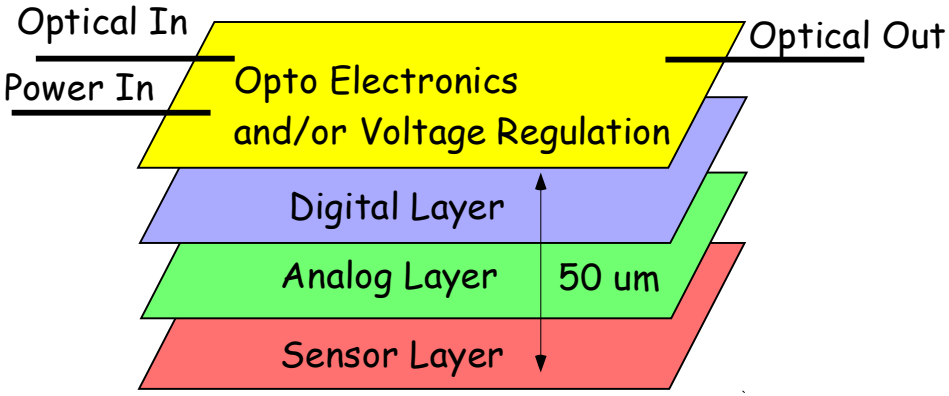
- 100% fill factor
- Large and fast signal
- Small active volume: high soft error immunity
- Full di-electric isolation: latchup free
- Low Junction Capacitance: high speed, low power

- **Bonded Wafer: low resistive top layer + high resistive substrate, separated through a Buried OXide (BOX) layer**
  - **Top layer: standard CMOS Electronics (NMOS, PMOS, etc. can be used)**
  - **Bottom substrate layer forms detector volume**
  - **The diode implants are formed beneath the BOX and connected by vias**
- **Monolithic detector, no bump bonds (lower cost, thin device)**
- **High density and smaller pixel size is possible**
- **Small capacitance of the sense node (high gain V=Q/C)**
- **Industrial standard technology (cost benefit and scalability)**

Vertical Scale Integrated Circuits (3D)

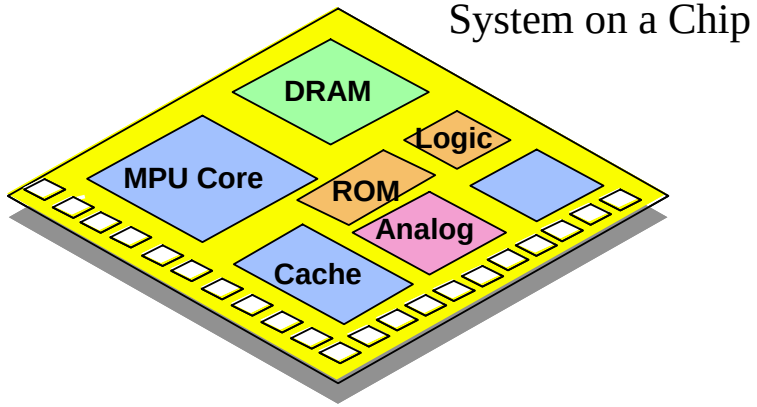
- SOI detector technology offers several advantages over MAPS; 3D offers advantages over SOI detectors

- A 3D device is a chip comprised of 2 or more layers of semiconductor devices which have been thinned, bonded, and interconnected to form a monolithic circuit



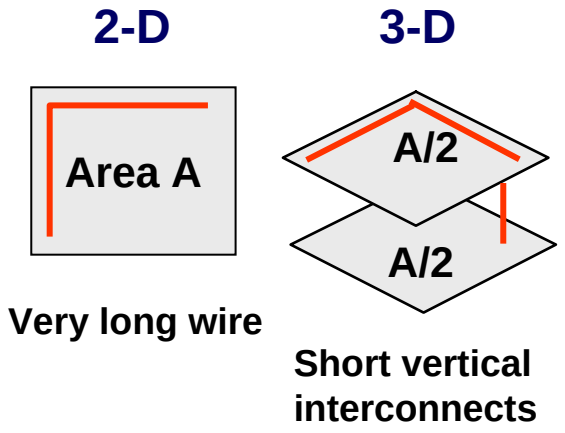
- Advantages of 3D over SOI
  - Increased circuit density due to multiple tiers of electronics
  - Independent control of substrate materials for each of the tiers.
  - Ability to mate various technologies in a monolithic assembly

- Technology driven by industry
  - Circuit performance limited by interconnects
    - Stacked, wirebonded asics
  - Desire to limit area of active elements
  - Provide increased functionality
  - Reduce interconnect power, crosstalk

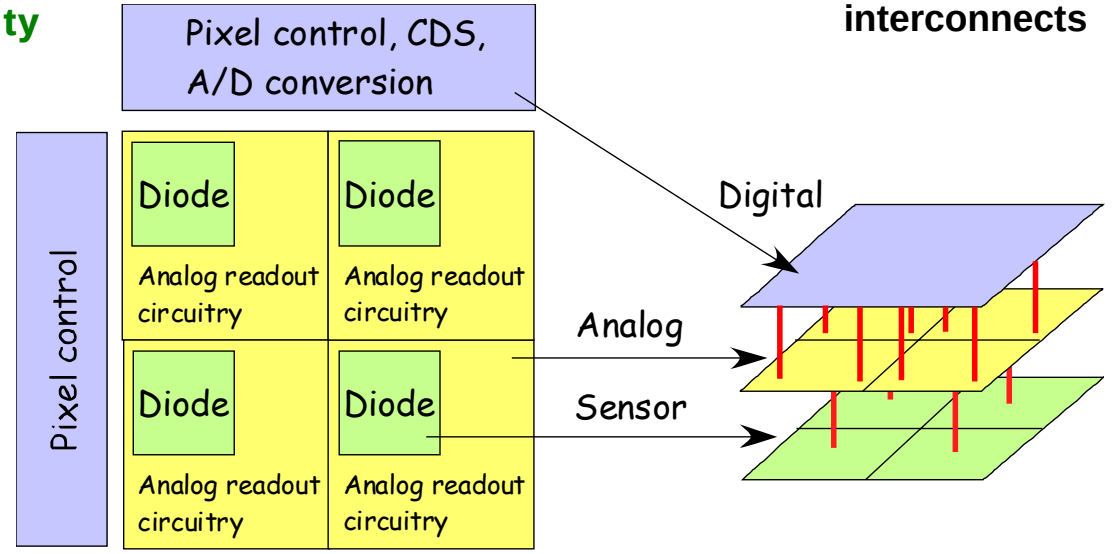


Benefits of Vertical Integration

- **Many benefits of 3D integration – also for HEP applications**
  - **Integration of heterogeneous technologies possible**
  - **IC fabrication optimized for each functionality reducing cost & increasing yield**
    - Process optimization for each layer (also called tier)
  - **Replaces long horizontal traces with short vertical interconnects**
  - **Interconnect length decreases therefore R, L, C decreases for higher speed**
  - **Reduce interconnect power, crosstalk**
  - **Power, delay and noise reduction**
  - **Reduce chip I/O pads**
  - **Provide increased functionality**



- **Benefits of pixellated arrays**
  - **Massively parallel signal processing**
  - **Dramatically increased electronic functionality in each pixel**



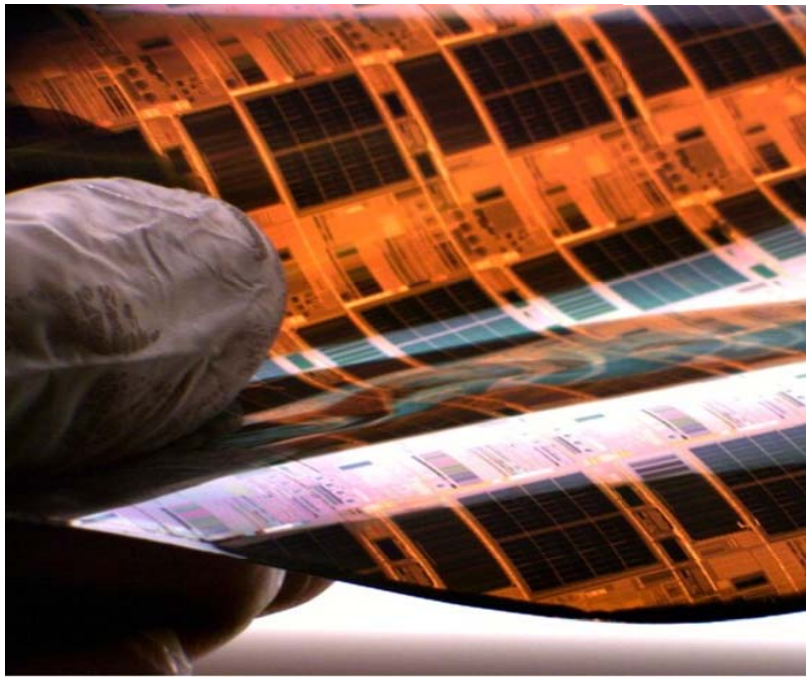
Key Technologies for 3D

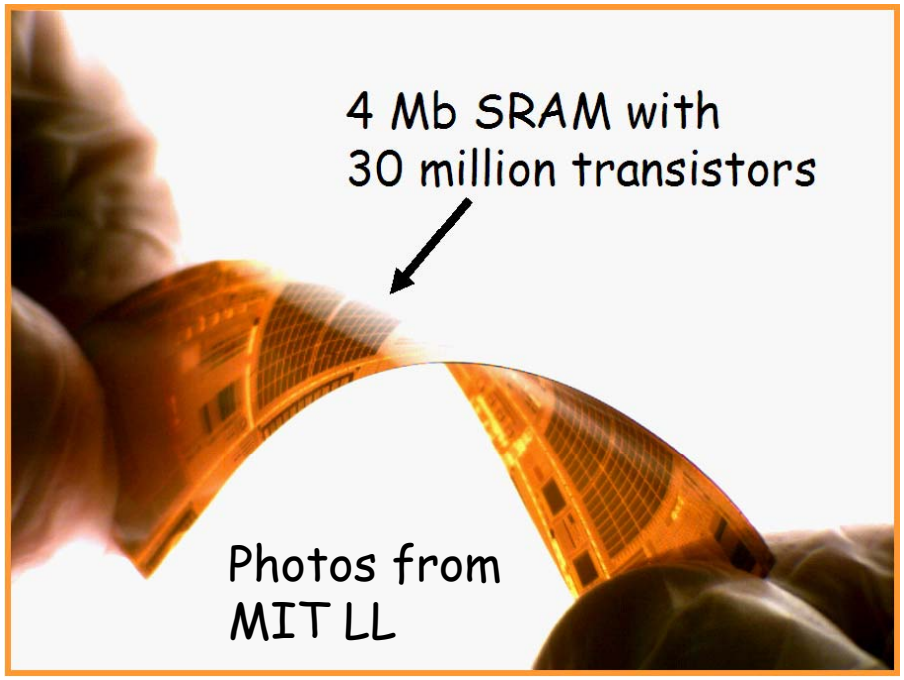
- **There are 4 key technologies for vertical scale integration**
  - **Wafer thinning**
    - Target thickness < 30 µm
    - Thickness tolerance = ± 1 µm
    - Temporary carrier mounting/demounting and thin die singulation without damage to ICs
  - **Through-wafer via formation and metallization**
    - High aspect ratio 3-D interconnects through SiO_2 and Si
    - Interconnects need to be insulated
  - **High precision alignment**
    - Uniform alignment < ±1 µm
  - **Bonding between layers**
    - Multiple techniques being employed

- **Many of these technologies are also used in the development of SOI detectors**

Key Technology: Wafer Thinning

- For compact, low mass devices, layers to be thinned as much as possible
- Through-wafer vias typically have an 8 to 1 aspect ratio. In order to keep the area associated with the via as small as possible, the wafers should be thinned as much as possible
- Thinning is typically done by a combination of grinding, lapping, and chemical or plasma etching



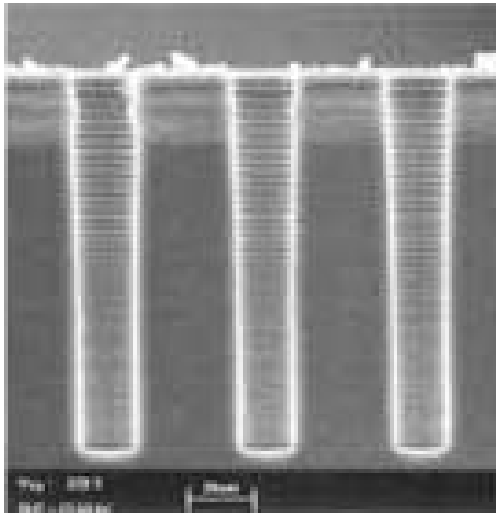


Six inch wafer thinned to 6 microns and mounted to 3 mil kapton.

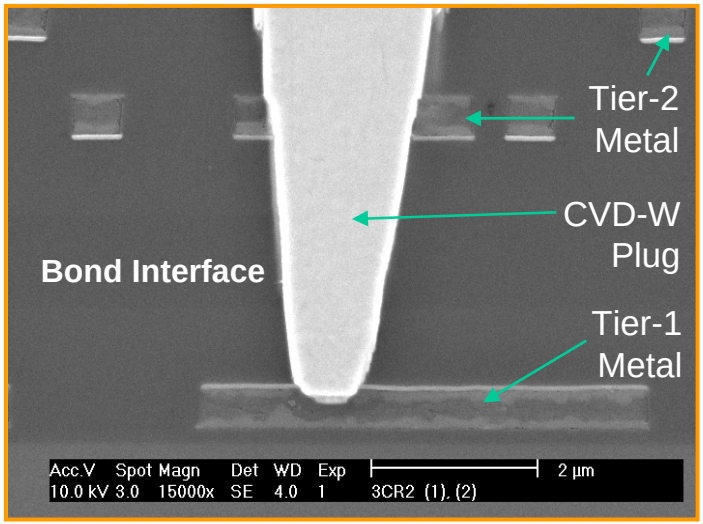
Key Technology: Via Formation and Metallization

- **Two different procedures are generally followed: Via First or Via Last**
  - **Via First: via hole creation and via metallization takes place on a wafer before wafer bonding**
  - **Via Last: via hole creation and via metallization takes place on a wafer after wafer bonding**
- **Vias in CMOS are formed using the Bosch process and are passivated before filling with metal, while vias in SOI are formed using a plasma oxide etch and are filled without passivation**

SEM of 3 vias using Bosch process



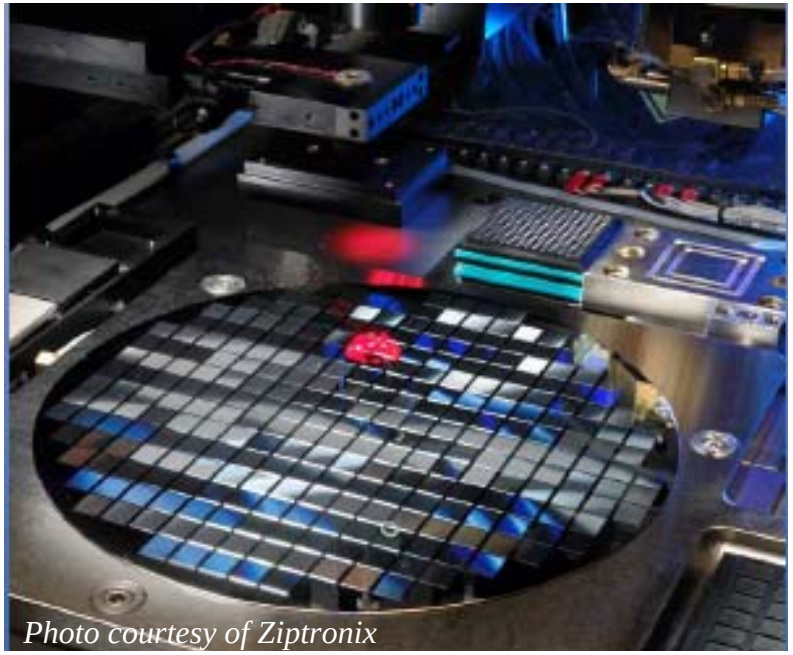
Via using oxide etch process (Lincoln Labs)



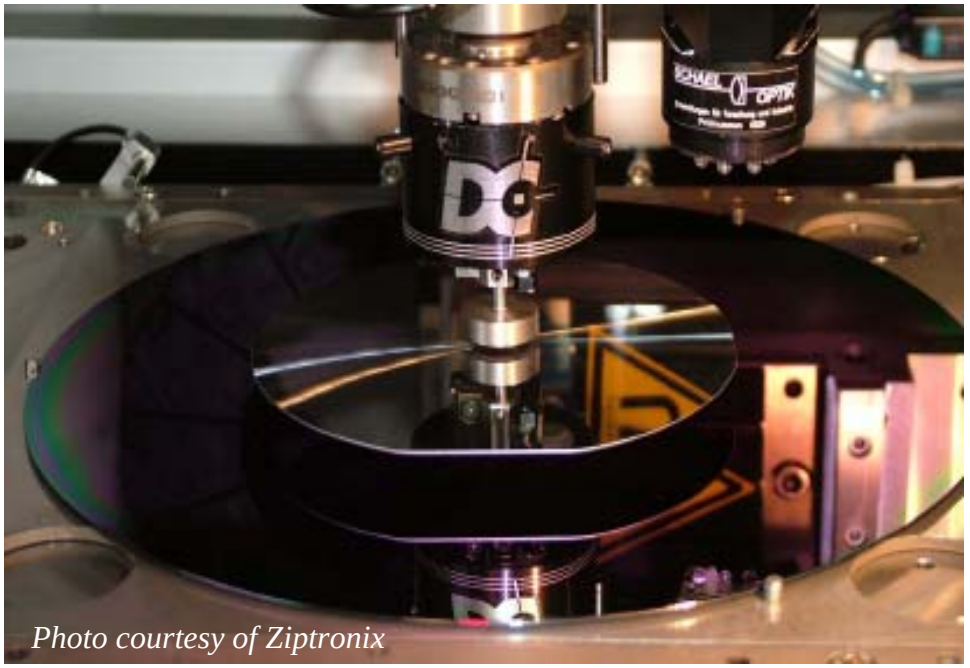
Typical diameters are 1-2 microns

Key Technology: Wafer Alignment

- **Alignment of die-to-wafer (D2W) or wafer-to-wafer (W2W) is generally better than 1 μm**
  - **MIT-LL 0.5 μm 3-sigma overlay demonstrated**



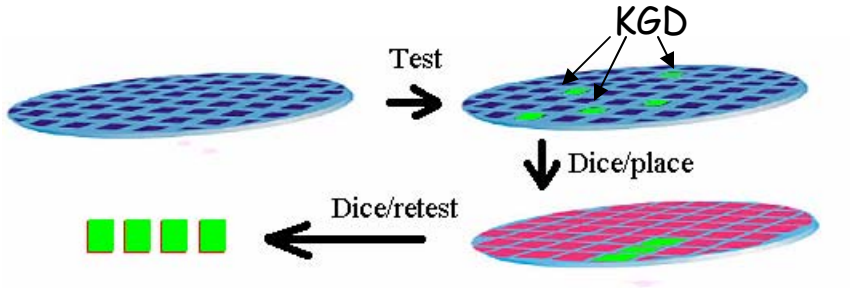
Die to Wafer alignment and placement



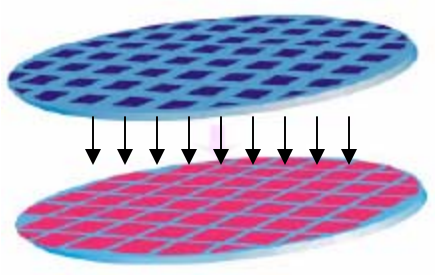
Wafer to Wafer alignment and placement

Key Technology: Wafer Bonding

- **Two approaches being followed:**
- **Die-to-Wafer (D2W) Bonding**
  - **Lower throughput**
  - **Can handle multiple die sizes**
  - **known good die (KGD) methods**
  - **Easier to stack mixed technologies and/or materials**
  - **Lower development cost**
  - **die-to-die process can further reduce development costs**
- **Wafer-to-Wafer (W2W) Bonding**
  - **High throughput**
  - **Compound yield loss**
  - **Wafer size must match**
  - **Die size must match**
  - **Larger development costs**



Die to wafer bonding

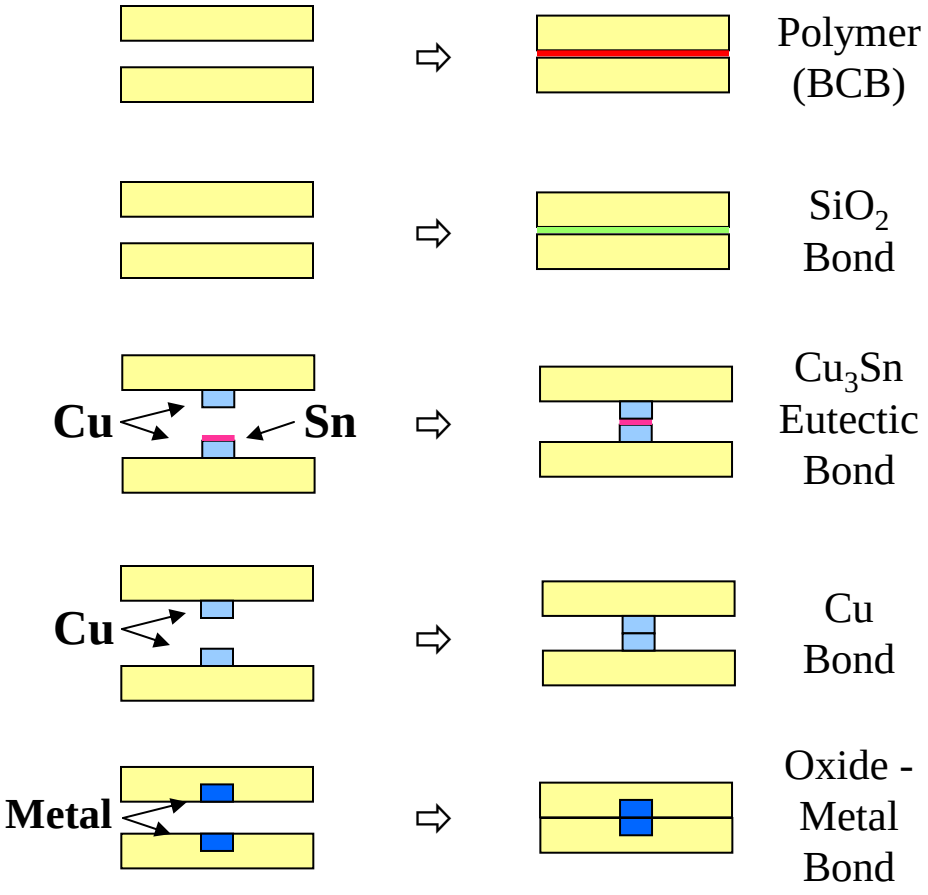


⇨ Dice/test

Wafer to wafer bonding

Key Technology: Wafer Bonding

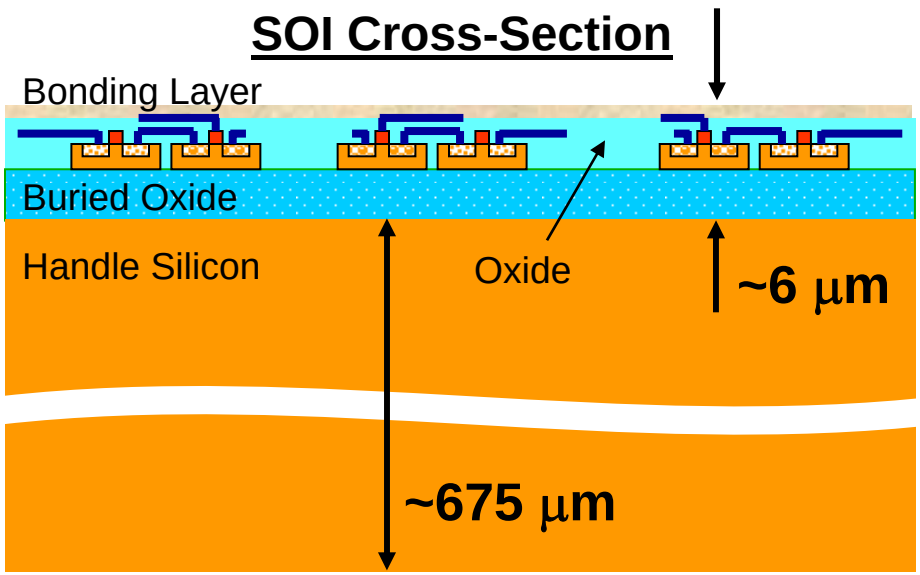
- **Bonding techniques between die/wafer and wafer**
  - **Adhesive bond**
  - **Oxide Bond: SiO_2 to SiO_2**
  - **Cu Sn Eutectic**
  - **Cu Thermocompression**
  - **Direct Bond Interconnect (DBI)**



- **Electrical connections are formed after the bonding process for the first two processes; for the last three processes, the electrical and mechanical connections are made at the same time**

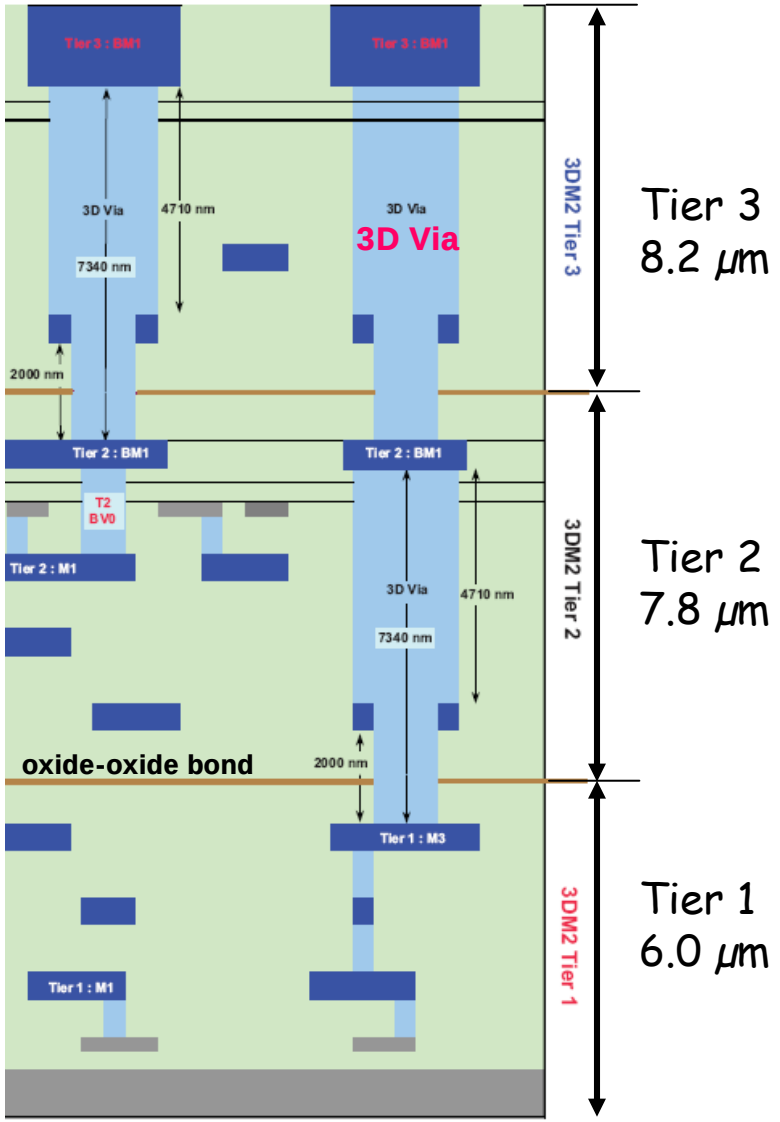
Advantages of SOI for 3D

- The electrically active portion of an integrated circuit wafer is < 1% of the total wafer thickness
- Buried oxide layer in SOI provides ideal etch stop for wafer thinning operation prior to 3D integration
- Full oxide isolation between transistors allows direct 3D via formation without the added complexity of a via isolation layer
- SOI's enhanced low-power operation (compared to bulk CMOS) reduces circuit stack heat load



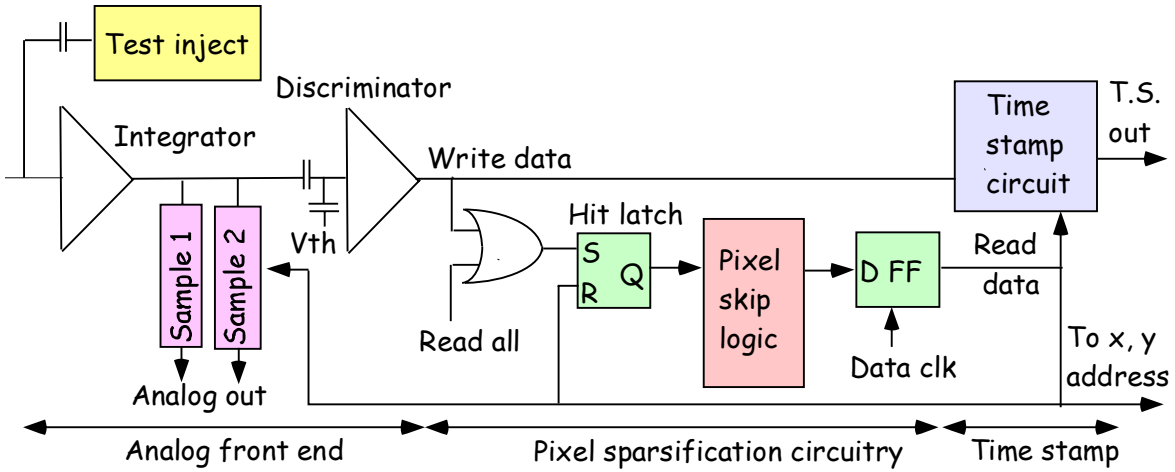
Development of a 3D Demo Chip

- MIT Lincoln Laboratories (MIT-LL) has developed the technology that enables 3D integration
  - Demonstrated the 3D technology through fabrication of imaging devices
  - Has infrastructure to allow for 3D Multi-Project Run fabrication
- We were invited to participate in the MIT-LL three-tier multi-project run
  - 3D design to be laid out in MIT-LL 0.18 μm SOI process
    - SOI provides additional advantages: BOX, full isolation, direct via formation, enhanced low-power operation
  - 3 levels of metal in each layer
- Submission deadline was Oct. 15, 2006
- Requested wafer space of ~ 2.5 x 2.5 mm^2
- Pixel size 20 x 20 μm; 64 x 64 pixel array
- No integrated sensor
- Chip to be received sometime in fall



Architecture of Demonstrator Chip

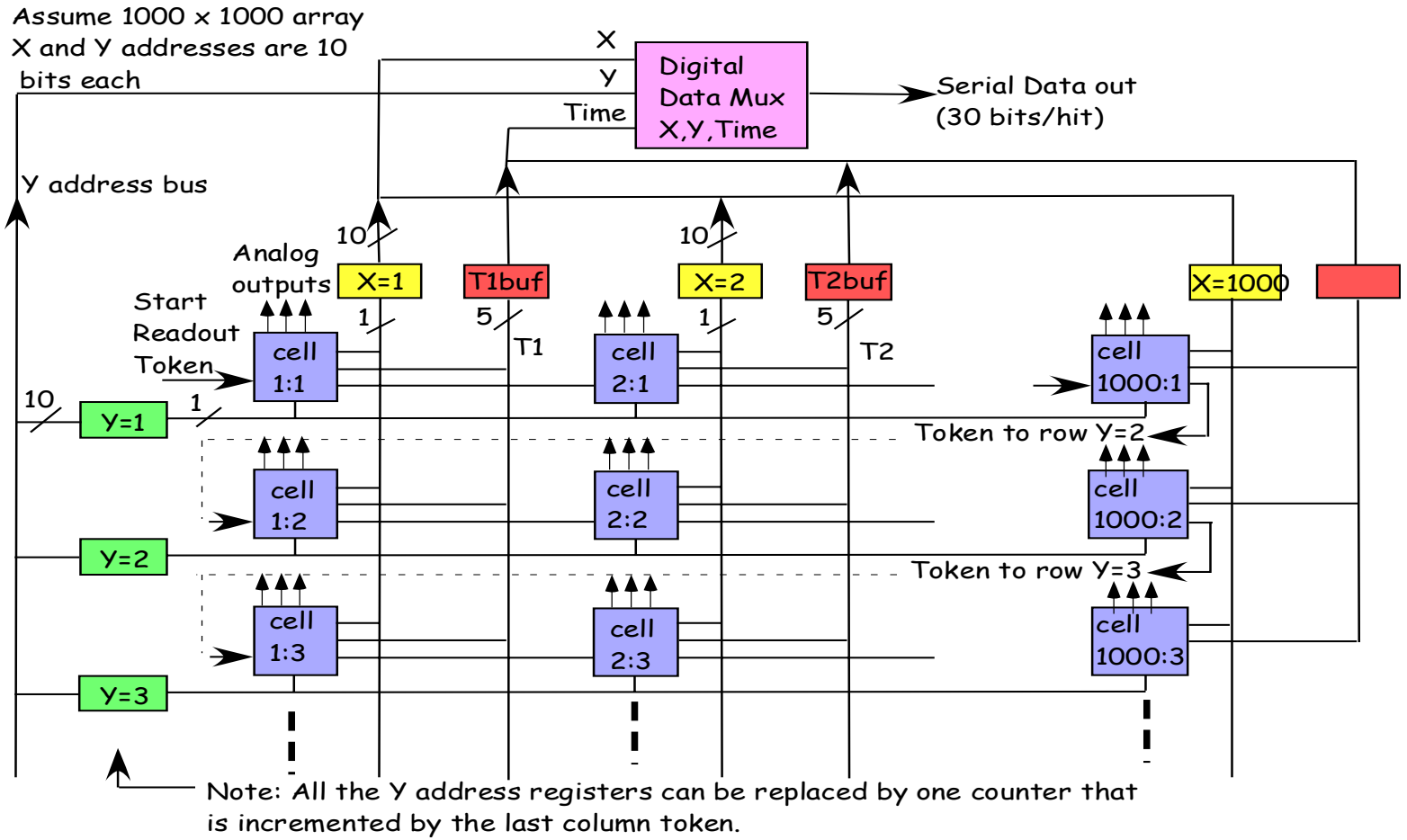
- **Design:**
  - **Provide analog and binary readout information**
  - **Time stamping of pixel hit for ILC environment**
    - Divide bunch train into 32 time slices; each hit pixel can store one time stamp equivalent to 5 bits of time information
  - **Sparsification to reduce data rate**
    - Use token passing scheme with look-ahead to reduce data output
      - During acquisition, a hit sets a latch
      - Sparse readout performed row by row with x- and y-address stored at end of row and column
  - **Chip divided into 3 tiers**
    - Pixels as small as possible but with significant functionality.
    - Design for 1000 x 1000 array but layout only for 64 x 64 array.



Schematic pixel cell block diagram

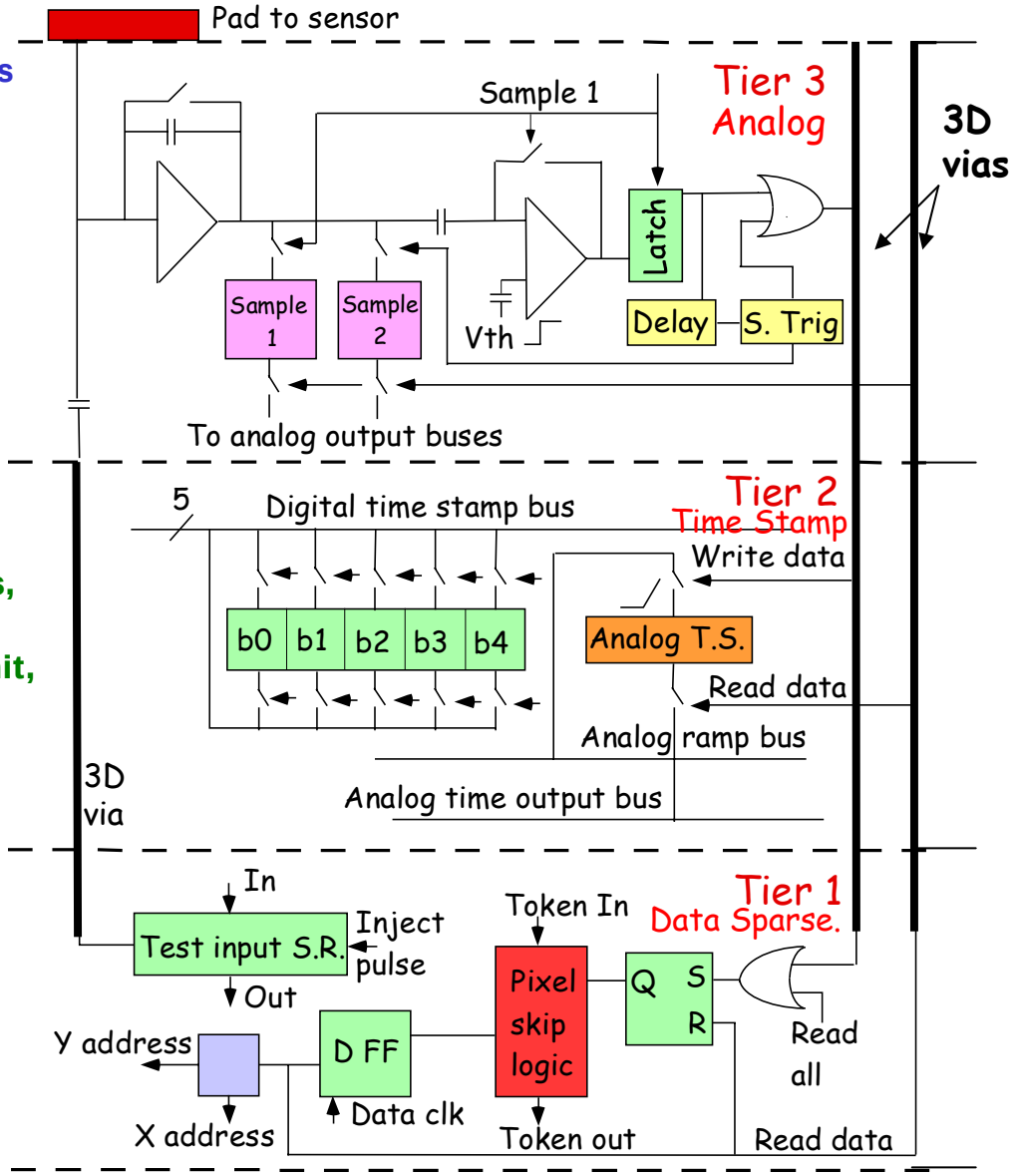
Pixel Readout Scheme

- Pixel being read points to the x address and y address stored on the perimeter.
- At same time, time stamp information and analog pulse height is read out
- During pixel readout, token scans ahead for the next hit pixel (200 ps/cell)



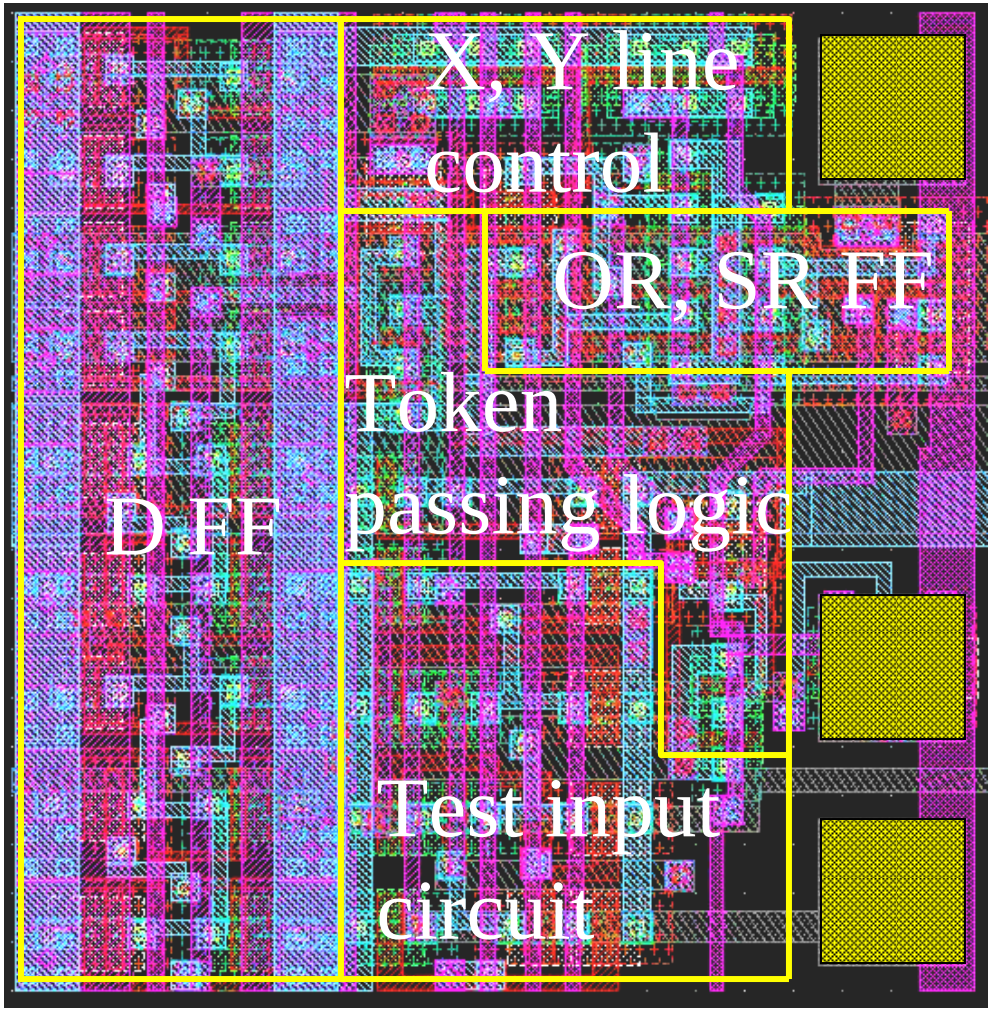
3D Three Tier Pixel Layout

- **Readout speed for an ILC environment**
- **Assume 1k x 1k array with 20 x 20 μm² pixels**
  - **First pixel in each row always read out**
    - Adds 1000 cells, small increase in data volume
  - **Time to scan 1 row:**
    200 ps x 1000 = 200 ns
  - **Time to readout cell**
    30 bits x 20 ns/bit = 600 ns
  - **Plenty of time to find next hit pixel during readout**
- **Assume maximum number of hits/chip of 250 hits/mm²**
  - **For a 1000 x 1000 array of 20 μm pixels, 100k hits/chip**
  - **For 50 MHz readout clock and 30 bits/hit, readout time:**
    100,000 hits x 30 bits/hit x
    20 ns/bit = 60 msec.
- **Readout time is far less than the ILC allowed 200 msec. Thus the readout clock can be even slower or several chips can be put on the same bus. Readout time is even less for smaller chips**



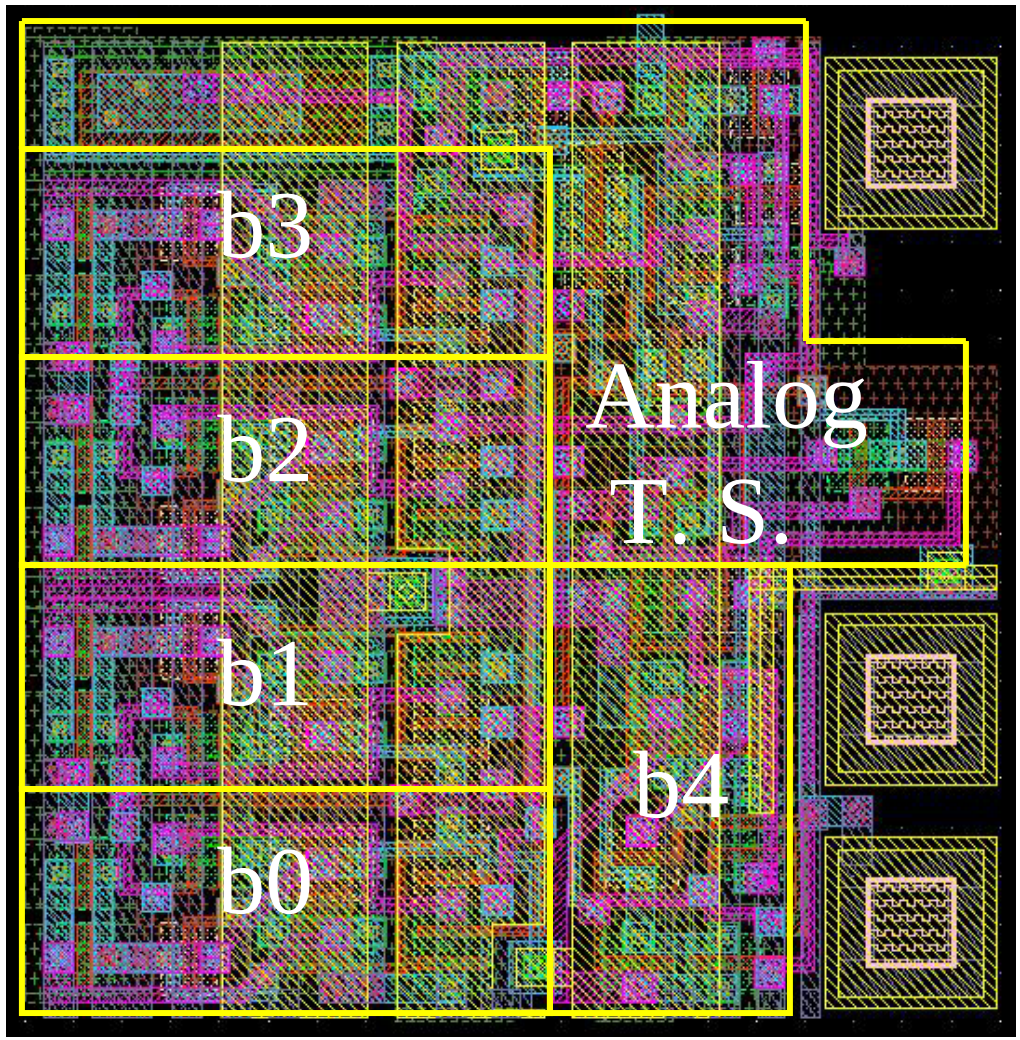
Tier 1: Sparsification

- OR for READ ALL cells
- Hit latch
- Pixel skip logic for token passing
- D flip flop (static), conservative design
- X, Y line pull down
- Register for programmable test input.
- Could probably add disable pixel feature with little extra space
- 65 transistors
- 3 via pads



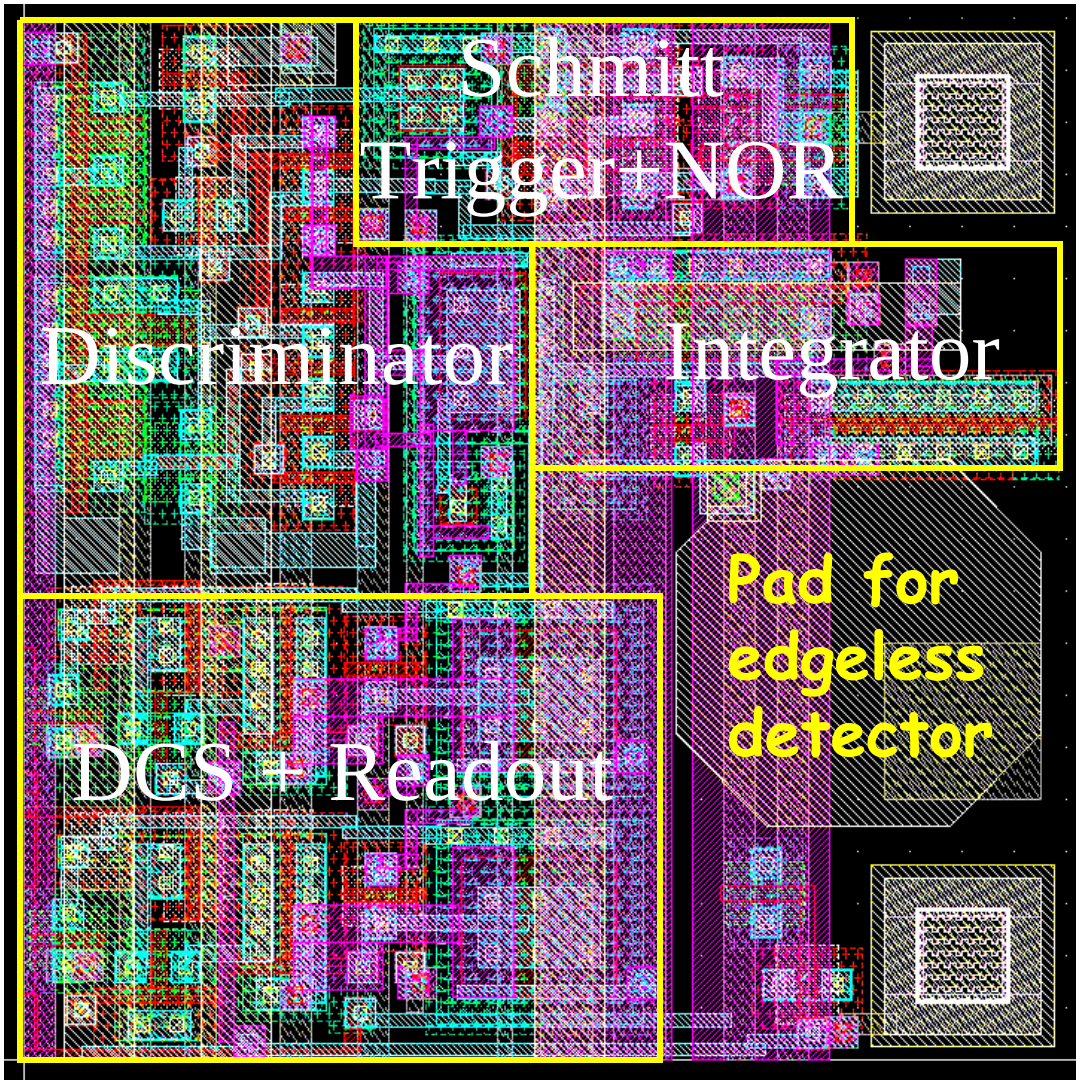
Tier 2: Time Stamp

- 5 bit digital time stamp
- Analog time stamp – resolution to be determined by analog offsets and off chip ADC
- Gray code counter on periphery
- 72 transistors
- 3 vias



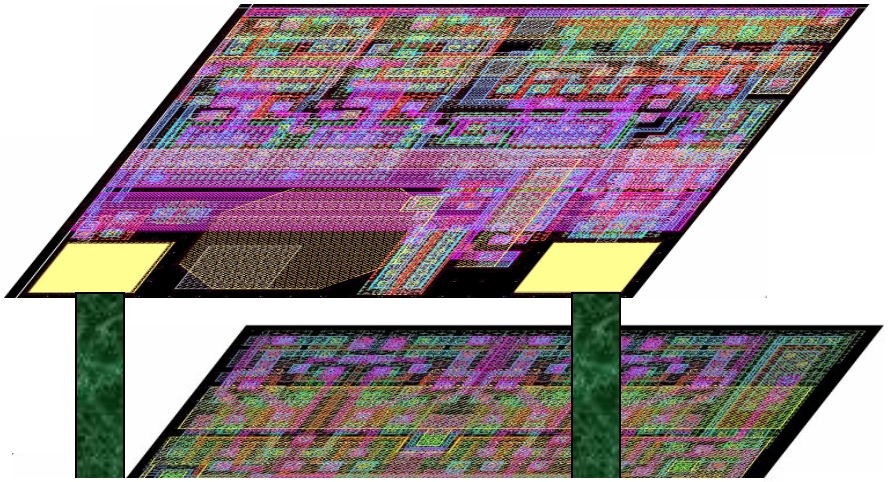
Tier 3: Analogue

- Integrator
- Double correlated sample plus readout
- Discriminator
- Chip scale programmable threshold input
- Capacitive test input
- 38 transistors
- 2 vias

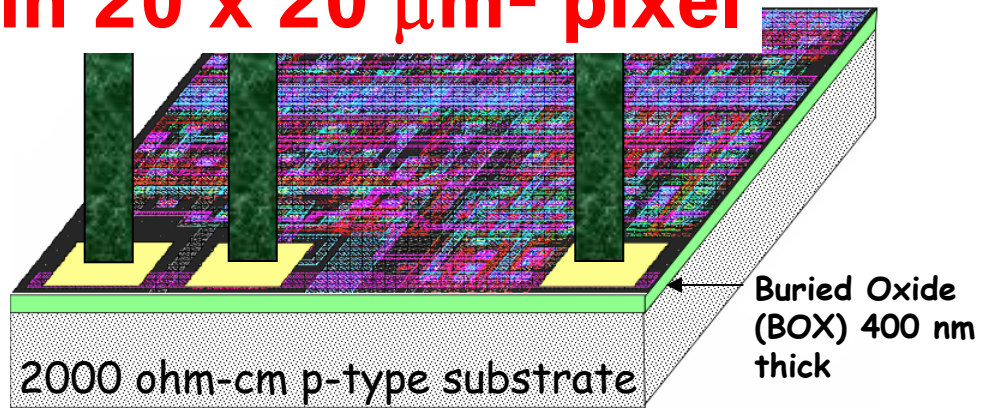


3D Stack

- Form 2 vias, 1.5 x 7.3 µm, through tier 3 to tier 2
- Tier 3
  - Integrator, DCS plus readout
  - Discriminator
  - 2 vias
  - 38 transistors
- Bond Tier 3 to Tier 2
- Form 3 vias, 1.5 x 7.3 µm, through Tier 2 to Tier 1
- Tier 2
  - 5 bit digital time stamp
  - Analog time stamp (ts)
    - Either analog or digital ts
  - 3 vias
  - 72 transistors
- Bond Tier 2 to Tier 1
- Tier 1
  - OR for READ ALL cells
  - Pixel skip logic for token passing
  - 3 vias
  - 65 transistors



175 Transistors in 20 x 20 μm^2 pixel



SOI Detector Development

- **SOI detector development is being pursued by Fermilab at two different foundries**
  - **OKI Electric Industry Co. Ltd. in Japan through Multi-Project Wafer submission (KEK)**
  - **American Semiconductor Inc. (ASI) in US, through SBIR phase I grant (Cypress semiconductor)**

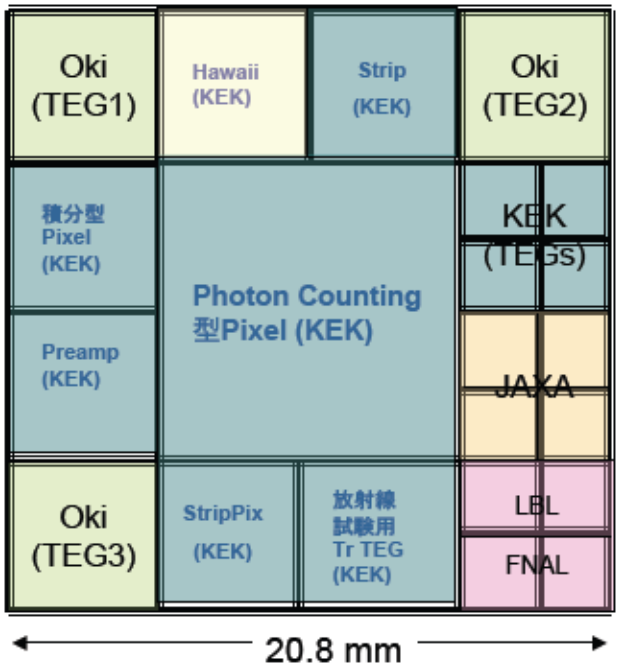
OKI		ASI	
Process	0.15μm Fully-Depleted SOI CMOS process 1 Poly, 5 Metal layers	Process	0.18μm Partially-Depleted dual gate SOI CMOS process, Dual gate transistor (Flexfet) No poly, 5 Metal layers
SOI wafer	Wafer Diameter: 150 mmϕ Top Si : Cz, ~18 Ω-cm, p-type, ~40 nm thick Buried Oxide: 200 nm thick Handle wafer: Cz、 >1k Ω-cm (*No type assignment*), 650 μm thick	SOI wafer	Wafer Diameter: 200 mmϕ Handle wafer: FZ>1k Ω-cm (*n type*)
Backside	Thinned to 350 μm no contact processing plated with Al (200 nm).	Backside	Thinned to 50-100 μm polished, laser annealed and plated with Al.

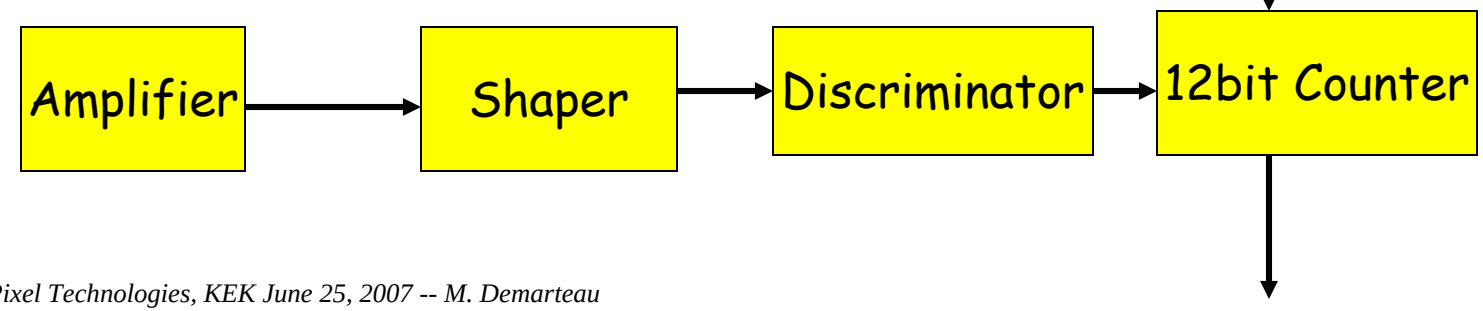
- **Goal is to understand the advantages and problems of SOI detector design, in particular issues related to trapped charges in the BOX layer due to radiation and its potential remedies through voltage on the substrate and the reduction of "back gate effect"**

OKI Process

- KEK organized first SOI Detector Workshop (March 6, 2007 at KEK) and two multi-project wafer (MPW) runs at the OKI foundry
  - The 2nd MPW run has 17 designs from 7 different organizations
  - A 3rd run is planned for later this year
- Fermilab submission on MPW: Counting pixel detector plus readout circuit
  - Maximum counting rate ~ 1 MHz/pixel.
- Simplified architecture due to design time constraint
  - Reconfigurable counter/shift register
    - 12 bit dynamic range
  - Limited peripheral circuitry
    - Drivers and bias generator
- Array size 64x64 pixels
- 350 micron detector thickness

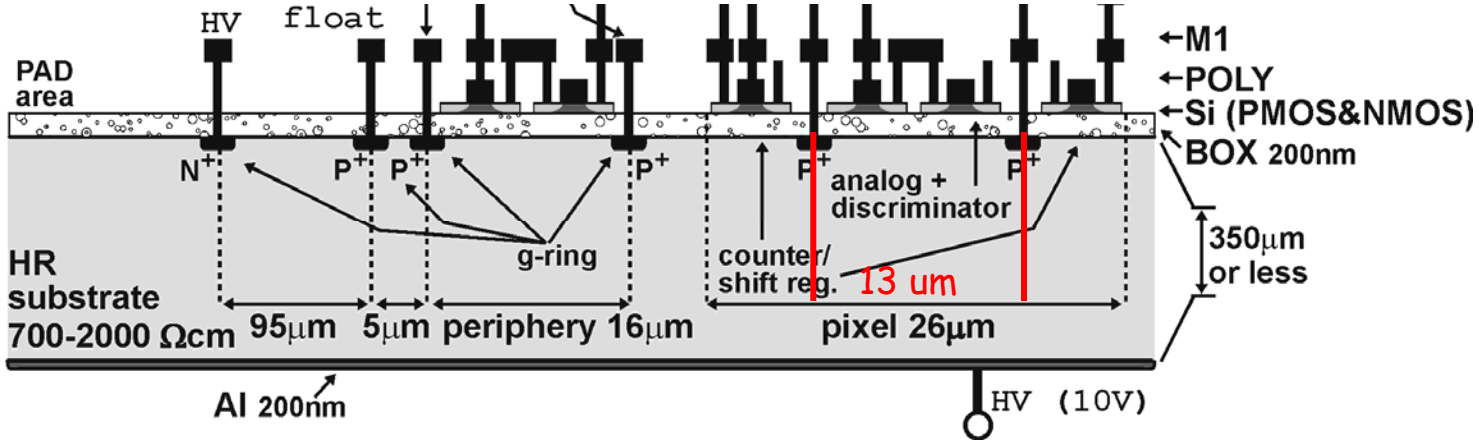
Reticule for 2nd OKI MPW run





Pixel Design in OKI Process

- **MAMBO Chip: Monolithic Active pixel Matrix with Binary cOunters**
  - **A wide dynamic range counting pixel detector plus readout circuitry, sensitive to 100-400 keV electrons, high energy X-rays, and minimum ionizing particles, designed in the OKI 0.15 micron process**
- **OKI process incorporates diode formation by implantation through the BOX**
- **Chip architecture (simplified due to design time constraint): amplifier – shaper – discriminator – binary counter**
  - **Maximum counting rate ~ 1 MHz/pixel**
  - **Reconfigurable counter/shift register**
    - 12 bit dynamic range
  - **Limited peripheral circuitry**
  - **Drivers and bias generator**
  - **Submitted Dec. 15, '06; delivered this month.**
  - **Array size 64x64 pixels, 26μmx26μm**
  - **13 μm implant pitch, to minimize the "back gate" effect**
    - 4 diodes per pixel
  - **350 micron detector thickness**

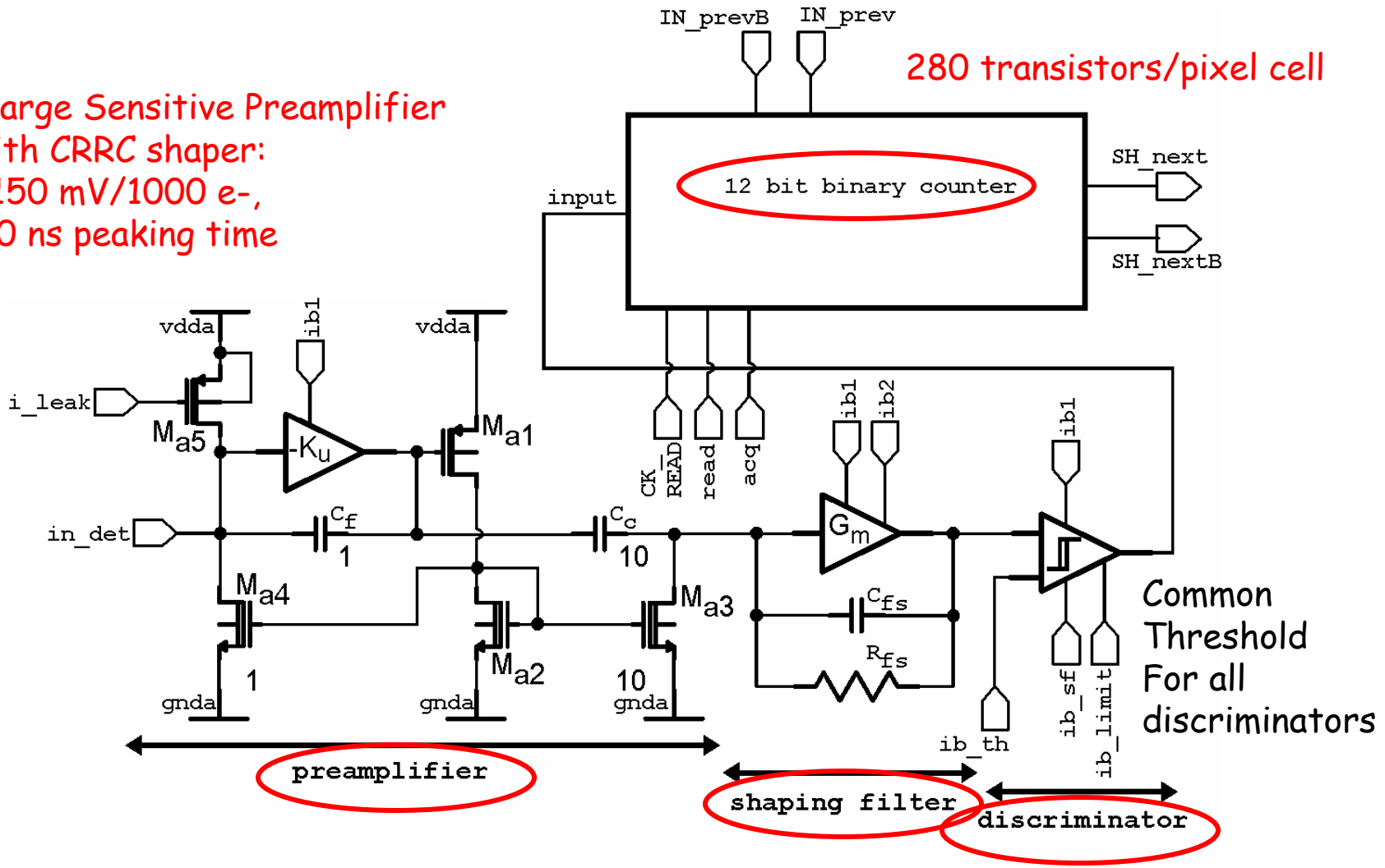


Pixel Design in OKI Process

- **Schematic circuit diagram**

Charge Sensitive Preamplifier
with CRRC shaper:
~ 150 mV/1000 e-,
150 ns peaking time

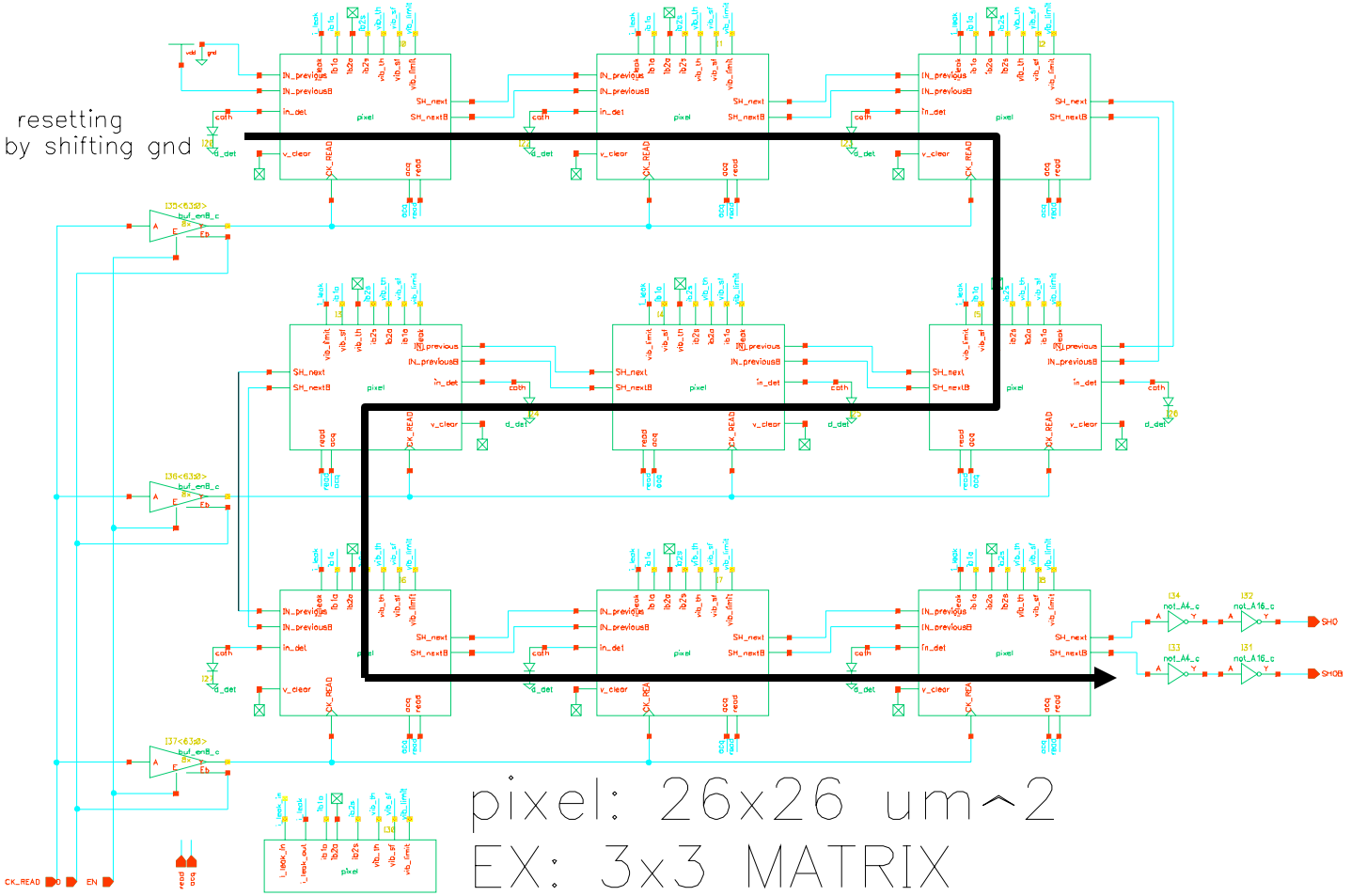
280 transistors/pixel cell



Simplified 3x3 Matrix

Operates in two modes:
Acquire/Read out

12 bit counter is reset by changing counter to a shift register configuration and shifting in zeros during read out.

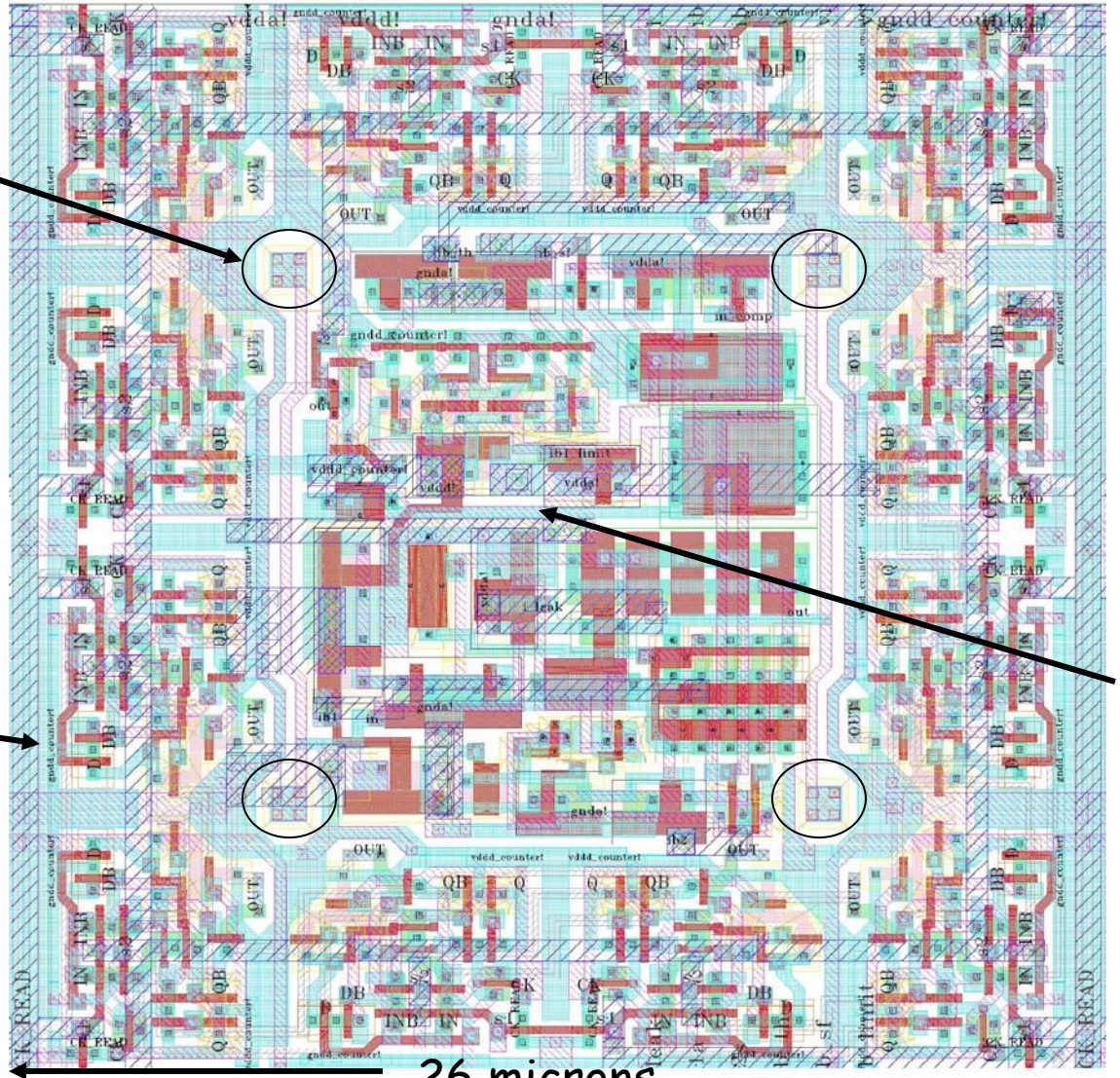


Pixel Cell Layout

- **Layout of single 26mmx26mm pixel cell**

One of four detector diodes

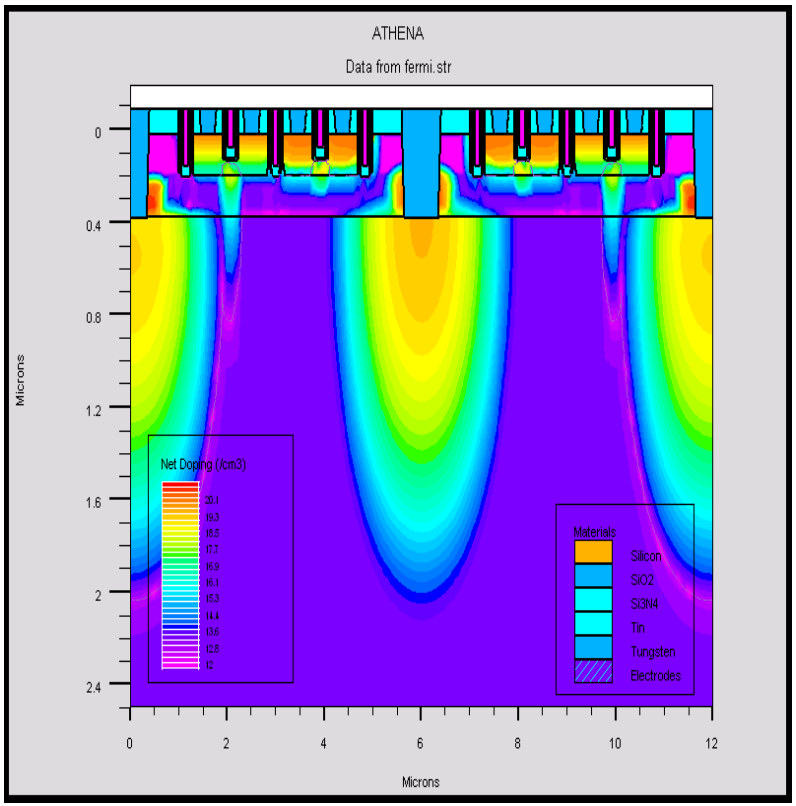
One of twelve D flip-flops arranged around perimeter of pixel cell



All analog circuits are located in center of pixel cell between diodes and surrounded by guard ring

Pixel Design in ASI Process

- **SBIR Phase I grant with American Semiconductor (ASI), Boise, Idaho**
- **ASI process (0.18μm) based on an SOI dual gate transistor called a Flexfet™**
  - **Flexfet has a top and bottom gate**
  - **Bottom gate shields the transistor channel from**
    - Charge build up in the BOX caused by radiation.
    - Voltage on the substrate and thus removes the back gate voltage problem
  - **Modeling and process simulation of a thinned, fully depleted sensor/readout device.**
  - **Studies of backside thinning, implantation, and laser annealing in collaboration with Cornell**
  - **Circuit design for ILC pixel cell**
    - Voltage ramp for time marker
    - ~20 micron analog pixel
    - Sample 1 - crossing time
    - Sample 2 - time over threshold for analogue pulse height information
    - Coarse time stamp

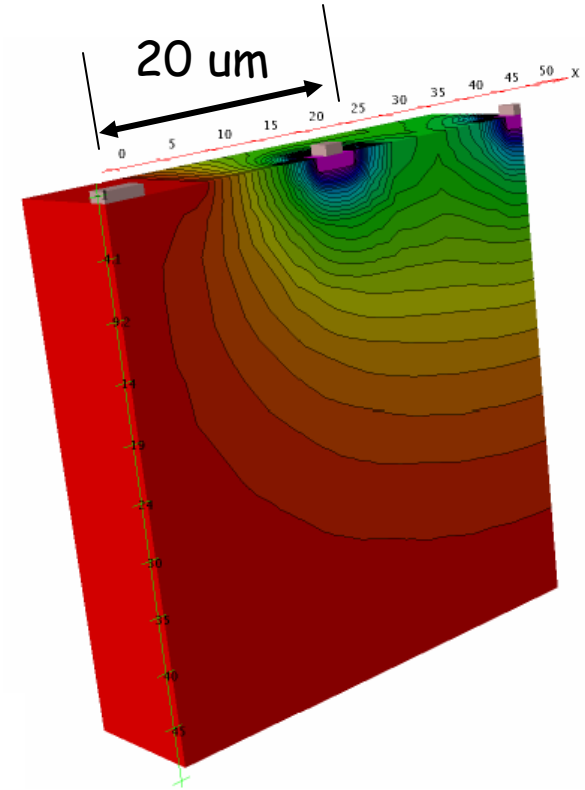


Diode simulation in Flexfet process

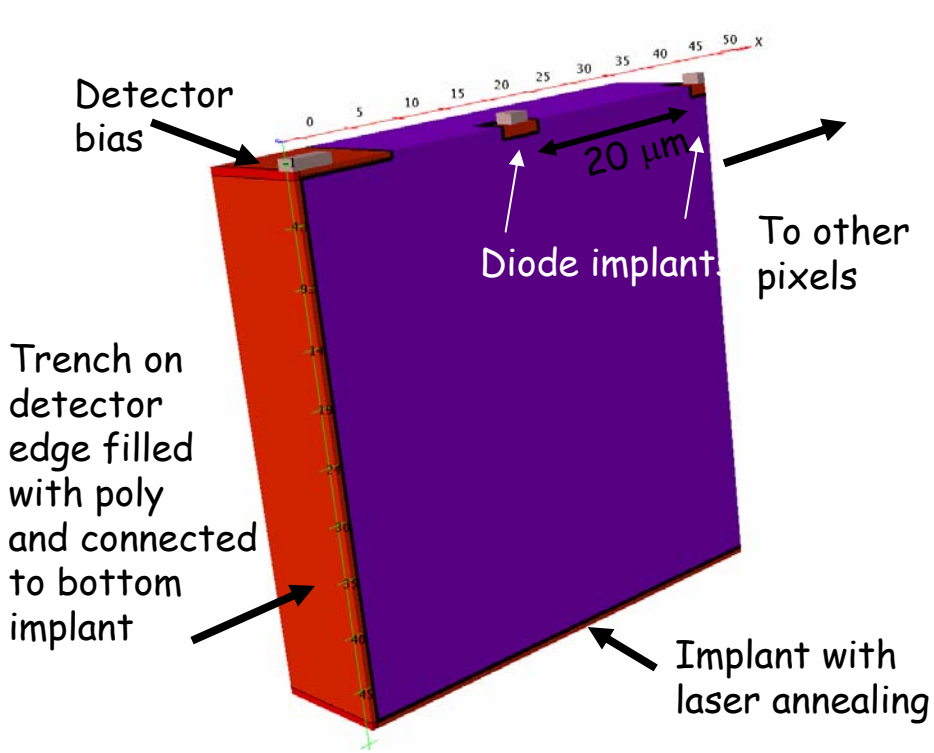
http://www.americansemi.com/

Development of Thinned Edgeless Sensors

- **3D chip provides only readout. In parallel we have submitted a design for sensors on 6", high resistivity, float-zone, n-type wafers to be bonded to 3D chips**
- **The sensors are of the "Thin Edgeless" design**



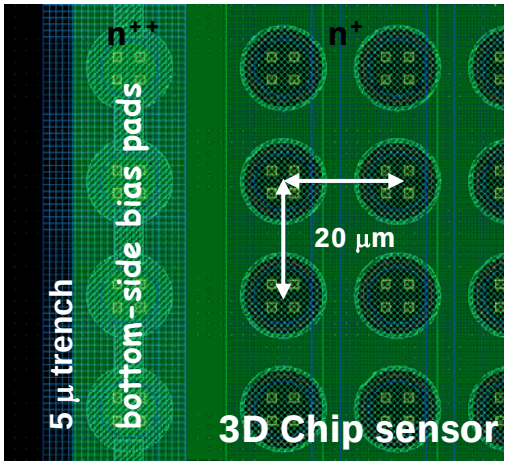
Equipotential lines in detector near one detector edge

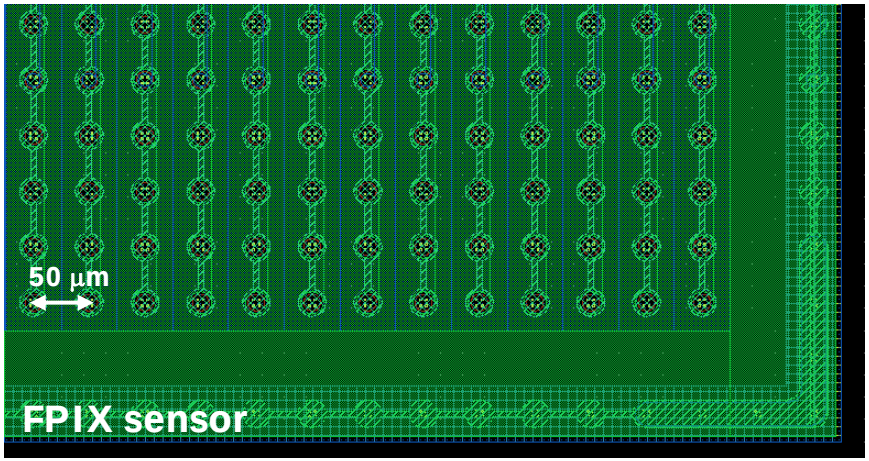


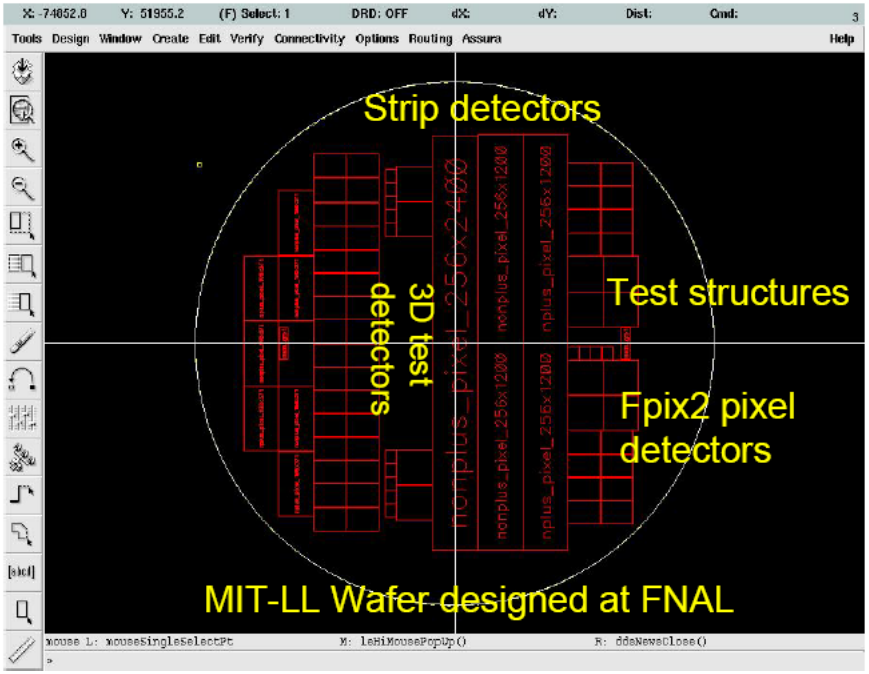
Detector Cross section near one detector edge

Sensor Design

- **Producing a set of detectors at MIT-LL, thinned to 50-100 microns for beam and probe tests**
  - **Masks designed at FNAL, standard p-on-n diodes**
    - Strip detectors (12.5 cm x ~2 cm)
    - Test structures
  - **Sensors to mate with 3D chip, 20 micron pitch**
  - **Sensors to mate with FPIX chip, 50 micron pitch**
- **Goal to validate the process**
  - **Explore and validate the technologies which provide thinned detectors sensitive to the edge**
  - **Measure the actual dead region in a test beam**

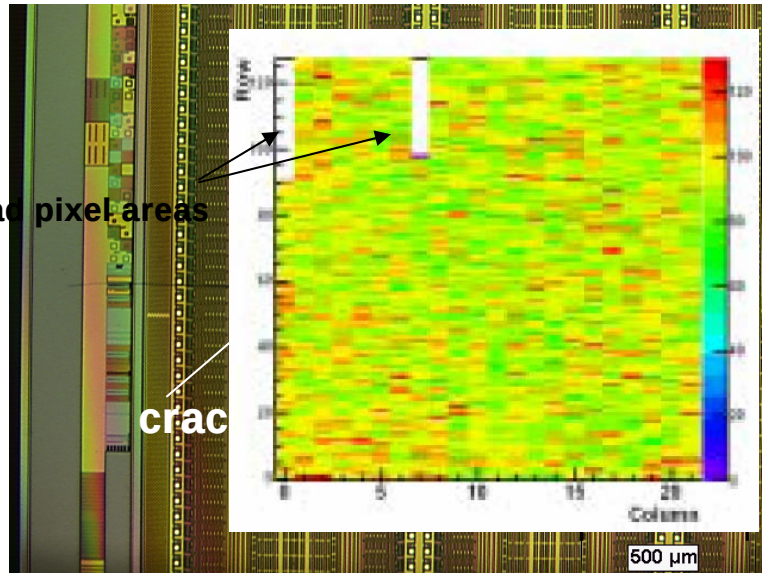


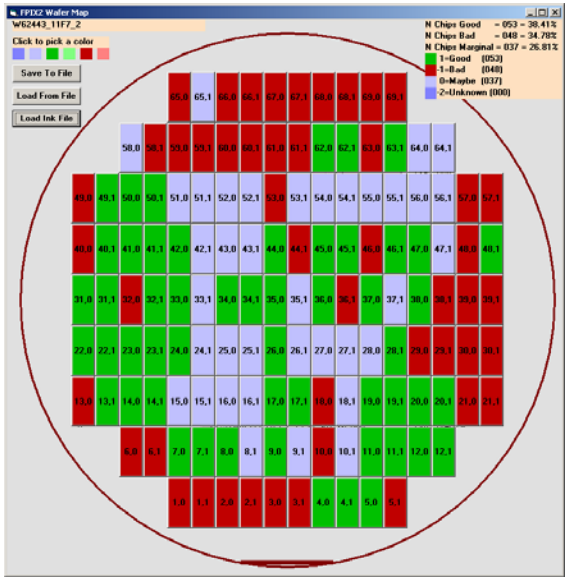




Device Thinning

- **Gaining experience on device thinning and thinned devices**
  - **Thinning of individual FPIX die at RTI**
    - Two step procedure:
      - Backgrind and polish to 150 μm
        - » 7 chips failed out of 72
      - Plasma thinning down to 50/25/15/10 μm
        - » 4 responding out of 20 testable die; all have areas of dead pixels
    - Repeat after evaluation
      - 6 chips out of 8 working (2 dead)
  - **Thinning of full wafer at IZM**
    - Yield ~50%

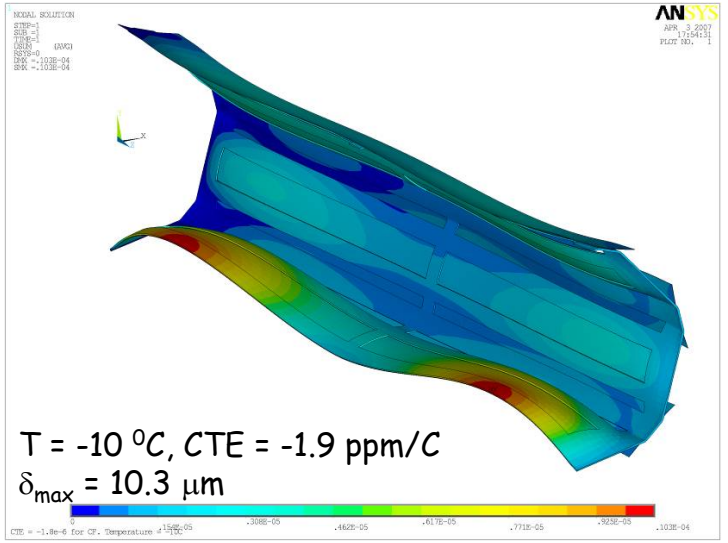




- **No indication of subtle electrical effects associated with thinning the wafer. The IZM wafer looks (visual inspection) very good except.**
- **Small (~10%) apparent noise and threshold dispersion increase observed for parts thinned by both RTI & IZM that tested "good" not understood**

Vertex Detector Mechanical Design

- **Multi-layered, high precision, very thin, low mass detectors**
  - **Goal: layer thickness of 0.1% X_0 per layer, equivalent of 100 μm of Si**
- **Collaborating with the University of Washington on carbon-fiber mechanical support structures**
- **Developing techniques for fabricating and handling thin-walled carbon fiber structures**
- **Prototypes of carbon-fiber support structures**
  - **Three prototype half-shell structures fabricated for evaluation and testing**
- **Develop assembly tooling / mandrels**
  - **Assembly mandrel, end ring glue fixture and vacuum chuck for precision placement of silicon wafers on support structure**
- **FEA analysis of mechanical and thermal behavior**
  - **Deflection under gravity OK**
    - maximum deflection vector is about 0.6 μm
  - **Thermal deflections unacceptably large**
    - assuming -10 ^{0}C operation, CTE mismatch
    - CTE = -1.9 ppm/C. δ_{max} = 10.3 μm
      - CTE_{Si} is 2.49 ppm/K



Fermilab Strategy

- We believe the 3D and SOI technologies are very promising – not just for HEP pixel detectors
- Our intent is to understand these technologies through the design and testing of demonstrator devices with test structures for the ILC/LHC and other applications
- With that goal, we are
  - Collaborating for the 3D technology with MIT-Lincoln Laboratory, RTI, IZM, Ziptronix, …
  - Exploring commercial processes which include processing of the handle wafer as part of the fabrication process for SOI (OKI, American Semiconductor)
  - Developing expertise in necessary technologies
    - Post processing (handling of thinned wafers, annealing, dicing...)
- R&D is underway to understand
  - How to retain good, low leakage current, detector performance through the CMOS topside processing
  - What is the optimal process for forming the detector diodes?
    - Model charge collection, shielding
  - Performance under radiation, notably behavior of the BOX
- We are, in addition, carrying out R&D in mechanical support structures and system integration issues for pixel vertex detectors