中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

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Tsukuba

R&D on SOI Counting Pixel Chips

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Experiments and Detectors of IHEP

IHEP at Beijing
- State Key Laboratory of Particle Detection and Elec.
- BESIII: DC+TOF+EMC+RPC
- PET and detectors in applycation
- Synchrotron Radiation Detector
- Satellite: HXMT
- ……

Yangbajing Cosmic Ray Exp.
- RPC
- Plastic Scintillator + PMT
- Water Cherenkov
- Scintillator + Fiber + PMT

Dayabay Neutrino Exp.
- Neutrino Detector
- Water Cherenkov
- RPC

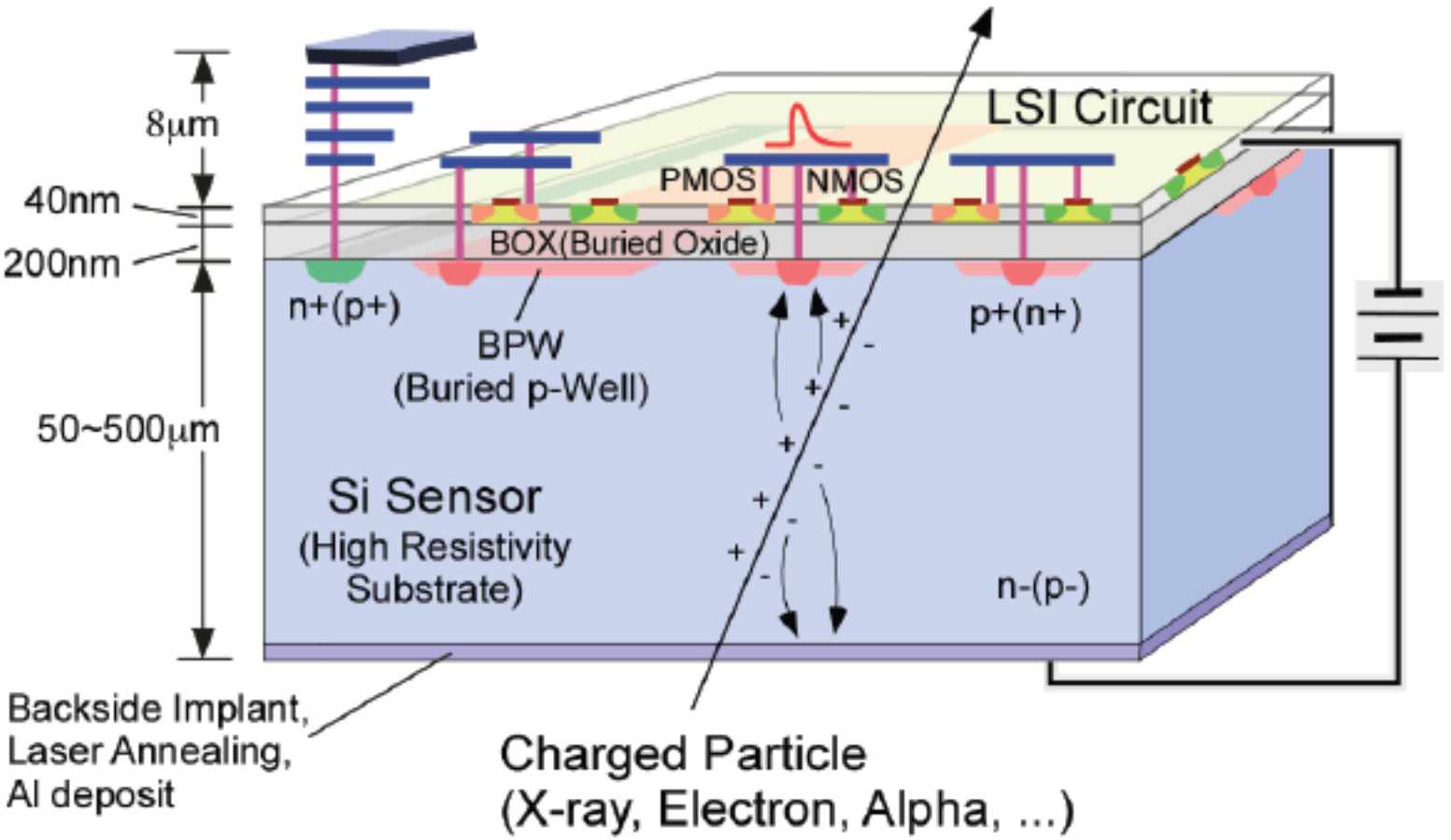
CSNS
- ^{3}He High pressure MWPC
- Fiber + ZnS:^{6}Li(Ag)
- GEM + Boron

JUNO Exp.
- 20K ton liquid scint.
- 3% energy resolution(at 1MeV)
- 700-meter deep underground

Outline

- Introduction to SOIPIX
- Motivation of Counting Pixel R&D
- Nested-Wells-based design
  - CPIXTEG2 by A-R-Tec
  - CPIXTEG3
- DSOI-based design
  - CPIXTEG3b
- Summary

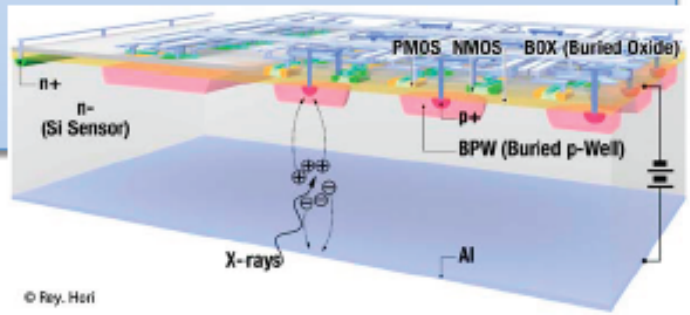
Silicon-On-Insulator Pixel Detector (SOIPIX)



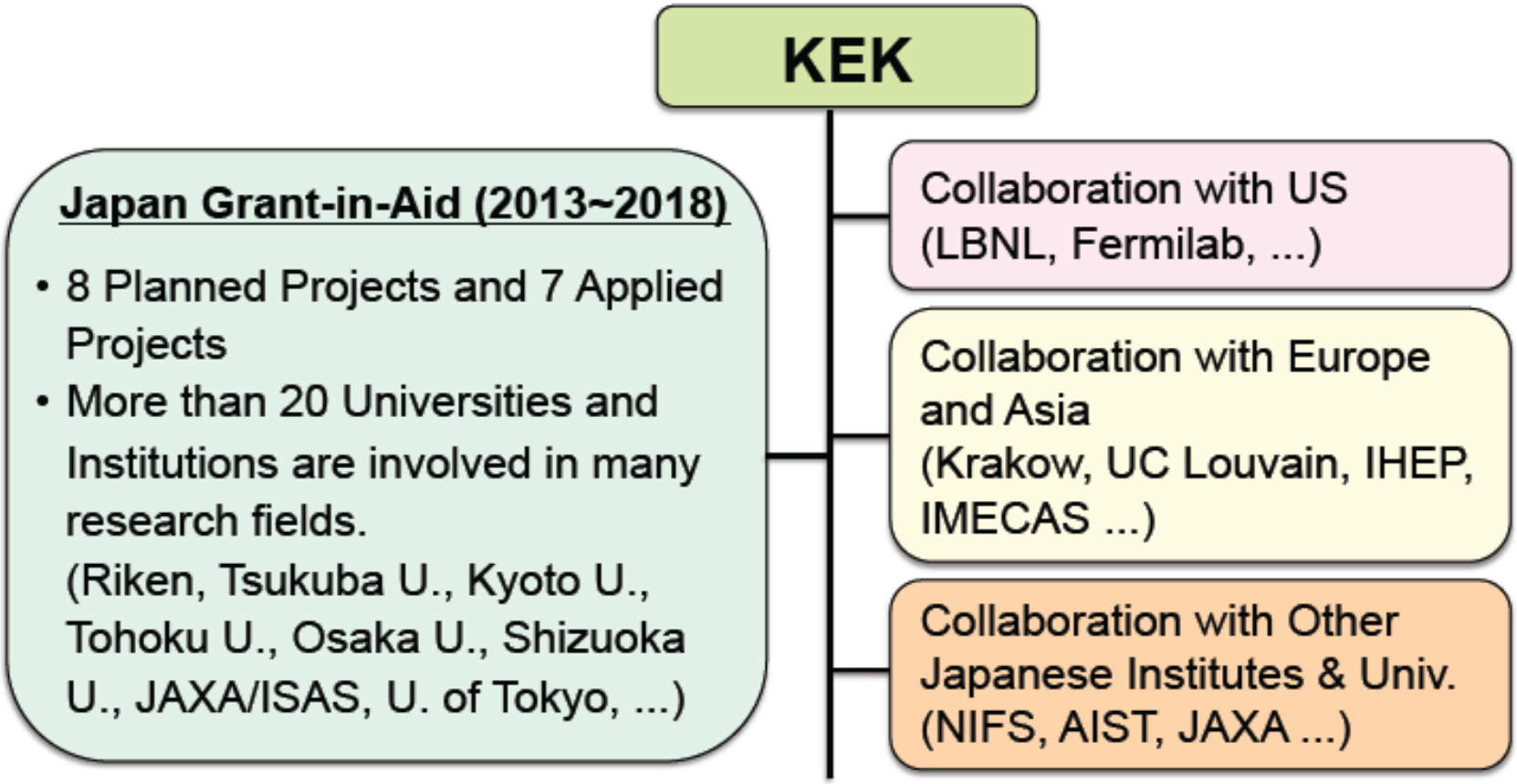
High Resistivity Substrate + CMOS Circuit

Features of the SOI Pixel Detector

- No mechanical bonding. Fabricated in industrial semiconductor process.
- Full CMOS transistors are available.
- Thickness of the sensor is adjustable（50~500um), and possible to operate in full depletion. (Wide Application)
- Low sense node capacitance and possible to fabricate custom sensor structure.
- No latch up and Low single event cross section.
- Can be operated in wide temperature (1K-570K) range.



SOIPIX Collaboration



T-Micro

ROHM GROUP LAPIS SEMICONDUCTOR

Rigaku

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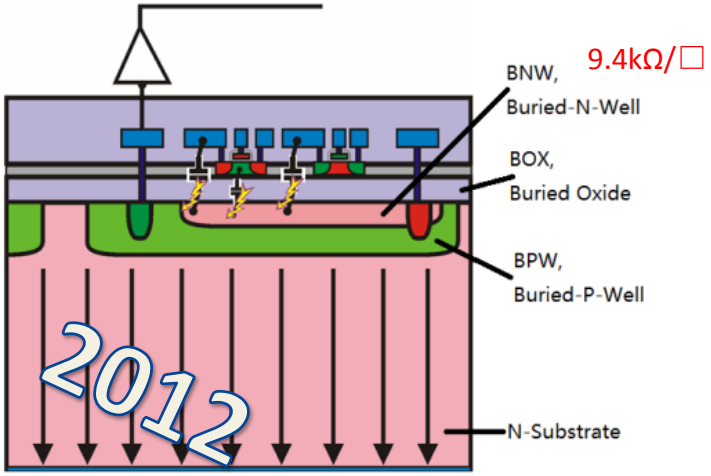
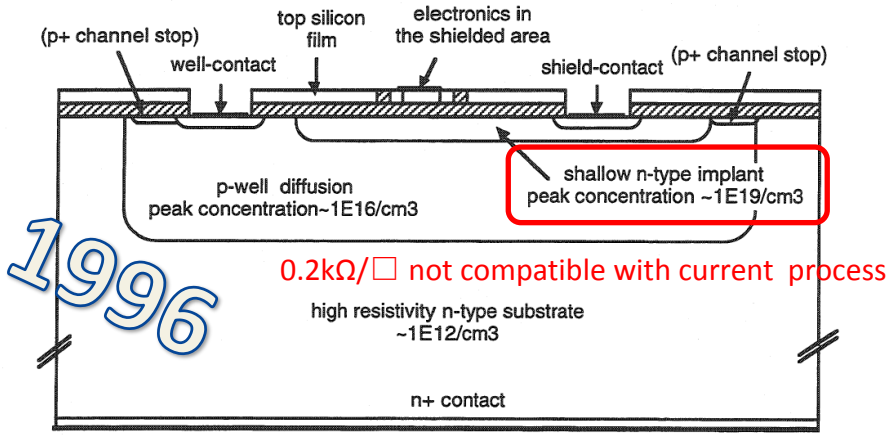
Motivation(1)

- Counting Pixel is an effective measure to study shielding effect in SOIPIX detectors.
  - A key issue in SOI Pixel Technology
  - Necessity of shielding recognized and understood by F. X. Pengg
  - Counting pixel suffered from charge injection most, while integrating pixel not sensitive to it.



- more recent version: Nested-Wells
- more fancy thing: Double SOI…



Figure(2.11a): The n+-p-n- structure of shield and well in the high resistivity substrate, cut.

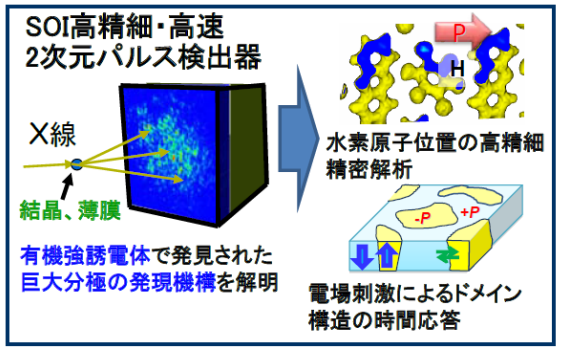
- Shielding-well proposed by F. X. Pengg in his dissertation “Monolithic Silicon Pixel Detectors in SOI Technology”
- Good in concept but not implemented successfully.

Motivation(2)

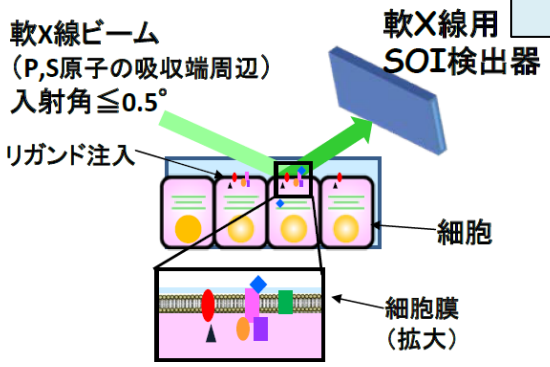
- Counting Pixel is getting more and more popular in synchrotron radiation application due to superior performance.
  - Macromolecular Crystallography, Small-Angle Scattering (SAXS) etc.
  - Fast readout / no readout noise / High dynamic range /Sharp point spread function
- Targeted on the detector proposed by Prof. Shunji Kishimoto (PF, KEK).
  - Very compact pixel circuit
  - Very good S/N required

Specifications:
30*30 um^2 pixel size
1k frames/s
14-bit counter
Low energy X-ray 2~4 keV

Ferroelectricity in a molecular crystal

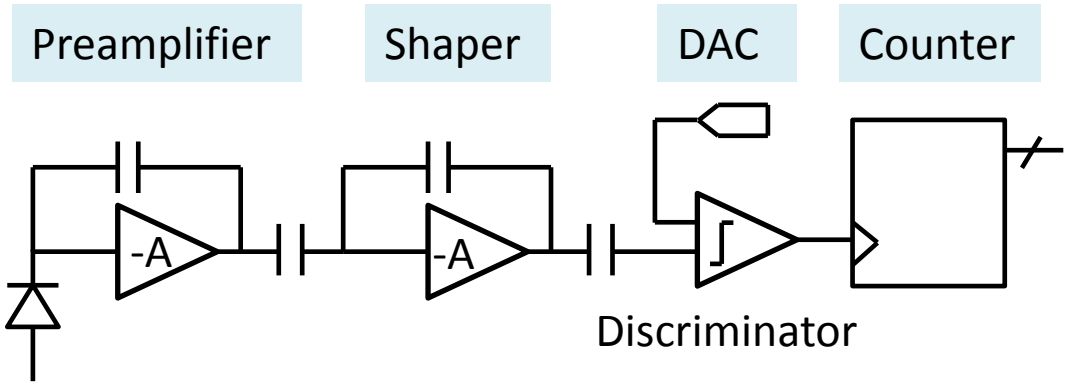


Structure change of a cell membrane



Fundamental Issues

- On-chip circuit
  - Amp-Sha-Disc system
  - Counter and register in pixel
- Shielding (Charge Injection)
  - Nested-wells
  - Double SOI
- Leakage current
  - Full depletion guaranteed
  - Contribute to noise level but can be mitigated by low temperature
- Radiation damage
  - Fine if back-illuminated by low energy X-ray



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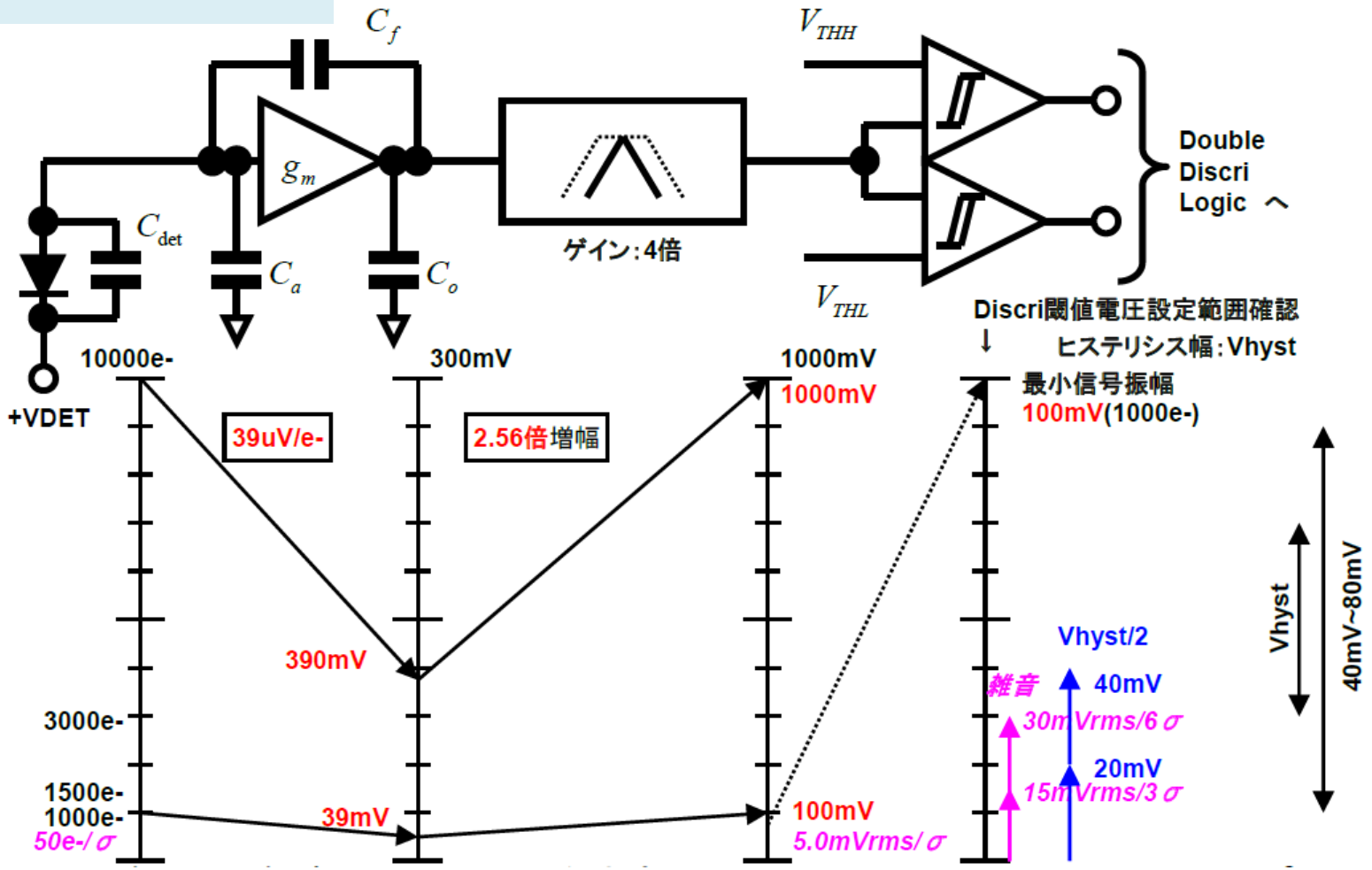
Amp-Sha-Disc in CPIXTEG2

Preamplifer
- 1000-10000e-
- Cf ~4fF

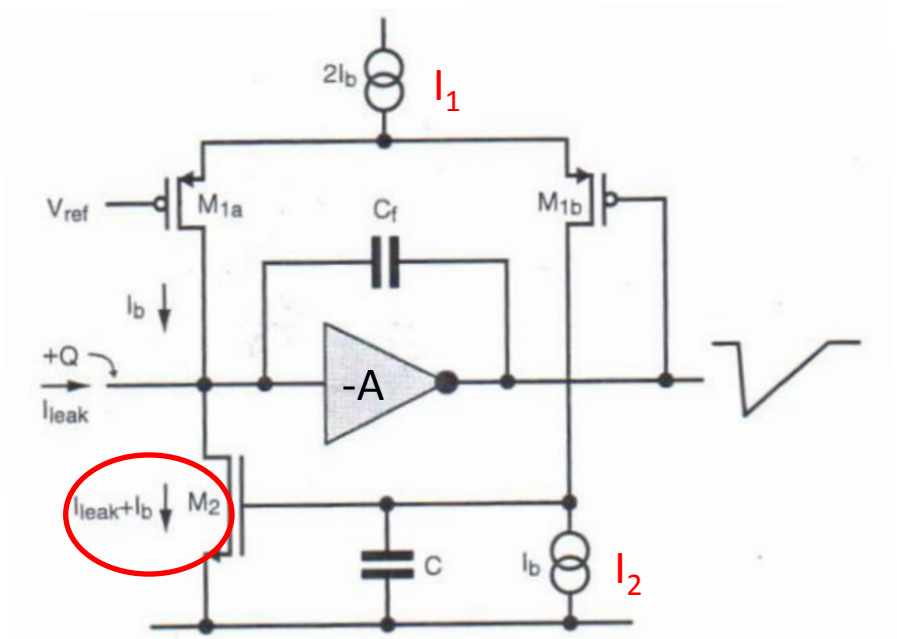
Shaper
- Vgain 2.5

Dual Discriminators
- Threshold window
- Hysteresis



Feedback and Leakage Compensation

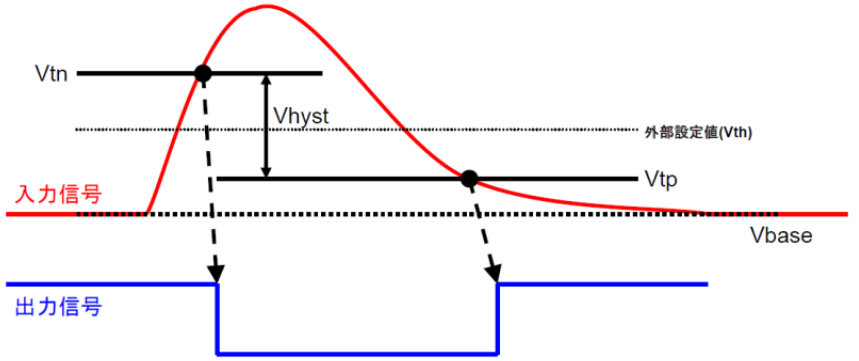
- The krummenacher scheme used for preamplifier and shaper
  - High gain amplifier in the core
  - Leakage compensated by M_2
  - Feedback current set by $I_b = I_1 - I_2$
  - Vout DC set by Vref
- Very popular in pixel circuit but it relys on the precise I_1 and I_2
  - Failure if $I_2 > I_1$



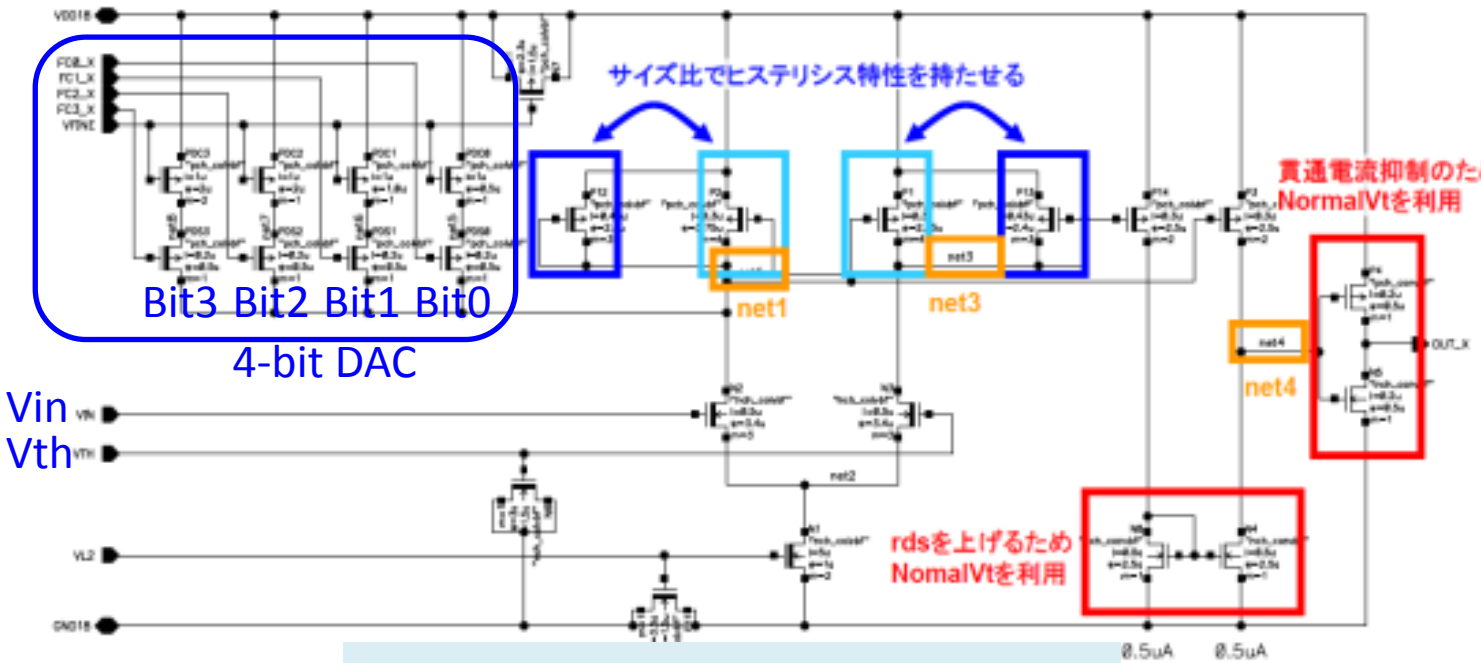
The krummenacher scheme for P-in-N sensor

Discriminator

- Hysteresis to avoid noise hit
  - Vtn, threshold for a Low to High transition
  - Vtp, threshold for a High to Low transition
  - Vhyst > $3\sigma_{noise}$
- Global threshold set by Vth
  - Local adjustment by a 4-bit DAC in pixel



Principle of hysteresis



Schematics of discriminator and DAC

Discriminator

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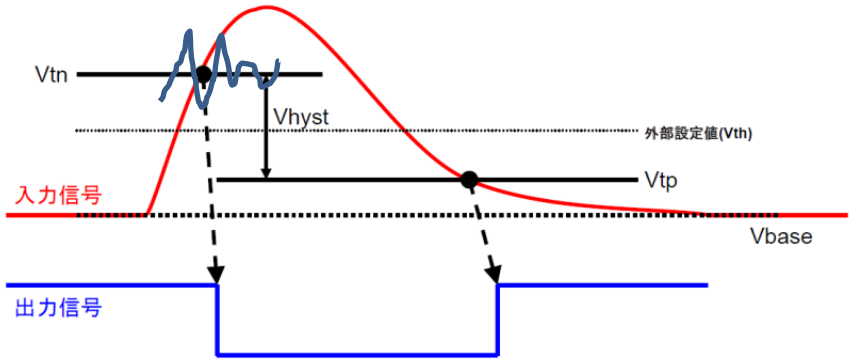
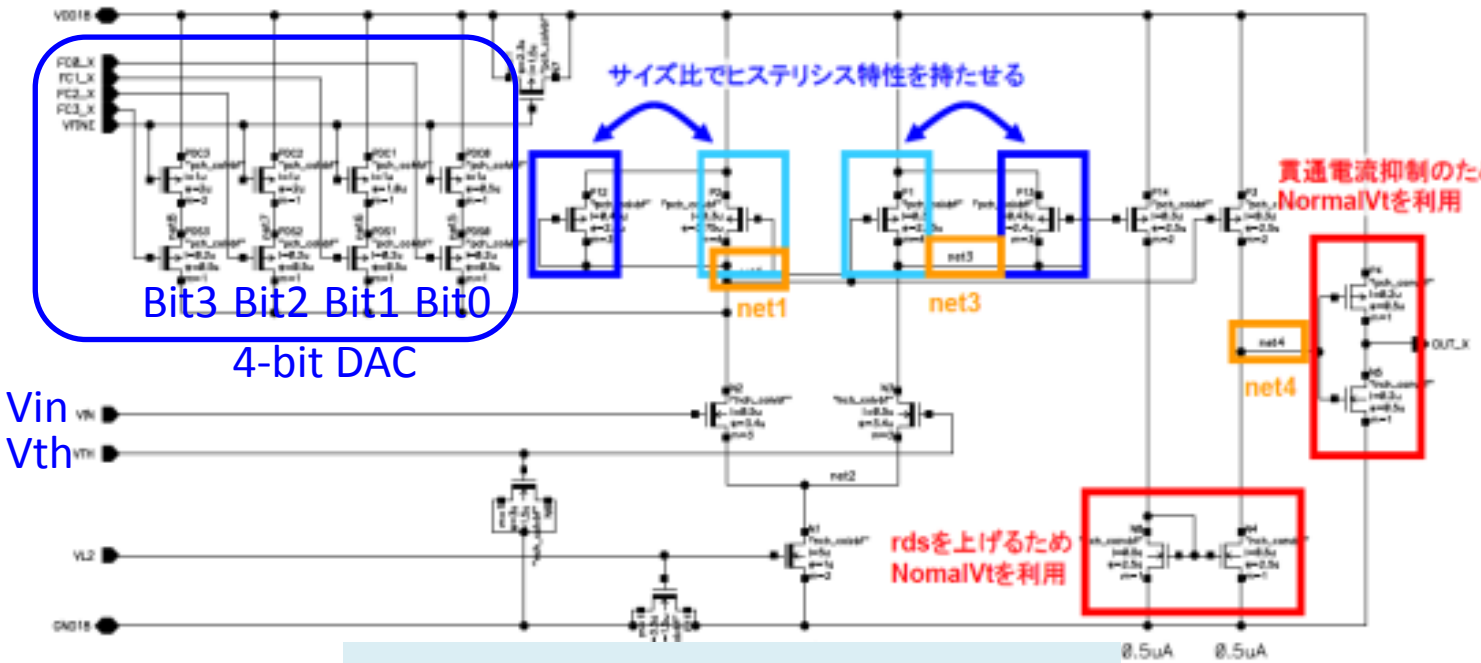


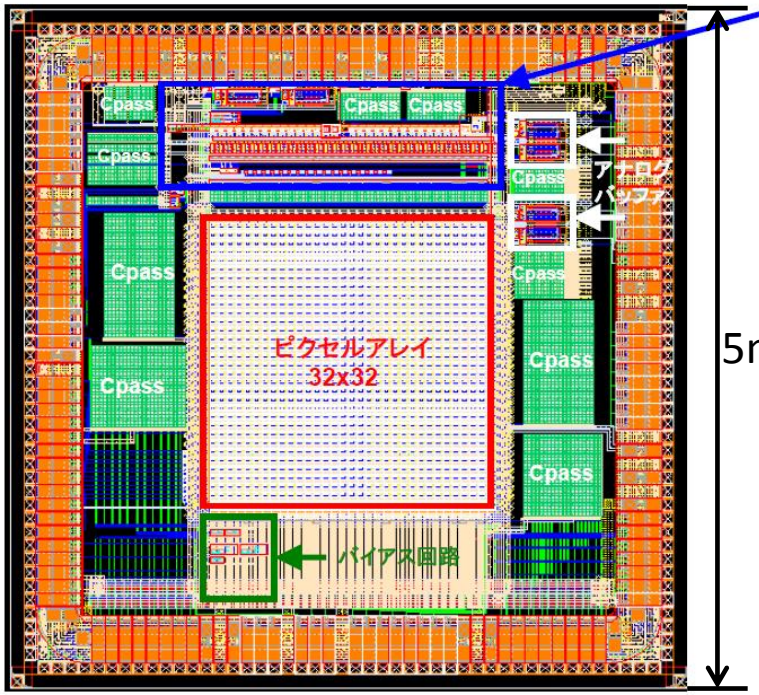
Principle of hysteresis



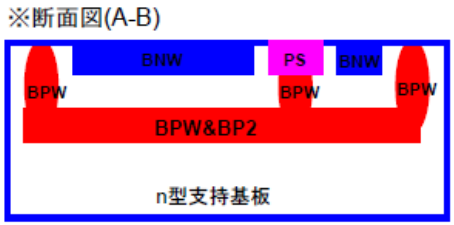
Schematics of discriminator and DAC

Layout

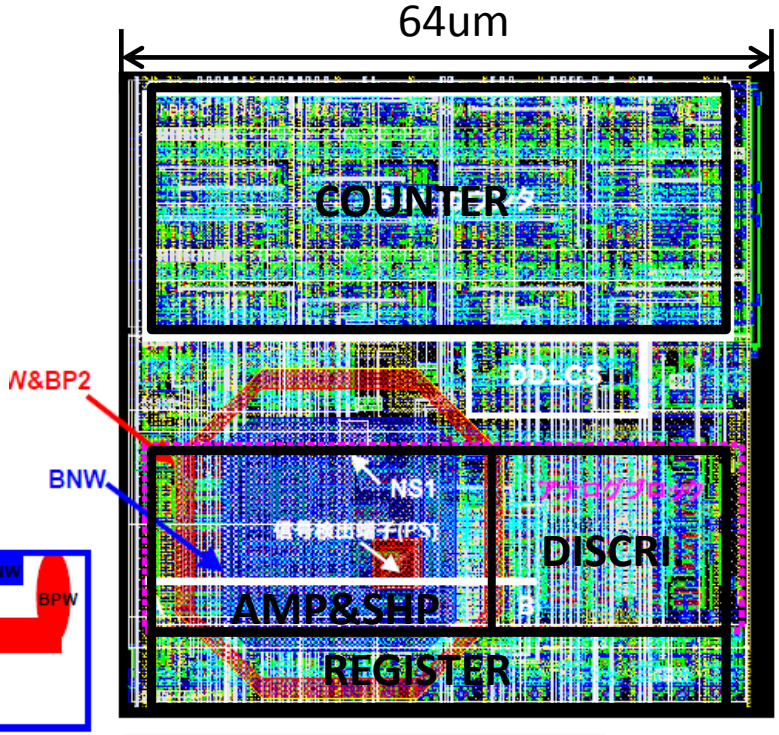
- Chip size 5mm*5mm
- Pixel size 64um*64um
- 16-bit Counter & 10-bit Register
- Amp-Sha covered by Nested-wells
  - Bias voltage limited due to back gate effect



CPIXTEG2 Chip layout



Nested-Wells

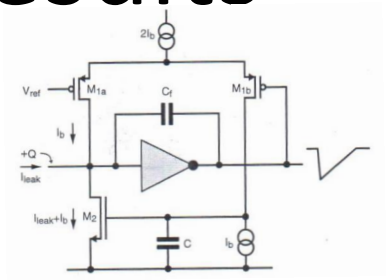


CPIXTEG2 Pixel layout

Overview of CPIXTEG2 results

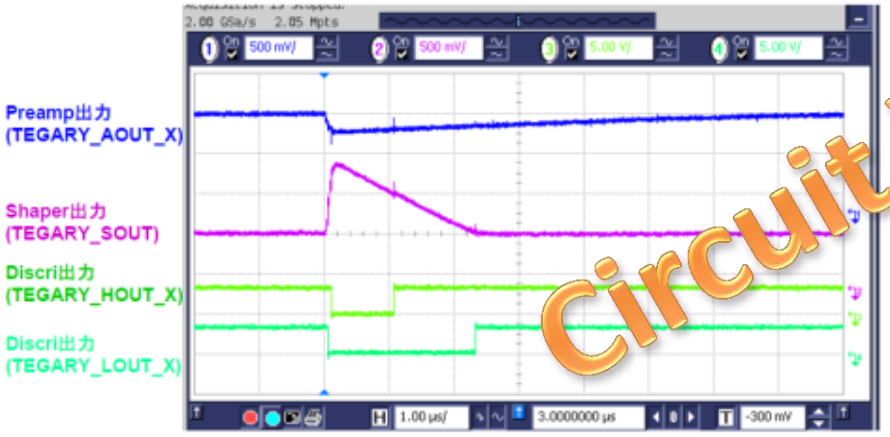
A-R-Tec

- ✓ Amp-Sha-Disc system
- ✓ Counter and Register
- ✓ Bias and Aobuf
- • Current Source variation

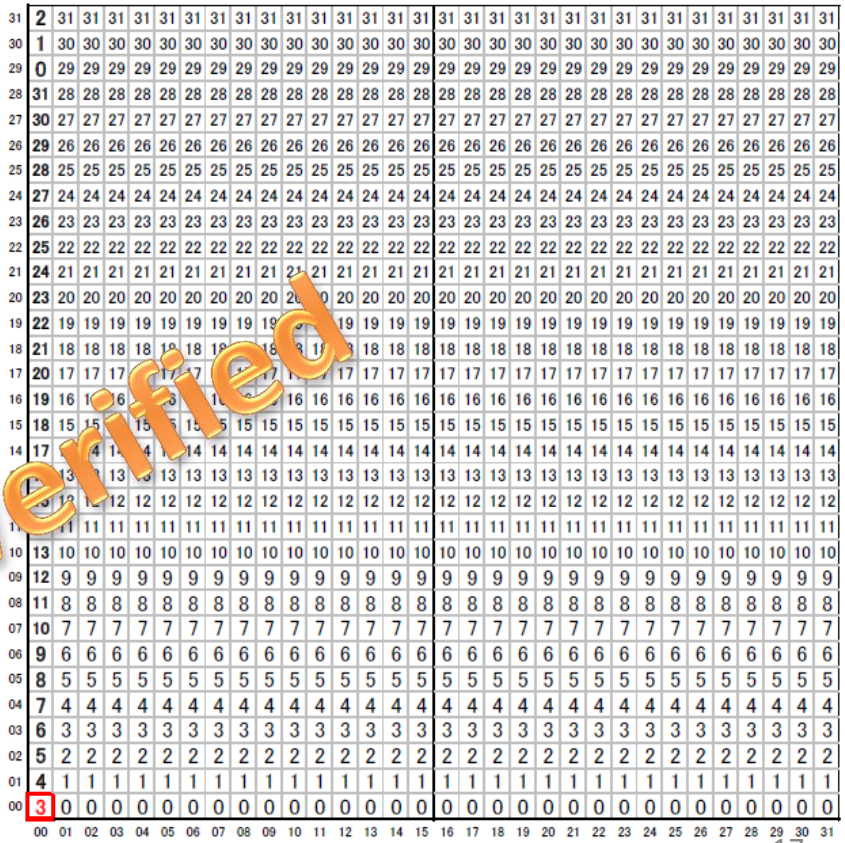


- ✓ Shielding between analog and sense node
- ✓ Response of Light stimulus
- • Shielding between counter and sense node not reported

analog waveform



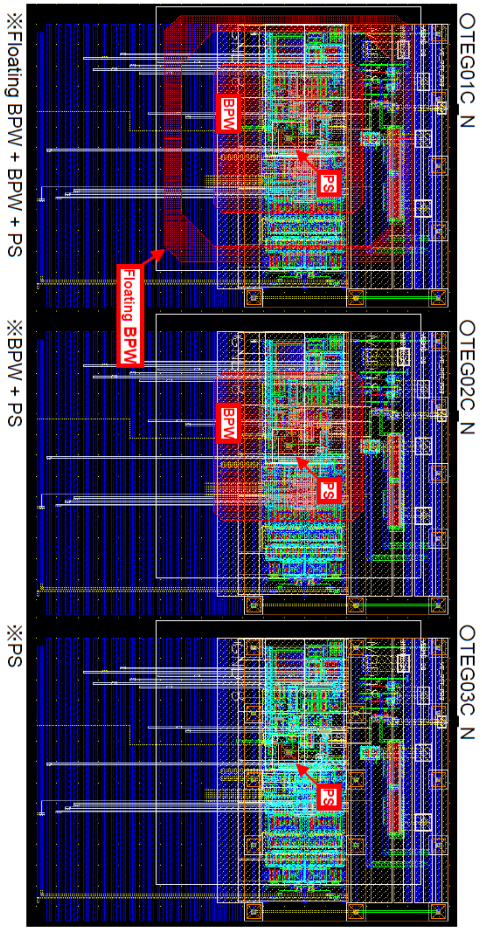
Counter & Register access

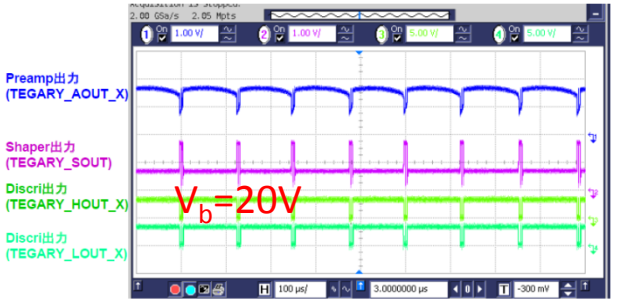


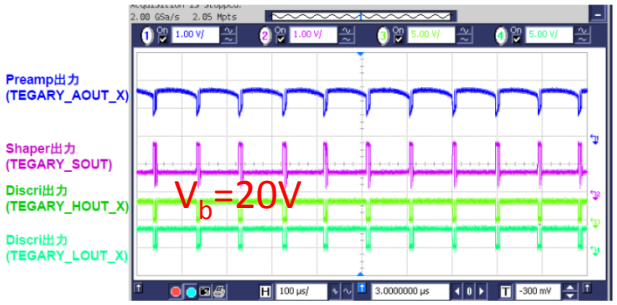
Circuit behaviors with sensor connected

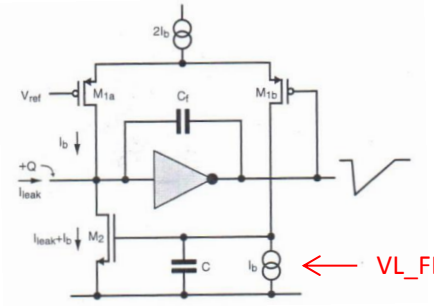
A-R-Tec

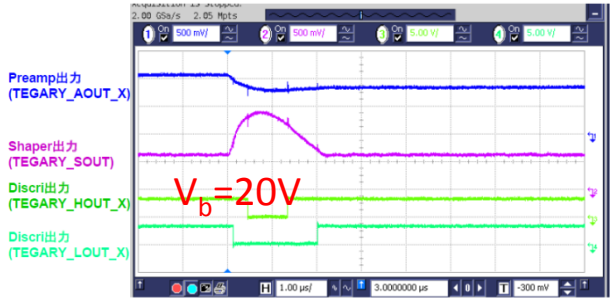
- ✓ Crosstalk between BPW and Transistors observed.
- ✓ Nested-wells is effective in shielding shaper.
- • Shielding of discriminator and counter not evaluated yet.
- • Failure of current mirror, overridden by external port.

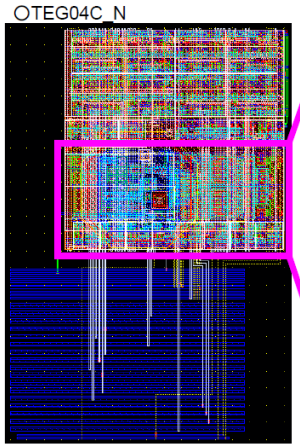


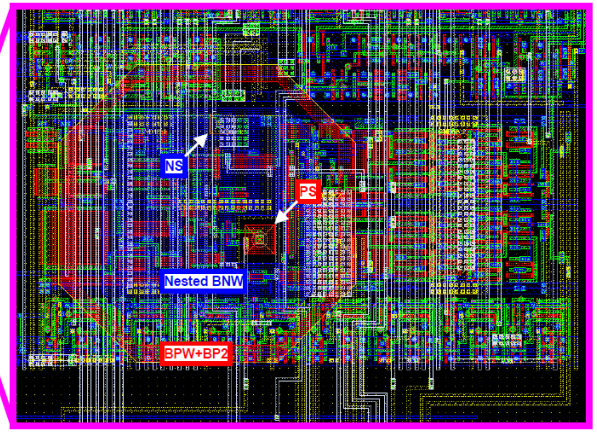












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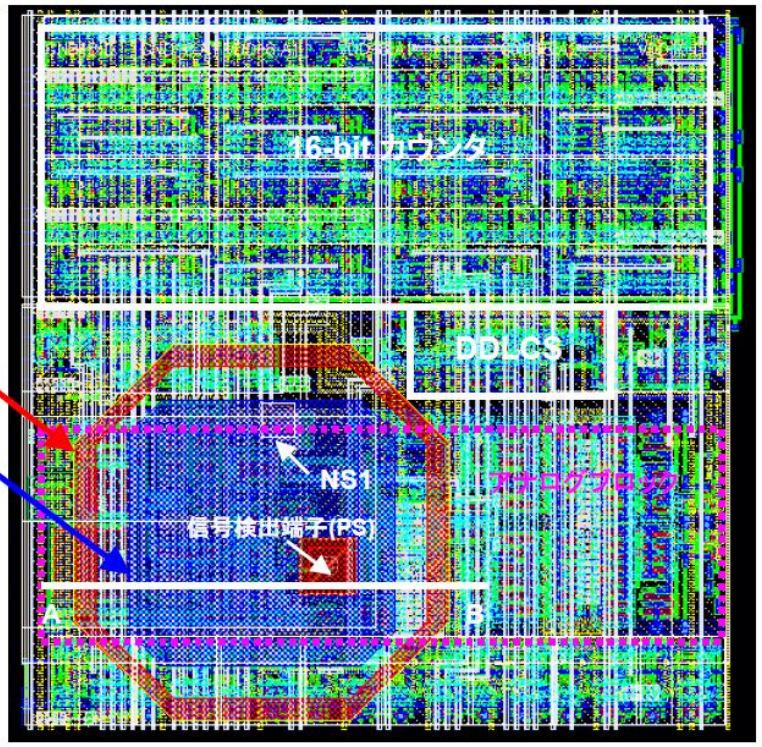
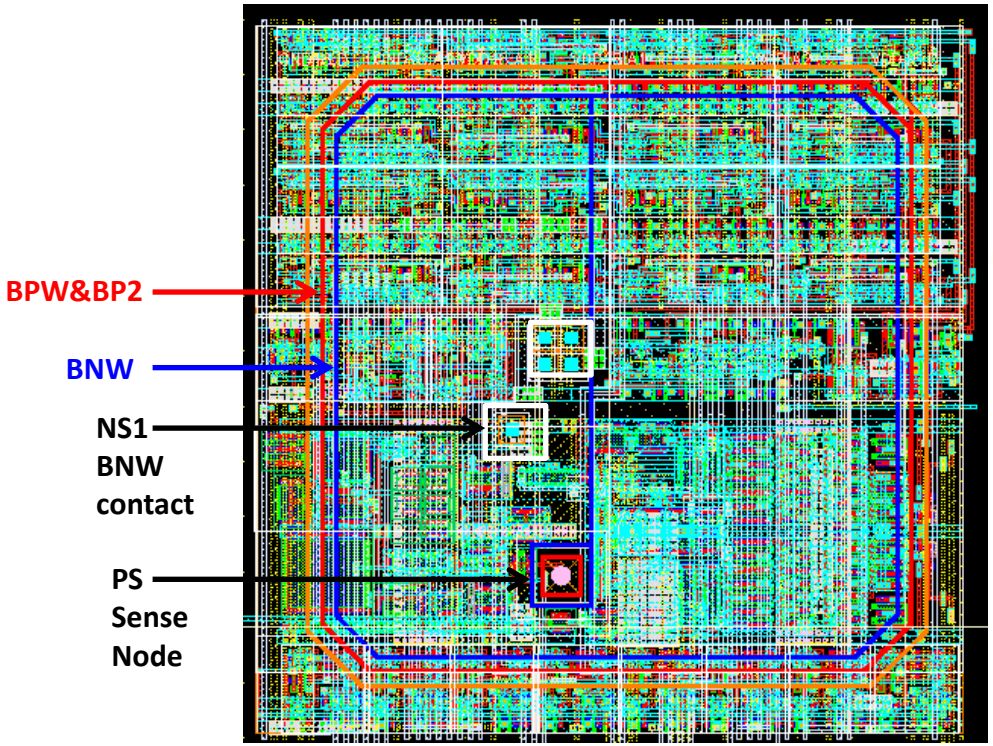
Continuing efforts of Nested-wells on CPIXTEG3

- Expand Nested-wells to full pixel
  - To suppress back gate effect
  - To evaluate shielding of digital part
  - But large Cd due to BNW/BPW junction
- More BNW contacts
  - BNW ~10KΩ/□
- A few bugs fixed

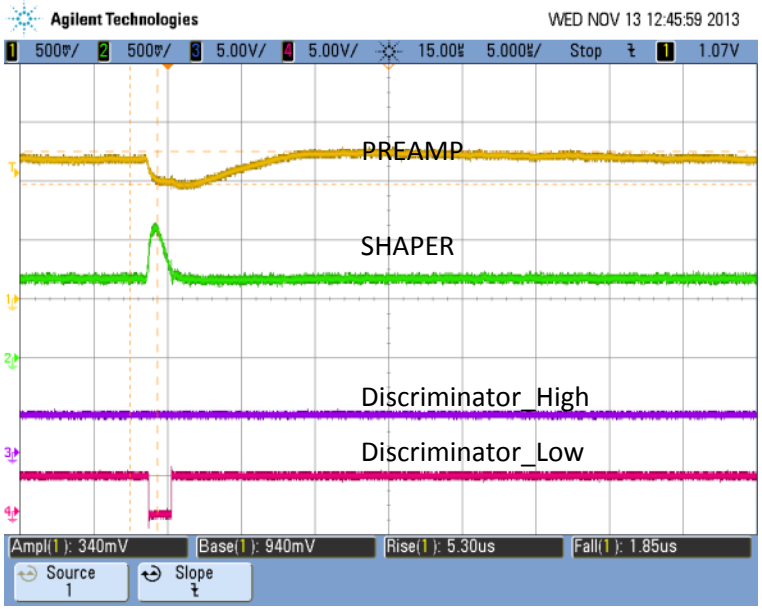




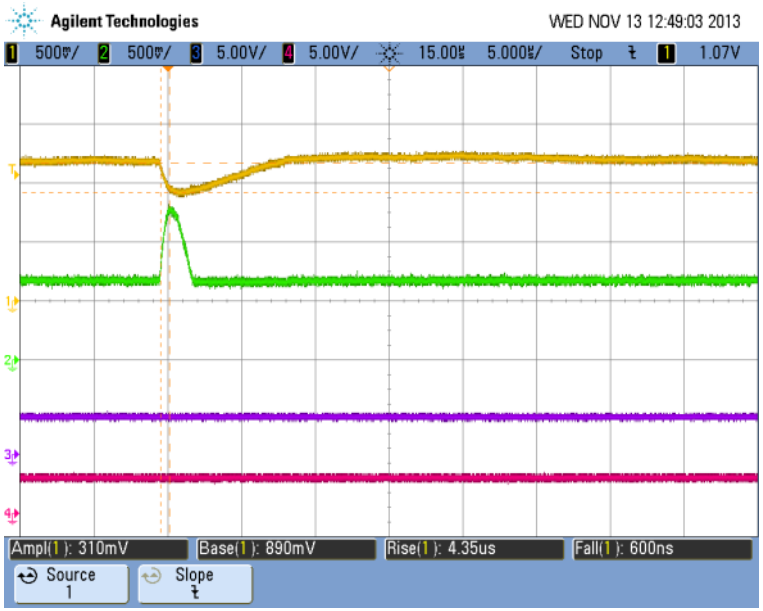
CPIXTEG2 pixel layout
CPIXTEG3 pixel layout

Measurement of crosstalk from discriminator

- Repeated all results on CPIXTEG2
- And found more:
  - Discriminator crosstalk if overlapped with nested-wells



Disable Disc.
via VH2



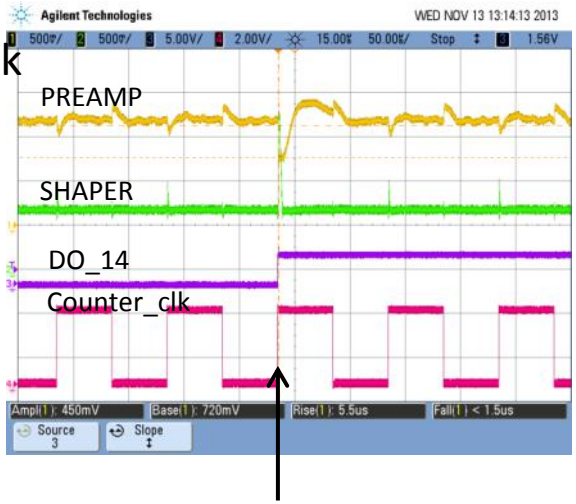
1. Charge Injection with Discr. working

Vtest = 600mV;
VL_AMP_N = 280mV;
Vdet = +5V

2. Charge injection with Discr. stopped

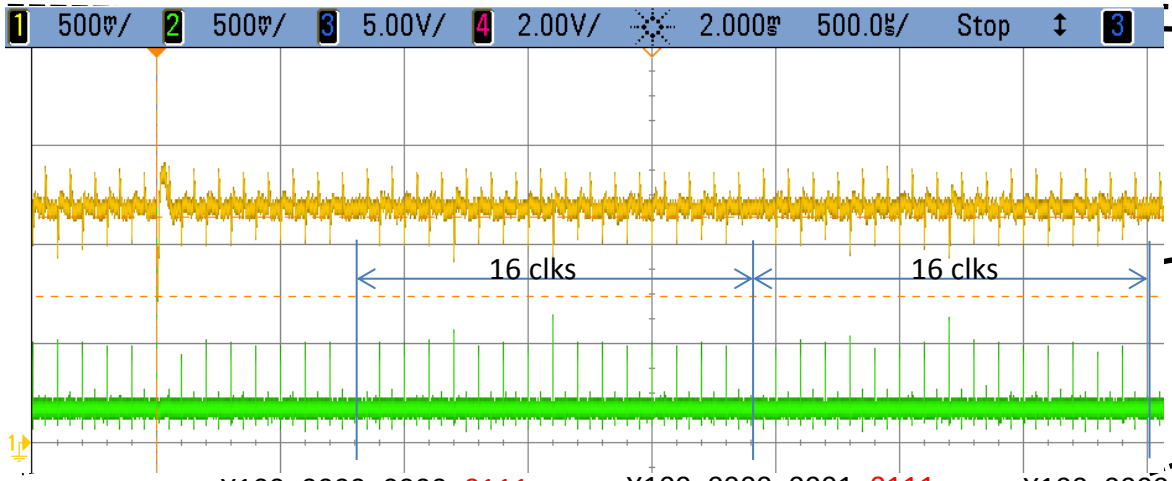
Measurement of crosstalk from counter

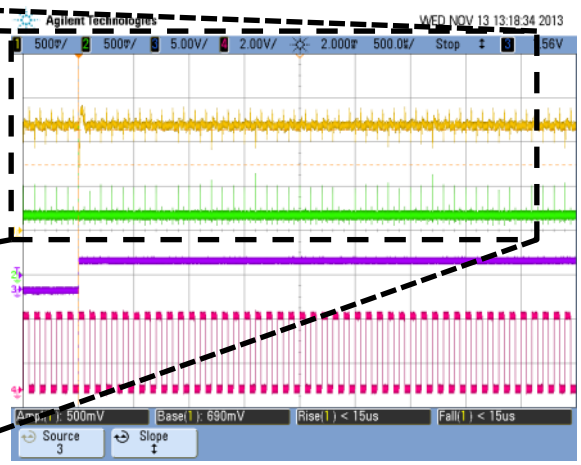
- Counter driven by external clock
  - Watch the analog output
- Counter crosstalk large
  - Clearly pattern related
  - Largest on the transition between all 1's and all 0's
  - Varing Vbnw and Vback, no change
- Not sufficient shielding



X011_1111_1111_1111
→X100_0000_0000_0000

X111_1111_1111_1111
→X000_0000_0000_0000





X100_0000_0000_0111
→X100_0000_0000_1000

X100_0000_0001_0111
→X100_0000_0001_1000

X100_0000_0010_0111
→X100_0000_0010_1000

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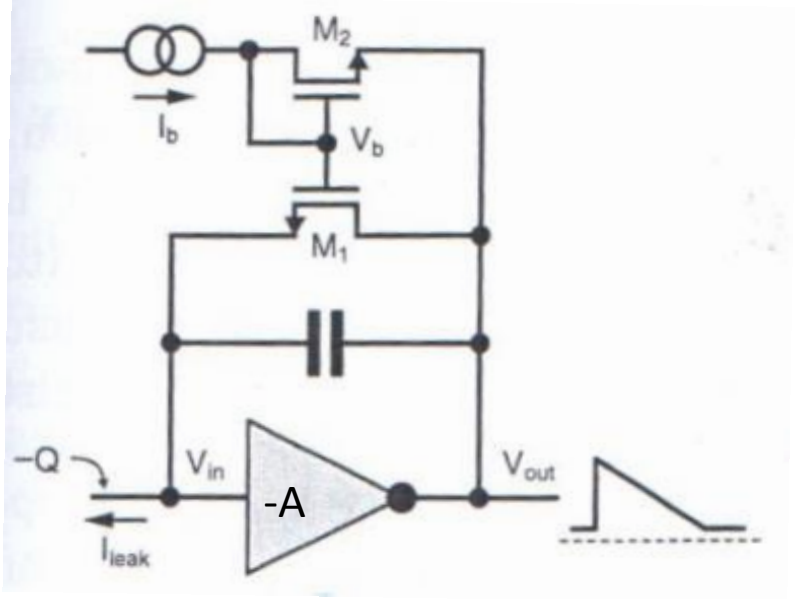
Design consideration for CPIXTEG3b

- A constant feedback current scheme adopted
  - The krummenacher scheme would fail due to mismatch of current mirrors.
- Diode-biased-inverter discriminator
  - Narrow threshold spreading reported
- Cut the pixel smaller
  - 2->1 discriminator
  - 16->6 bits counter
  - 10->6 bits register
  - 64um->50um pixel pitch
- New shielding scheme based on DSOI process
- Larger pixel array
  - 64*64

Constant Current Feedback

- A constant current feedback used for Preamp and Shaper
  - High gain amplifier in the core
  - M1 in linear region and compensate leakage current when no hit
  - M1 in saturation region and discharge C_f by copying I_b after a hit
  - Avoid the risk of failure as in the krummenacher scheme
- Used in the ATLAS FEI pixel chips

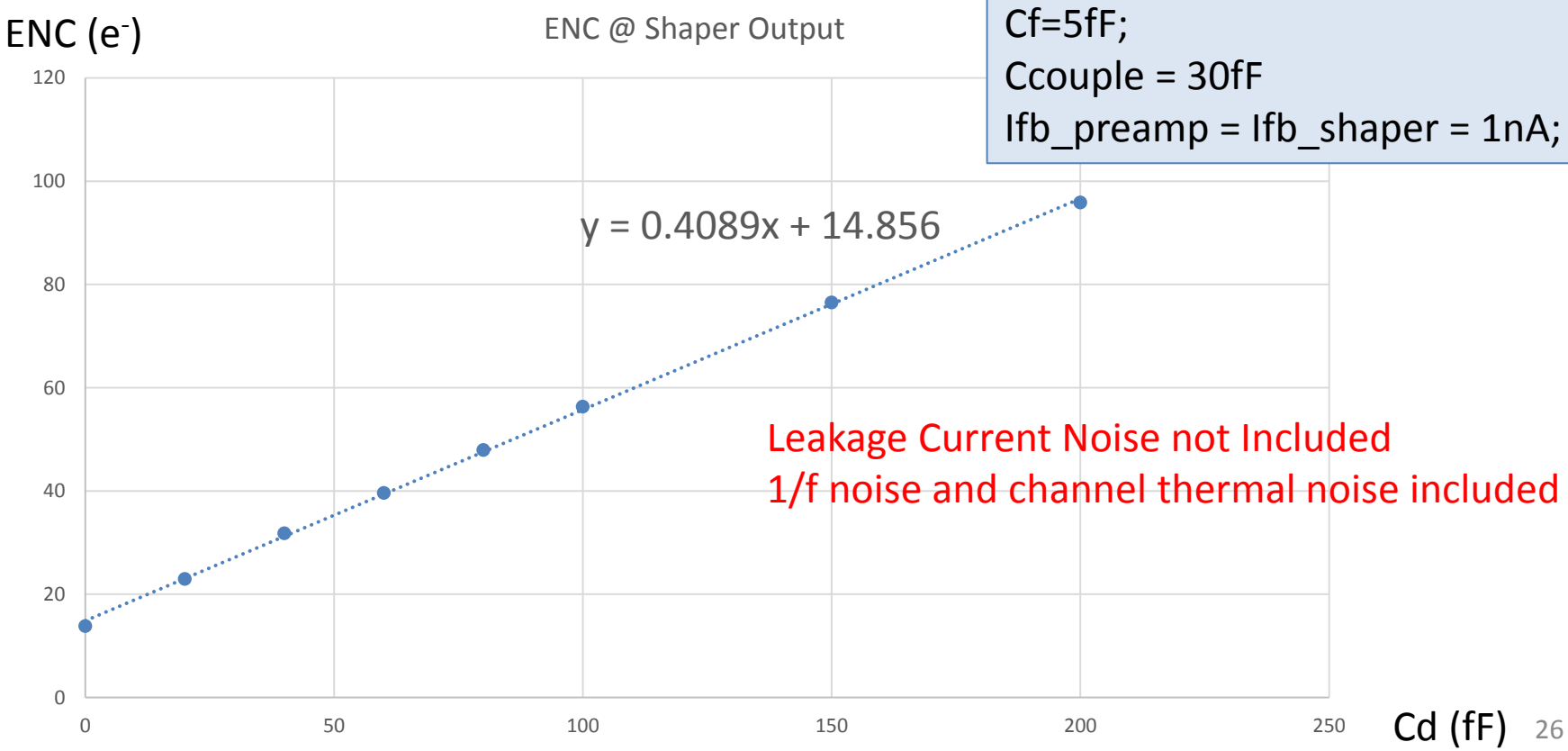
A constant current feedback scheme



Noise analysis by HSPICE simulation

- Noise @ PREAMP Output
  - n_o = 1.4mV
  - equivalent to 70 e^-
- Noise @ SHAPER Output
  - n_o = 6.8mV
  - equivalent to 57 e^-

Cd=100fF;
Cf=5fF;
Ccouple = 30fF
Ifb_preamp = Ifb_shaper = 1nA;

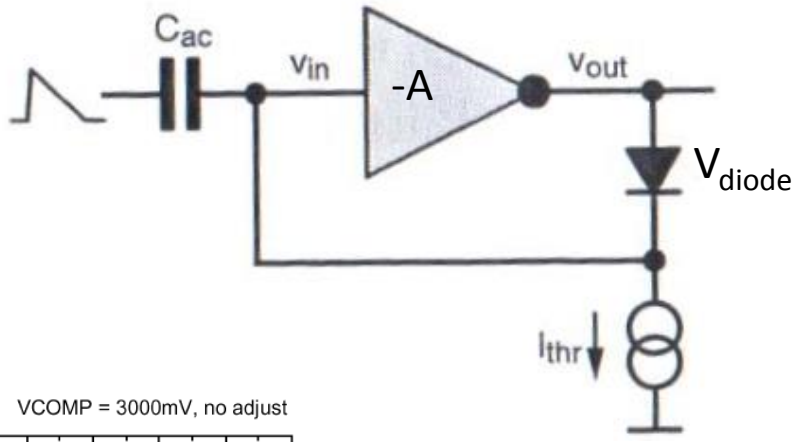


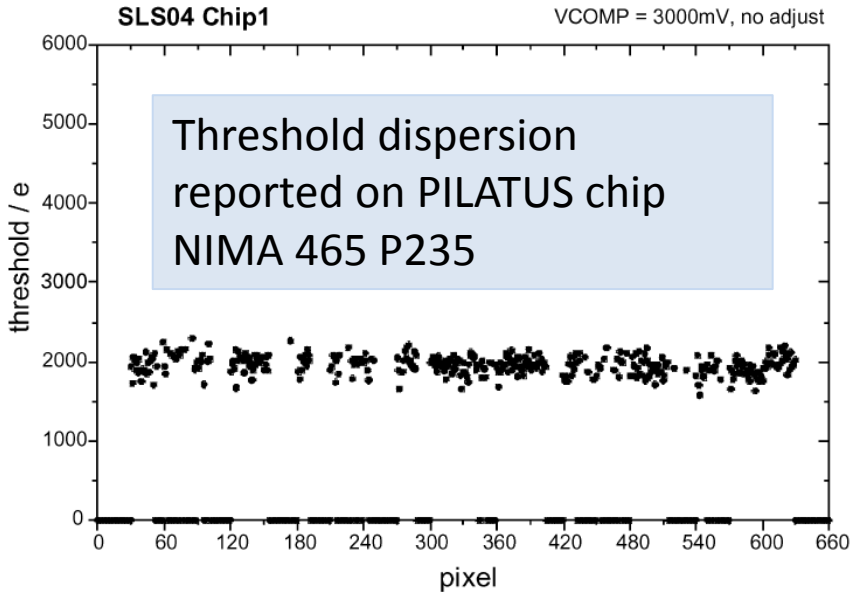
Leakage Current Noise not Included
1/f noise and channel thermal noise included

Diode-biased-inverter discriminator

- AC coupled, baseline of shaper blocked
- Threshold voltages equals V_{diode} /A
  - $I_{thr} = I_s(e^{Vdiode/VT} -1)$
  - $V_T = kT/e$
- Limited range of possible threshold
- Low threshold dispersion
  - 120e without threshold trim reported

Diode-biased-inverter discriminator



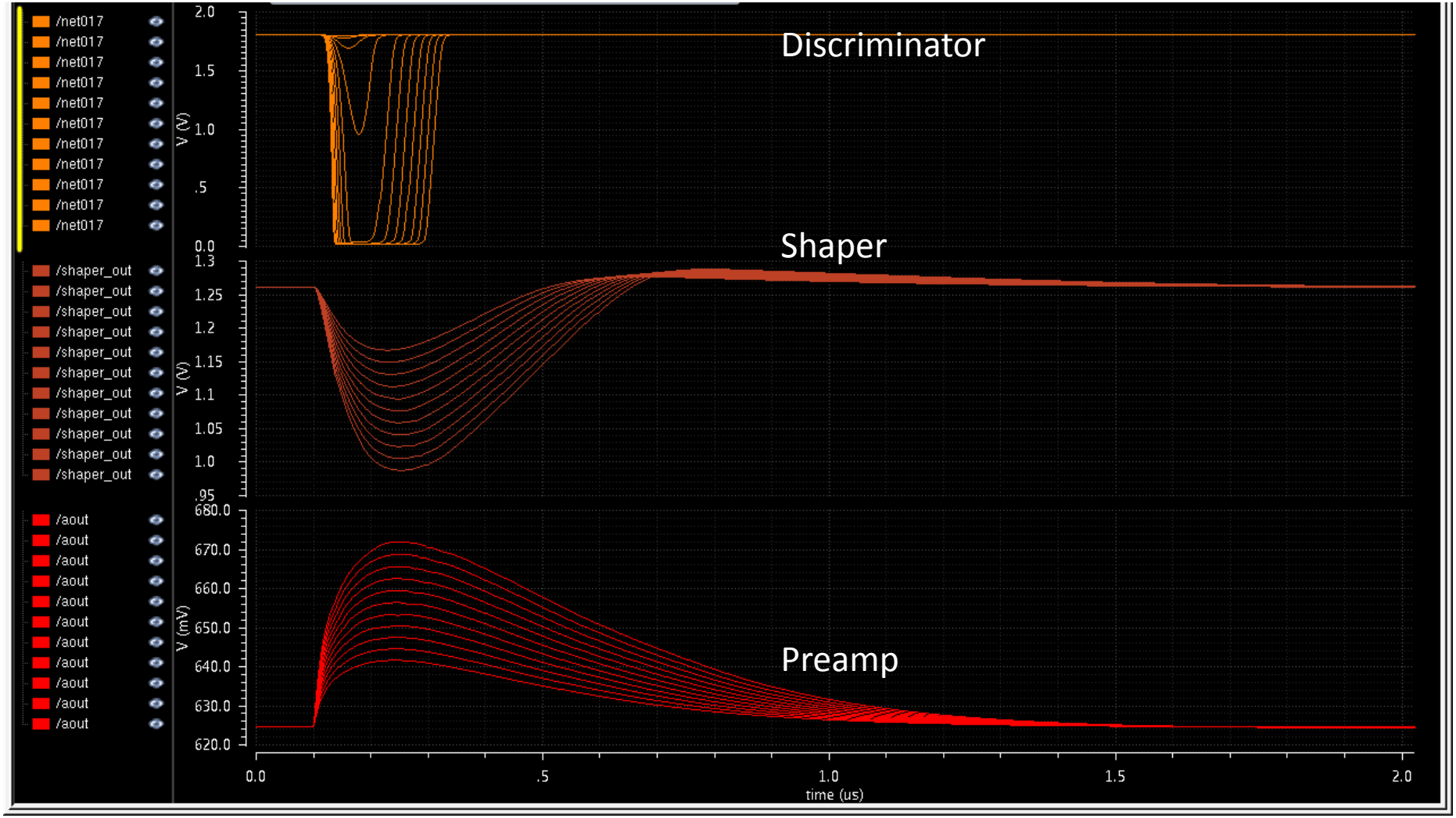


Threshold dispersion reported on PILATUS chip NIMA 465 P235

Fig. 5. The threshold dispersion of the chip, without individual adjustment of the pixels. Zeros arise from pixels with defective SR cells. The rms value of the unadjusted threshold is 120 e^-.

Simulation of PSD system

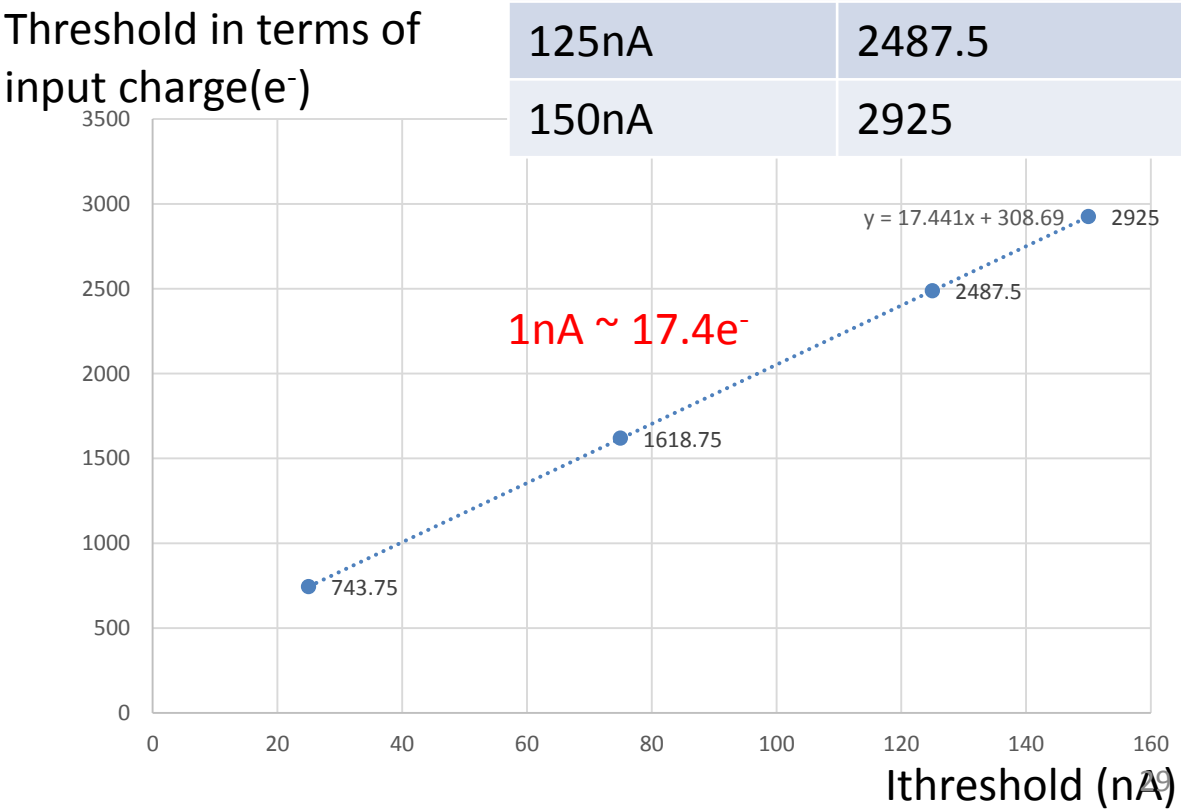
$I_{threshold}$ (I_0) =40nA, input charge = 750e$^-$ to 2000e$^-$



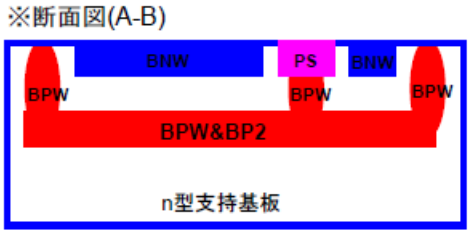
Threshold adjustment

- Simulated Range: 25nA - 150nA
  - 740-2920 e^- in terms of input charge
- $I_{threshold}$ tuning step: 2-5nA
  - 4-bit DAC

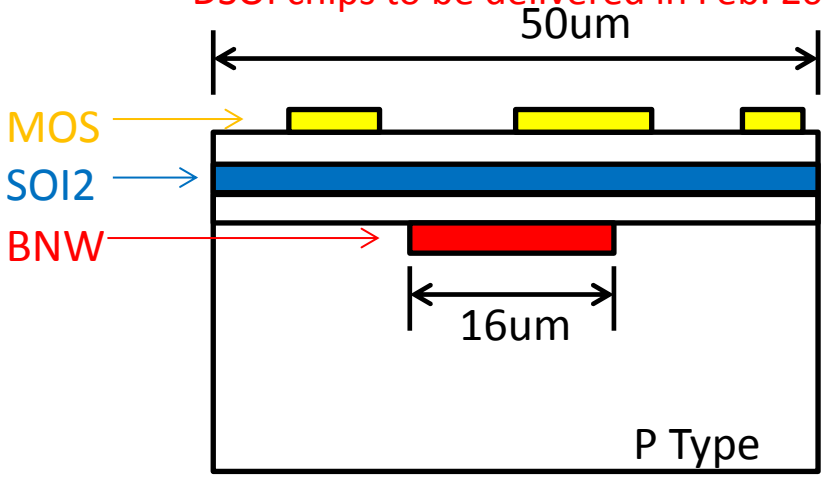
$I_{threshold}$	Threshold in terms of input charge (e^-)
25nA	743.75
75nA	1618.75
125nA	2487.5
150nA	2925



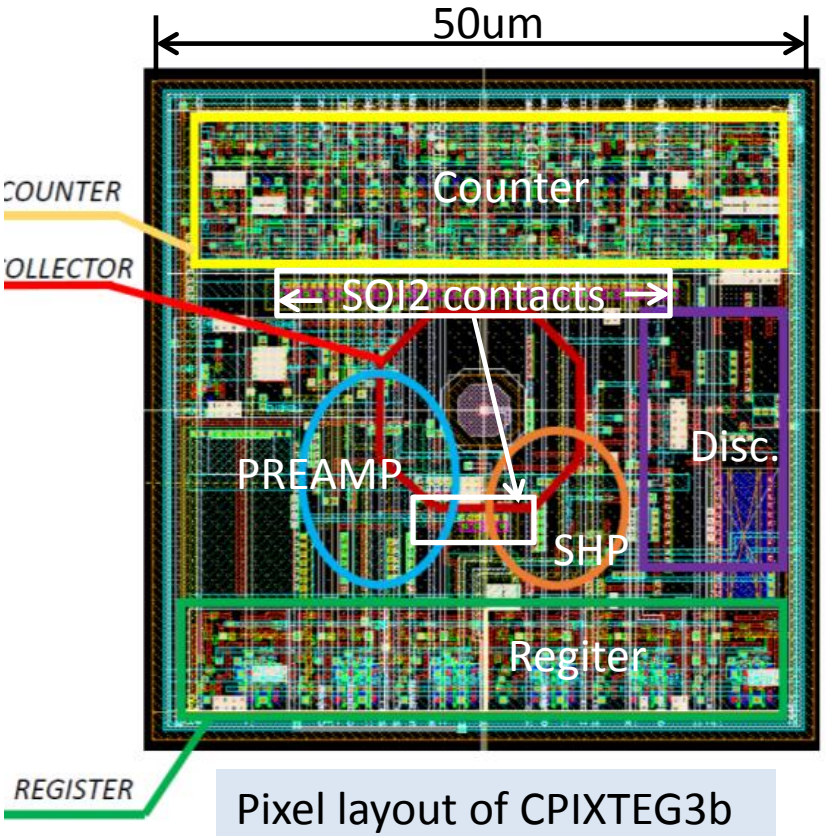
Layout



- New design freedom enabled by DSOI process (compared to Nested-wells)
  - SOI2 covers the full pixel as the shielding layer
  - Charge collection electrode overlaps with Preamp & SHP only, Cd ~ 100fF
- DSOI contacts in between counter and collection electrode.
  - 170kΩ/□ SOI2 layer
- Local bypass capacitors
  - Analog and digital power line
  - SOI2 shielding line
- Backgate/Shielding/Cd/CCE
  - First chips delivered on normal SOI wafer
  - DSOI chips to be delivered in Feb. 2015



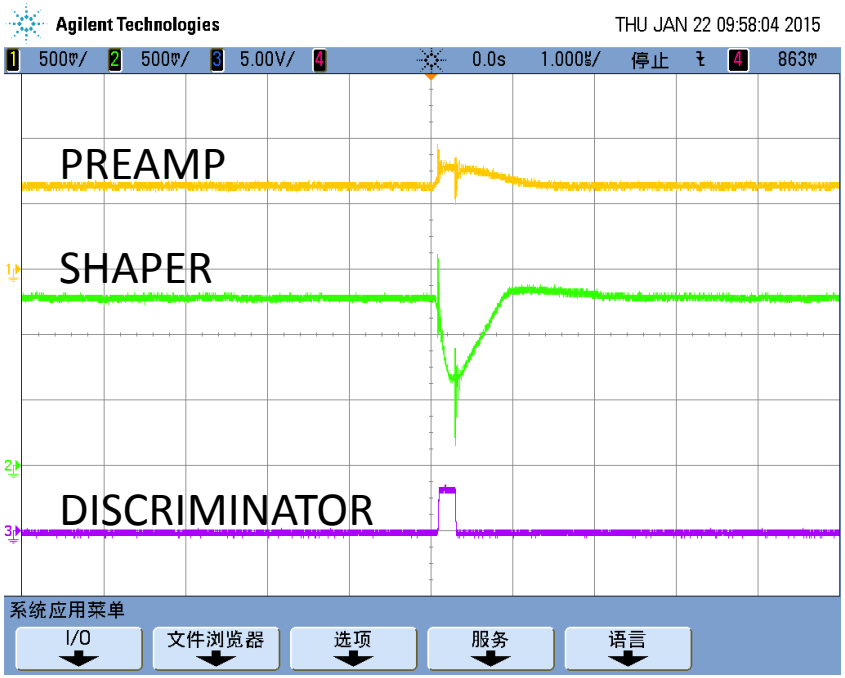
Single pixel in cross section



Pixel layout of CPIXTEG3b

Pixel Circuit without sensor connected(1)

- The new Amp-Sha-Disc system proved working!
  - Safe to dismiss the glitches which were caused by output buffer



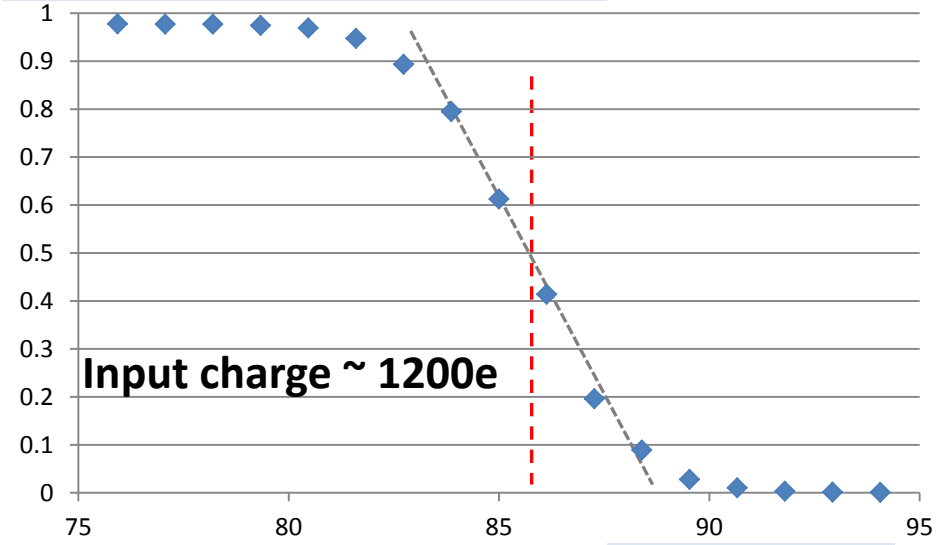
Vtest_pulse = -200mV equivalent to ~4800e$^-$

Ithreshold = -113nA equivalent to ~ 2000e$^-$

Pixel Circuit without sensor connected(2)

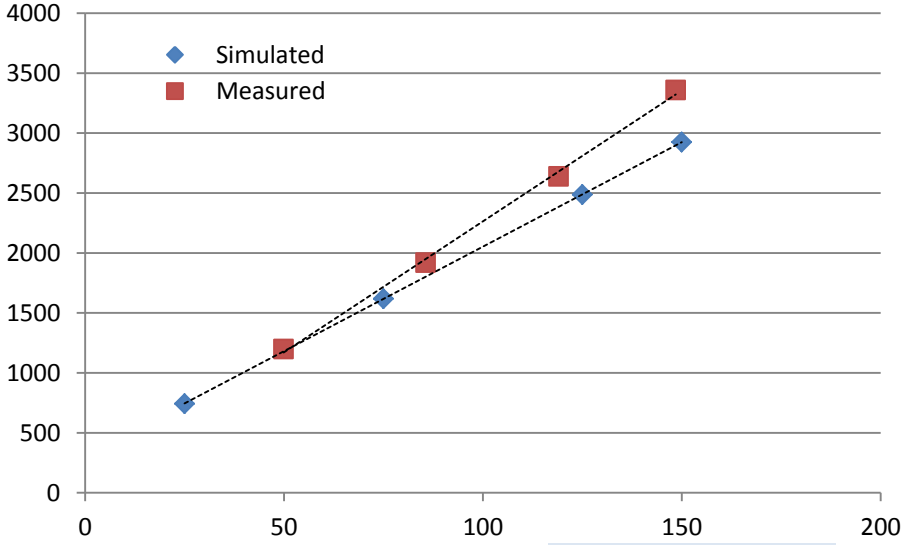
- S-curve measurement
  - Noise
  - Threshold in terms of input charge
- Noise of analog system without sensor connected($C_d \sim 0$)
  - ~27e^-, consistent with simulation
- Measured threshold agreed with simulation
  - Discrepancy due to different Cd and variation of Gain

# of test pulses passed discrimination (normalized)



$I_{threshold}$(nA)

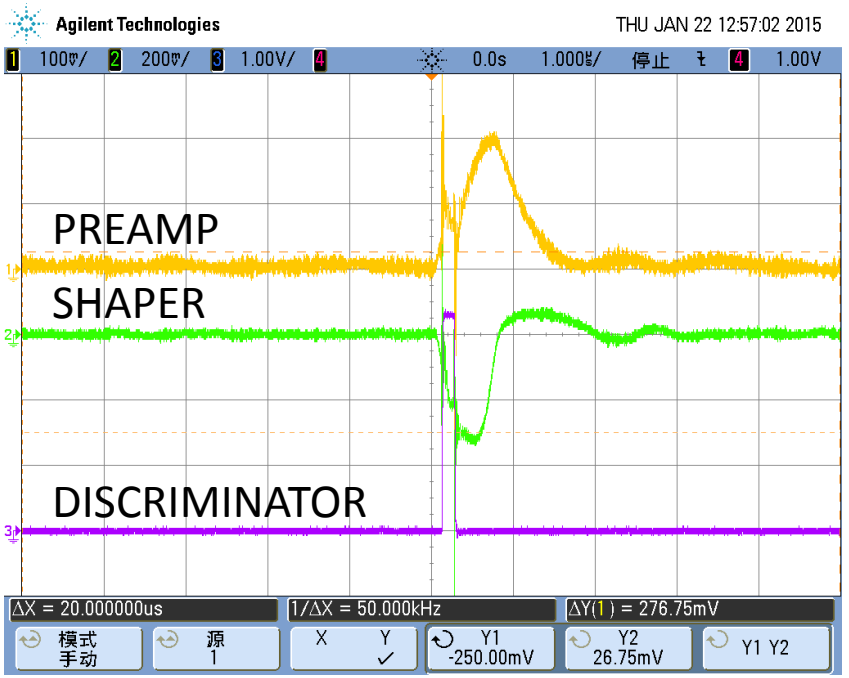
Threshold in terms of input charge(e^-)



$I_{threshold}$(nA)

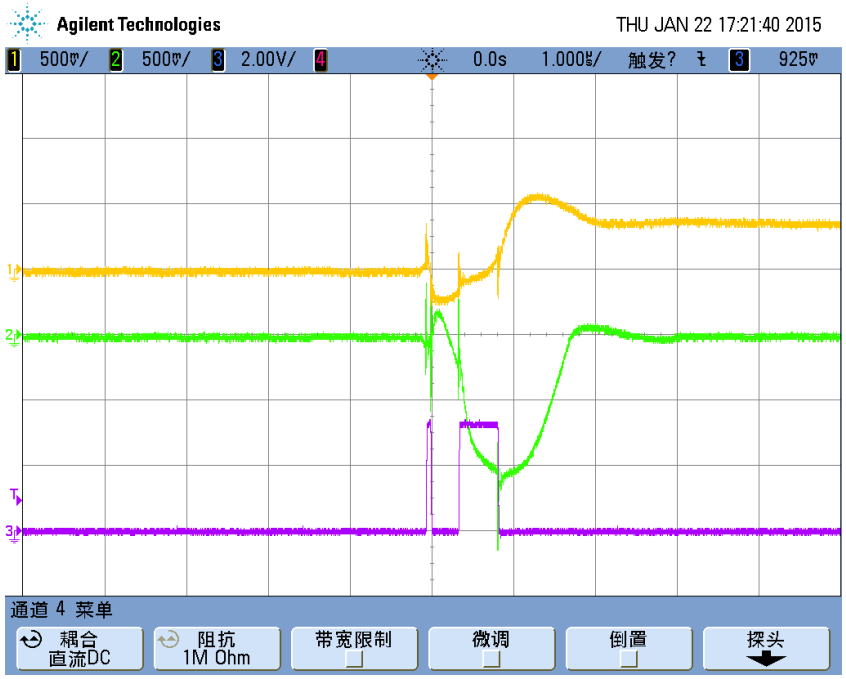
Pixel Circuit with sensor connected(1)

- Managed to operate the circuit with sensor connected (No shielding at all!)
  - Vb = -4.2V
  - Vgain of shaper decreased andstopped oscillation.
  - Input charge ~10ke$^-$
  - Counter off



Vtest_pulse = 400mV, Ifb_shaper = -10nA
Counter off

Pixel Circuit with sensor connected(2)

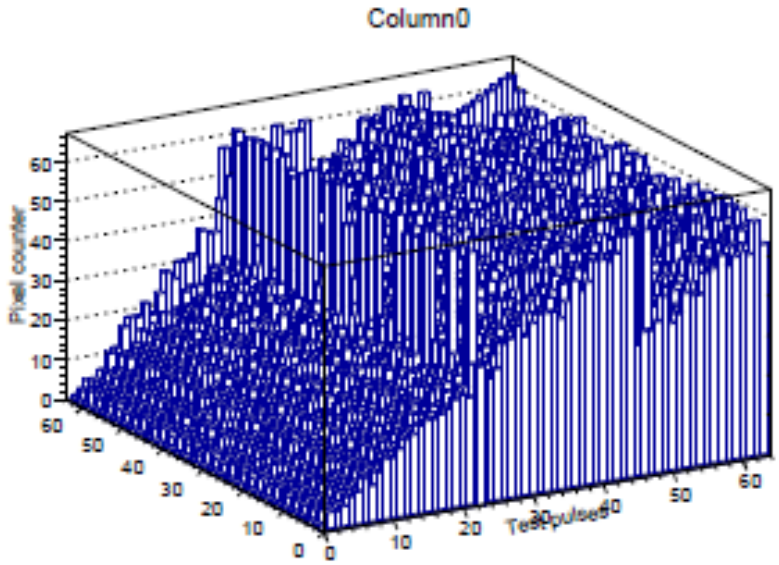


Counter transition:
63->0

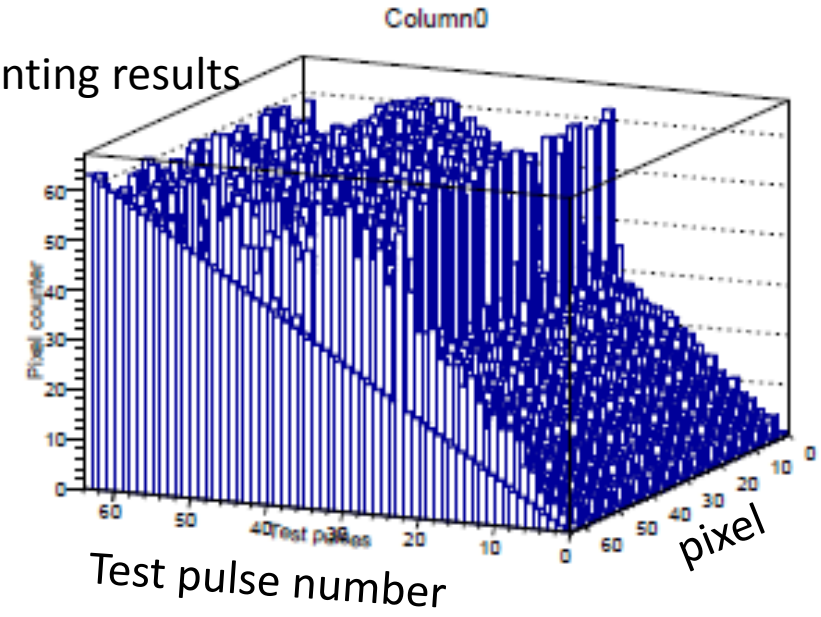
- Amplitude of crosstalk is related to the pattern of counter
  - Input charge ~ 20ke$^-$
  - The worst case is all 1'-> all 0's

Counter transition:
32->33

Counting results of a single column

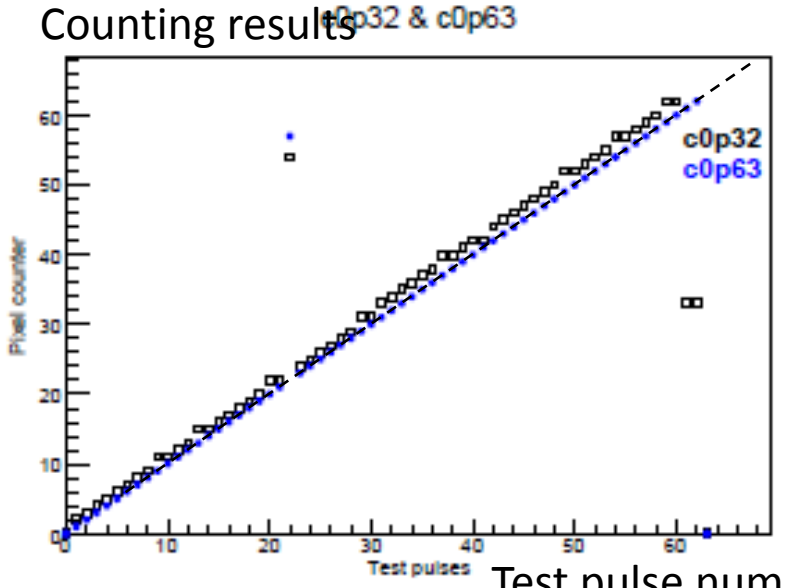


Counting results



Test pulse number

Counting results

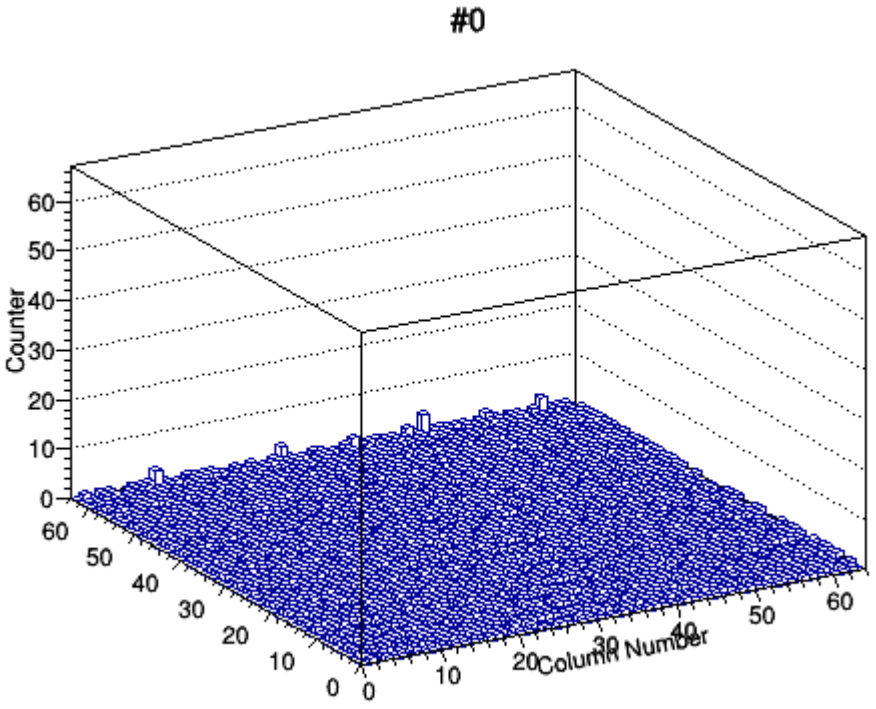


Test pulse number

- Input charge applied to column 0
  - 64 pixels
  - Pixel63 without sensor, counting correctly.
  - Other pixel connected to sensor, a few noise hit recorded.
- Further investigation needed.

Counting results of the whole pixel array

- Input charge applied to the whole pixel array except column 0
  - 64*63 pixels
  - All pixels alive!



Counting results of pulsed laser beam

- Pulsed infrared laser beam
  - 1064nm
  - A few 100ps
  - ~200um in diameter
  - ~pJ/pulse
- Two adjacent pixels responded to the laser stimulus and counted the pulses
  - A proof of principle!

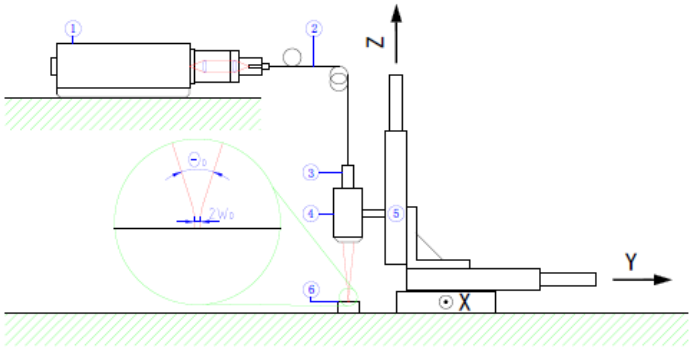
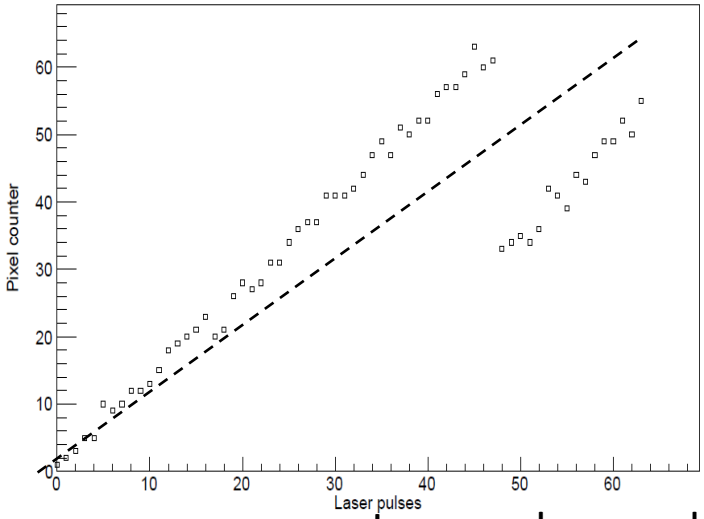
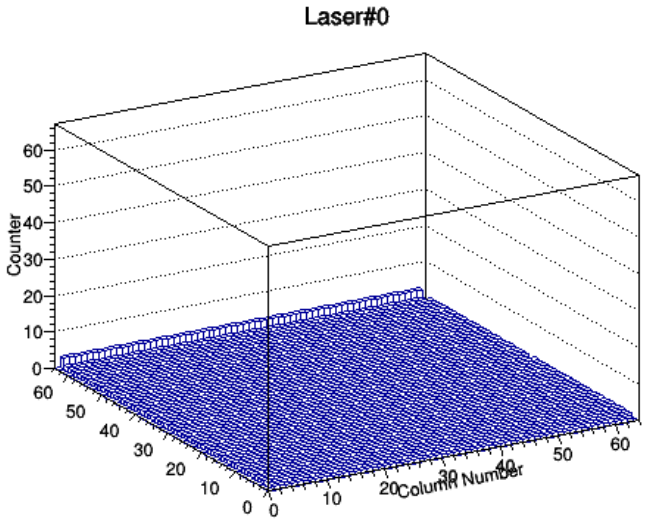


Fig. 2. ① Laser generator, ② optical fiber, ③ collimator, ④ lens, ⑤ 3D linear motion platform, ⑥ detector chip

Counting results c38p29



Laser pulse number



Outline

- Introduction to SOIPIX
- Motivation of Counting Pixel R&D
- Nested-Wells-based design
  - CPIXTEG2 by A-R-Tec
  - CPIXTEG3
- DSOI-based design
  - CPIXTEG3b
- Summary

- Findings & Achievements
  - Nested-wells is effective to shield shaper, but not sufficient to shield counter
  - On-chip circuit works well
  - Obtained very encouraging results of counting laser pulses
  - Firmware and software developed, well prepared for the forthcoming DSOI chips.
- Considerations for further optimization
  - Very compact memory cell developed by Prof. Kurachi is now ready for user.
  - Option of a low power auto-zero comparator as discriminator
  - Option of a SDD-like sensor structure proposed by collaboration members in Shizuoka U.

All efforts point to a counting pixel chip with:
- ✓ 30*30 um^2 pixel size
- ✓ 1k frames/s
- ✓ 14-bit counter
- ✓ Low energy X-ray 2~4 keV

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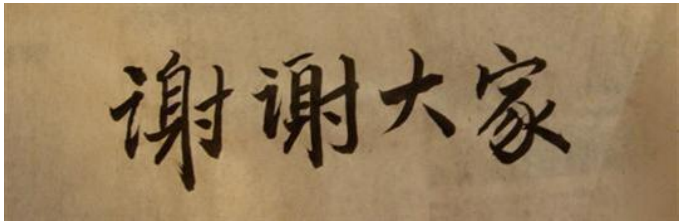
Masao Okihara, Naoya Kuriyama, Noriyuki Miura, Hiroki Kasai (Lapis)

T. Imamura (A-R-Tec)



THANKS FOR YOUR TIME!