IN2P3
Les deux infinis

Omega

ÉCOLE POLYTECHNIQUE
UNIVERSITÉ PARIS-SACLAY

SiGe ROC chips for HEP at OMEGA lab

KEK seminar, つくば市 (日本国)

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OMEGA microelectronics laboratory
Ecole Polytechnique & CNRS IN2P3
http://omega.in2p3.fr
& WEEROC SAS
http://weeroc.com

AIDA 2020

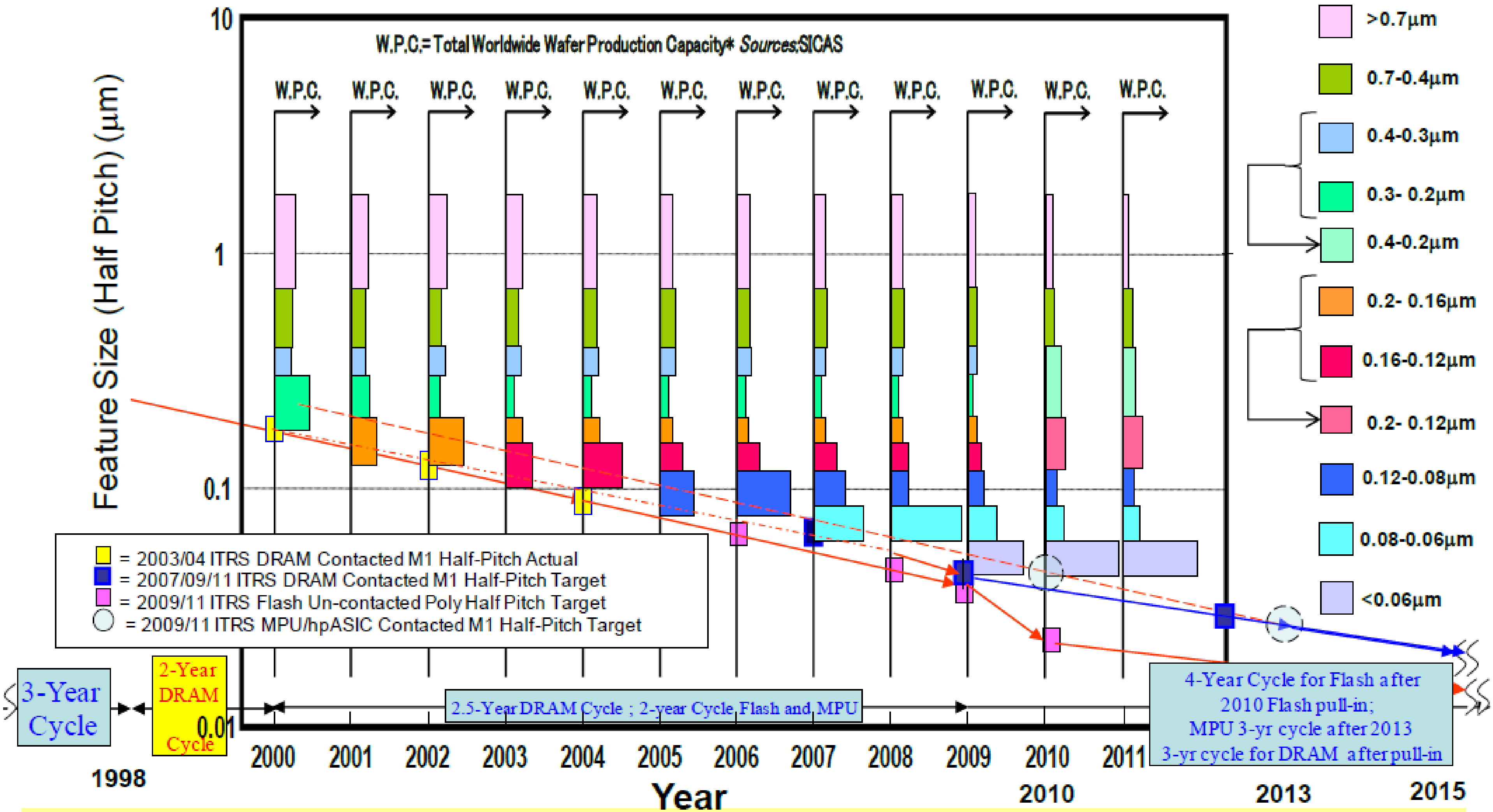
weeroc

Organization for Micro-Electronics desiGn and Applications

Outline

- Evolution of technologies, advantages of SiGe
- Examples of OMEGA chips in SiGe for photdetector readout
- Evolution of SiGe projects

ITRS 2011 roadmap



** Note: The wafer production capacity data are plotted from the SICAS* 4Q data for each year, except 1Q data for 2011. The width of each of the production capacity bars corresponds to the MOS IC production start silicon area for that range of the feature size (y-axis). Data are based upon capacity if fully utilized.*

http://www.itrs.net/Links/2011ITRS/2011Chapters/2011ExecSum.pdf

MOS and Bipolar

© K. Troki (CMP)

Example of prices, prototyping

CMOS	.35 µ	AMS	650 €/mm^2
CMOS opto	.35 µ	AMS	810 €/mm^2
CMOS HV	.35 µ	AMS	1000 €/mm^2
CMOS	130nm	ST	2200 €/mm^2
CMOS	65 nm	ST	7500 €/mm^2
CMOS	40 nm	ST	15000 €/mm^2
SiGe BiCMOS	.35 µ	AMS	890 €/mm^2
SiGe:C BiCMOS	130nm	ST	3500 €/mm^2
SOI	130nm	ST	4000 €/mm^2
SOI	65nm	ST	9500 €/mm^2
Poly-SOI-Metal	MUMPS	MEMSCAP	3700 €/cm^2

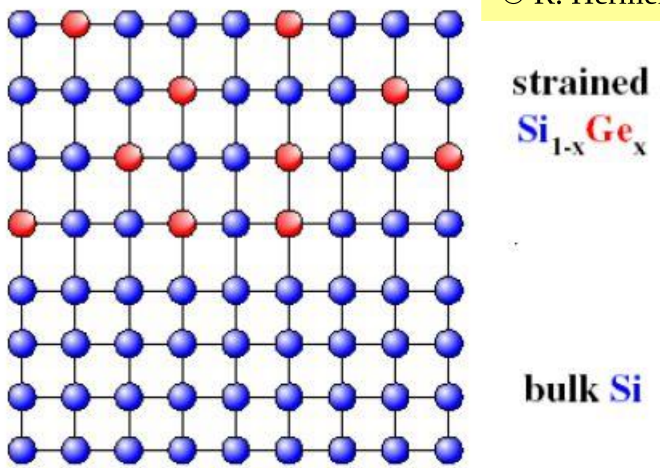
CMP annual users meeting, January 20th 2011, PARIS

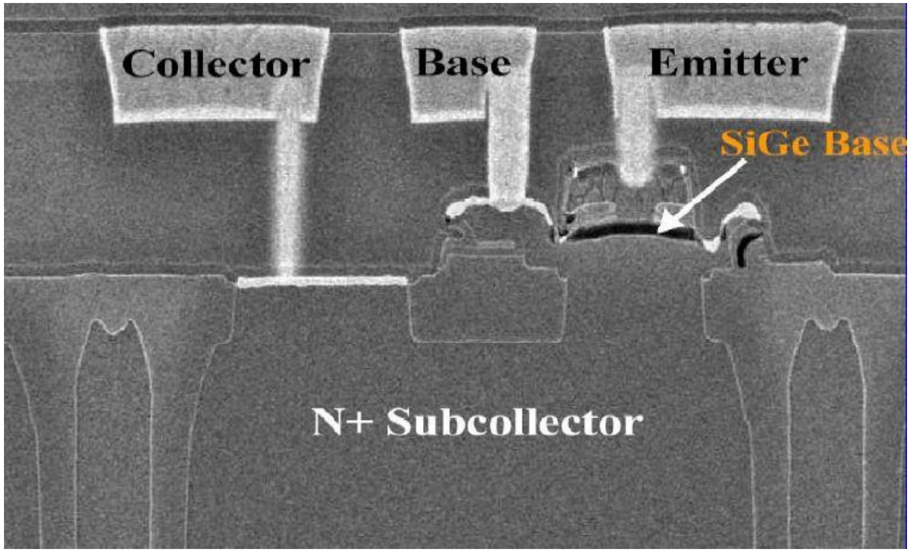
http://cmp.imag.fr/aboutus/slides/Slides2011/02_Runs_2011.pdf

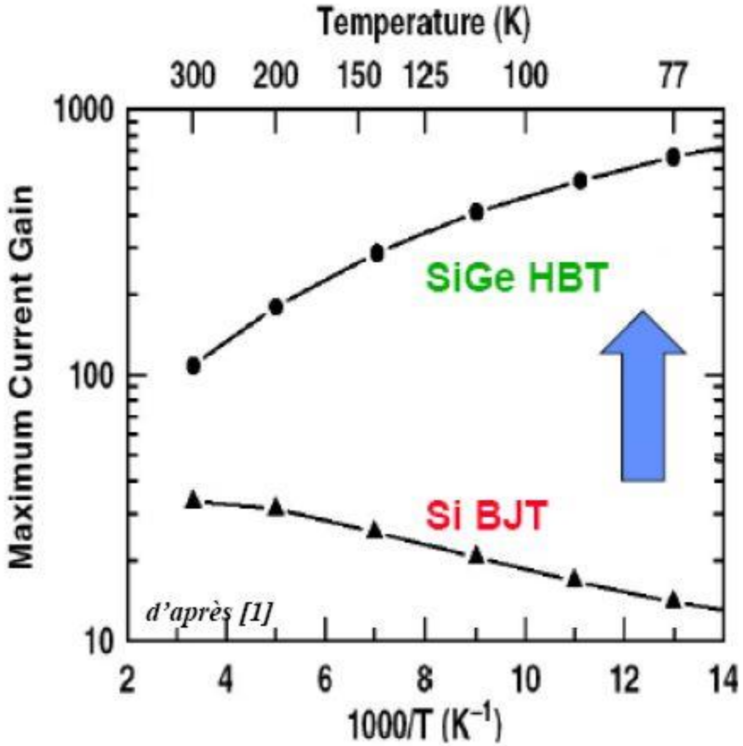
SiGe technology

- Faster bipolar transistors for RF telecom
  - Better mobility and FT
  - Better current gain (beta)
  - Better Early voltage
  - Interesting improvement at low T
  - Compact CMOS (0.25 or 0.35µm) for mixed-s

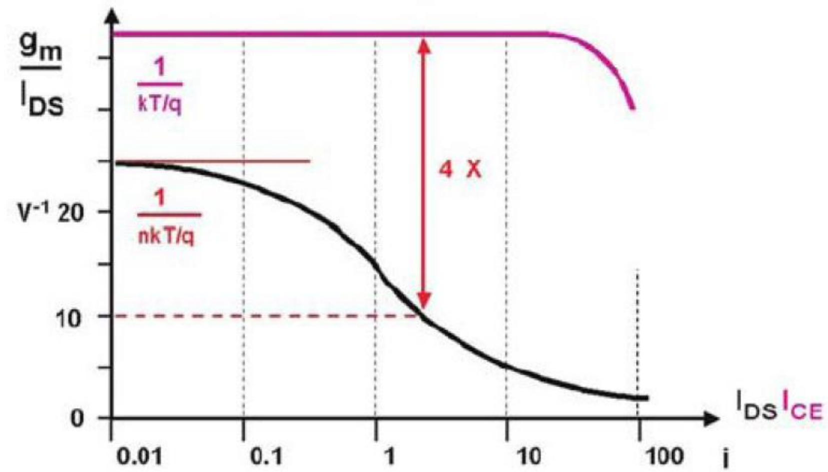
© R. Hermel

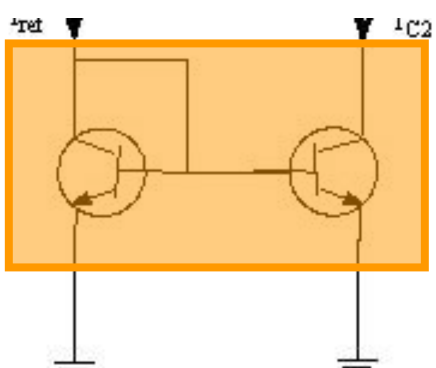


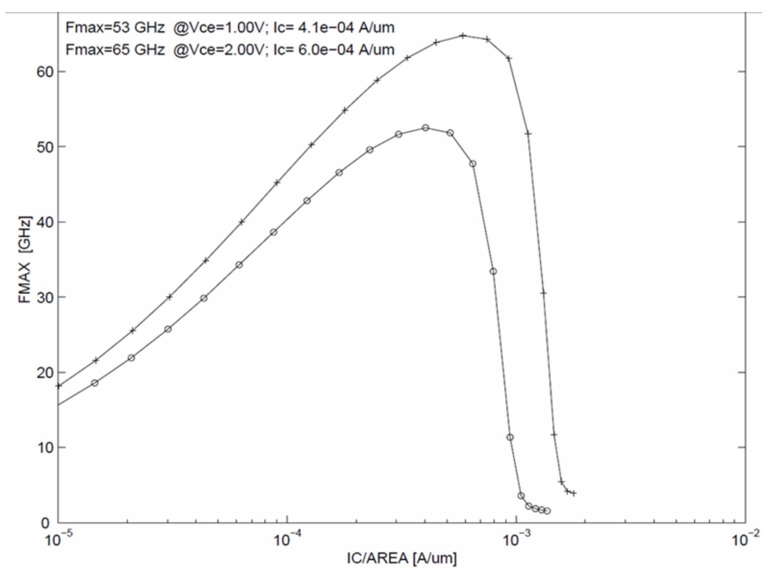




- BJT : best g_m /I ratio (1/U_T)
  - Large transconductance with small devices
- Speed goes as $F_T = g_m / 2\pi C$
  - C~10 fF g_m typ mA/V
  - F_T ~60 GHz for SiGe 0.35µm
  - Interesting for fast preamps
- Not forgetting 100V Early voltage and matching performance (A~mV*µm)
- $V_{BE} = V_T Ln(I_C/I_S)$
- Large swing : V_{CEsat} ~3 U_T







Evolution of technologies in practice

- Performant design is at transistor level
- More and more functions are integrated inside chips (ASICs)
- Evolution of technologies make them more and more performant but more and more complex

10 ans d'évolution des spécifications techniques pour la réalisation d' ASIC

Design Groups – Current Status

design groups ≈ 30-40

active designs ≈ 30-40

… NOvA APV25 … MAPS POM
3D FSSR2 ASDQ PACIFIC ICECAL
FE-I5 CBC LBNE VMM CLARO MAROC3
KPIX nEXO LAPAS ASDCDC SAMPA
BEAN QIE ABC … SAO3 VELOPIX
CLIC TARGET ISR3B SALT …

Average one design per group

- institutions leading collaborative efforts
- institutions performing R&D on technologies

One FE-ASIC design currently requires
2-4 full-time designers and 2-4 years

average, from concept to ready-for-production

Design Groups – Current Status

In order to be **efficient** and maintain **state-of-the-art** ASIC groups must:

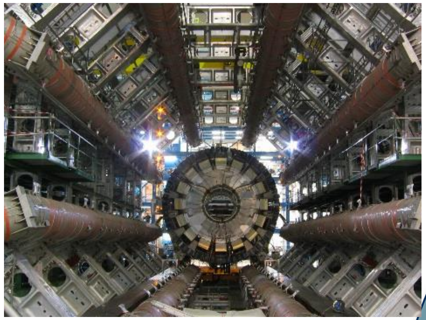
- develop **1-2 new designs** and 2-4 revisions per year
- work with **2 technologies** (re-usage & next)
- perform **R&D** on circuits and technologies

The **critical minimum** is currently **5-6 designers**

Need to **diversify** while contributing to PP with an average of 25-30 % of resources

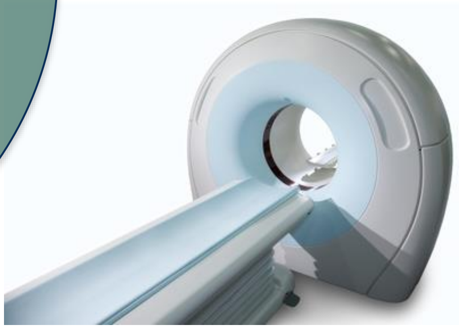
PP currently supports/uses up to **25-30 %**

Omega microelectronics lab



Research,
Institute

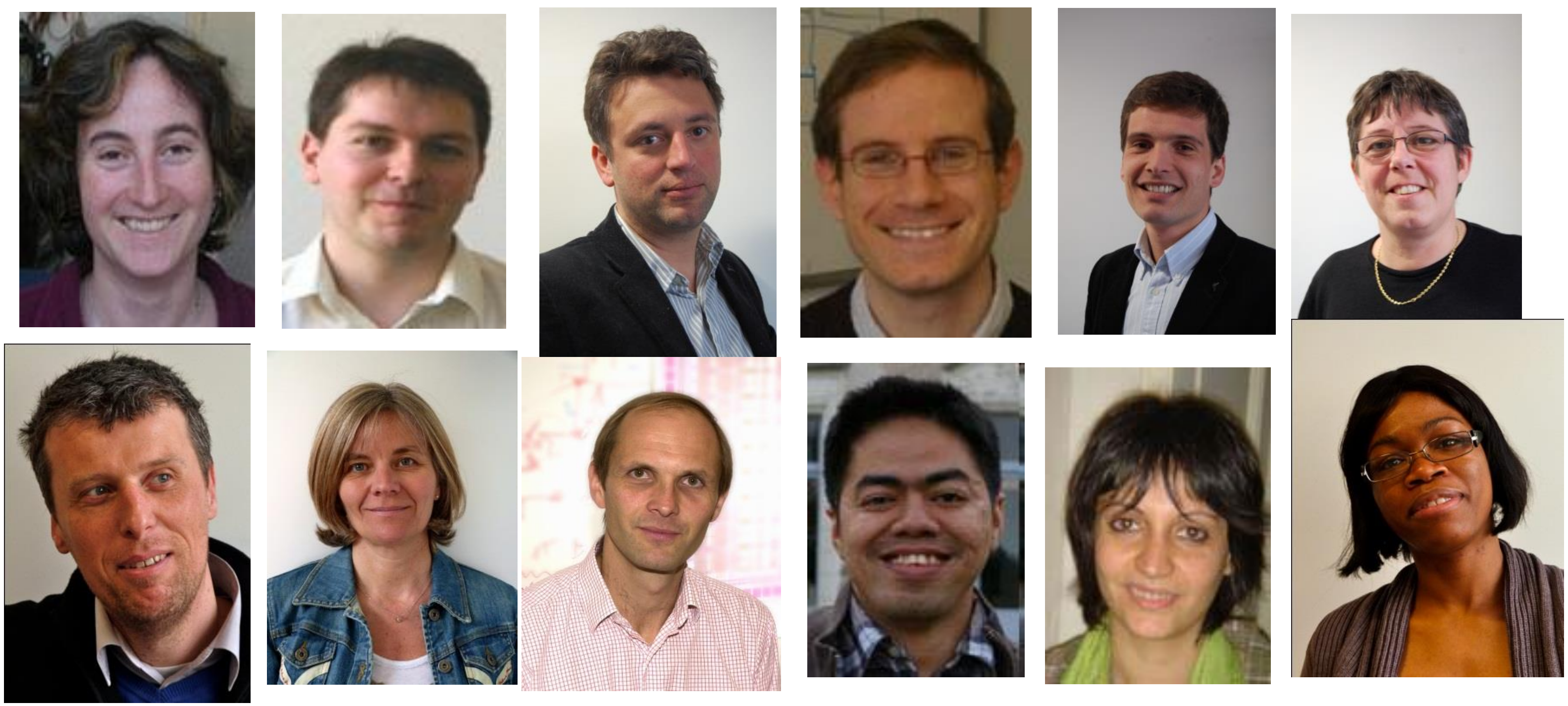
Education
School



Industry, company

OMEGA laboratory

- Mutualized ASIC design team
- 10 research engineers (1 IR0, 2 IR1, 6 IR2, 1CDD), 2 pHD students
- Importance of critical mass for more and more complex circuits
- Cross-fertilization between projects
- Technology transfer via startup WEEROC

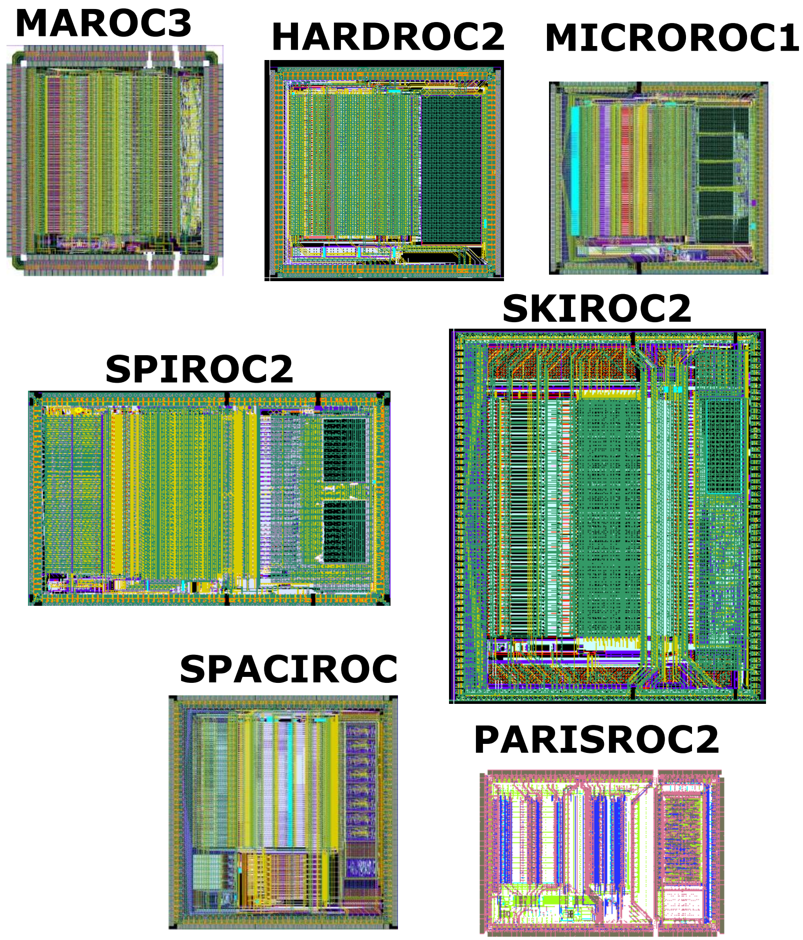


OMEGA ROC chips

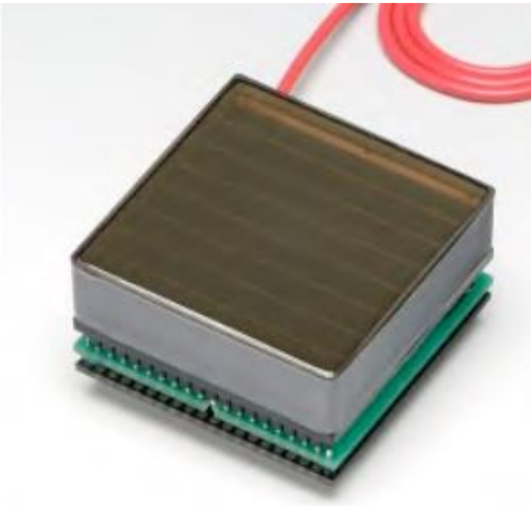
- Use of Silicon Germanium 0.35 µm BiCMOS technology since 2004
- Readout for MaPMT and SiPM for ILC calorimeters and other applications
- Very high level of integration : System on Chip (SoC)

Chip	detector	ch	DR (C)
MAROC	PMT	64	-2f-50p
SPIROC	SiPM	36	+10f-200p
SKIROC	Si	64	+0.3f-10p
HARDROC	RPC	64	-2f-10p
PARISROC	PM	16	-5f-50p
SPACIROC	PMT	64	-5f-15p
MICROROC	µMegas	64	-0.2f-0.5p
PETIROC	SiPM	32	50fC-300pC

http://omega.in2p3.fr

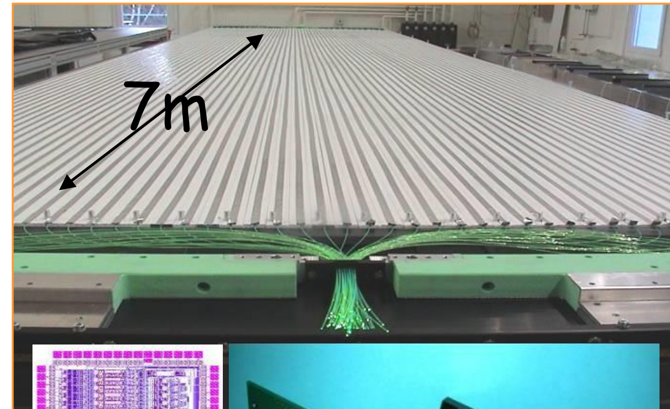


- MAROC
- SPACIROC
- PARISROC

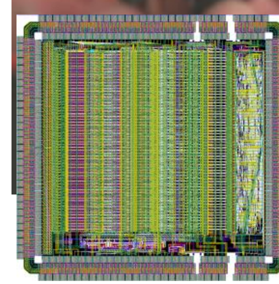


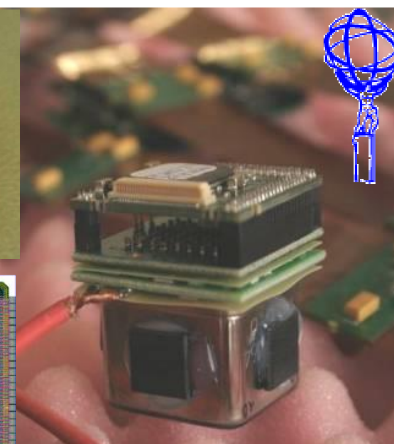
MAROC for MAPMT

- Started with OPERA_ROC (2001)
  - 32 Channels in BiCMOS 0.8 µm
  - 3000 chips produced in 2002
  - Readout OPERA Target tracker in Gran Sasso
- MAROC1 (2004)
  - First prototype with 64 channels
  - AMS SiGe 0.35 µm (12 mm^2, Pw=5 mW/ch)
- MAROC2 (2006)
  - **1000 chips produced and bonded on a compact PCB for ATLAS luminometer (ALFA)**
- MAROC3 (2009)
  - Lower power dissipation
  - Wilkinson ADC added
  - 1000 chips produced in 2010
- Many applications: Double-Chooz, Menphyno, medical imaging(Valencia, ISS Roma)…



OPERA_ROC

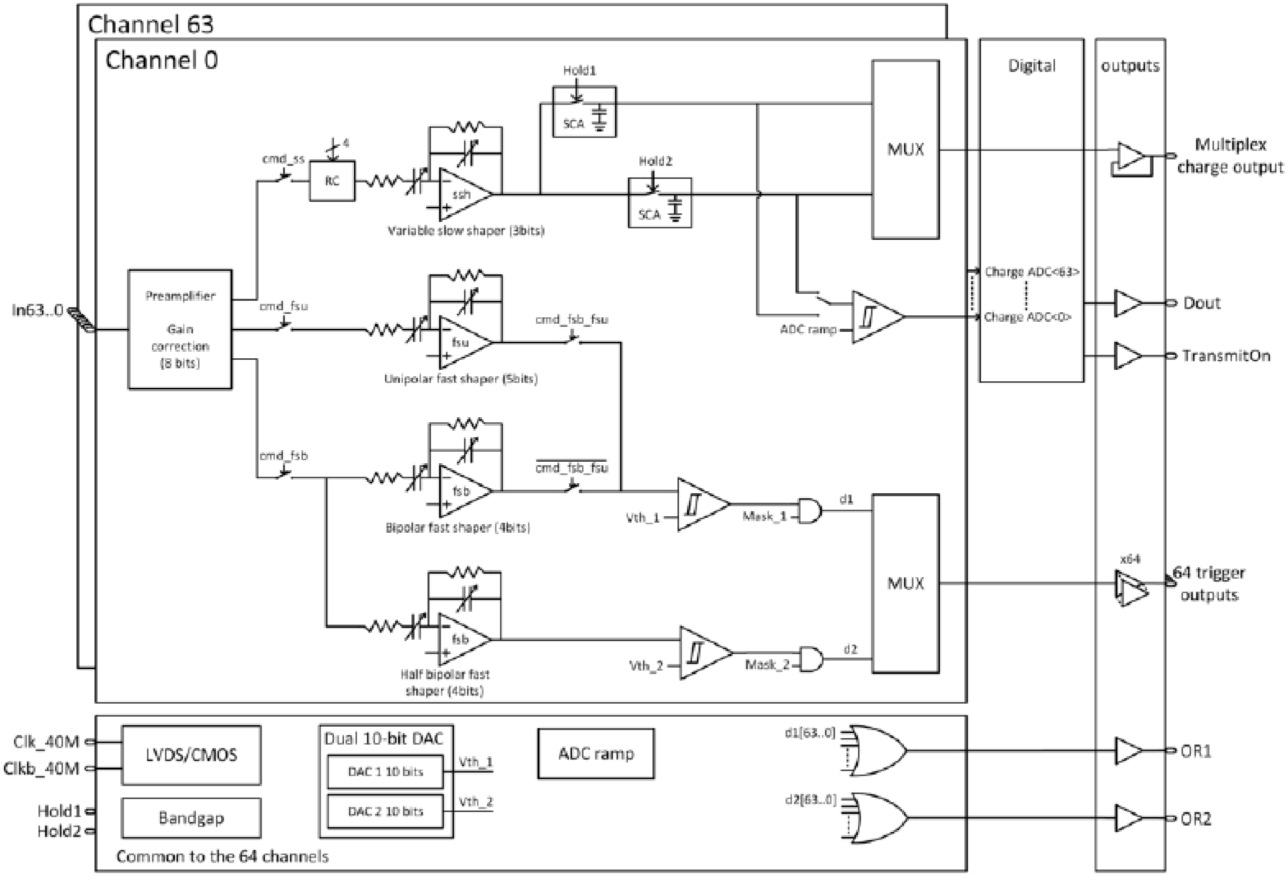


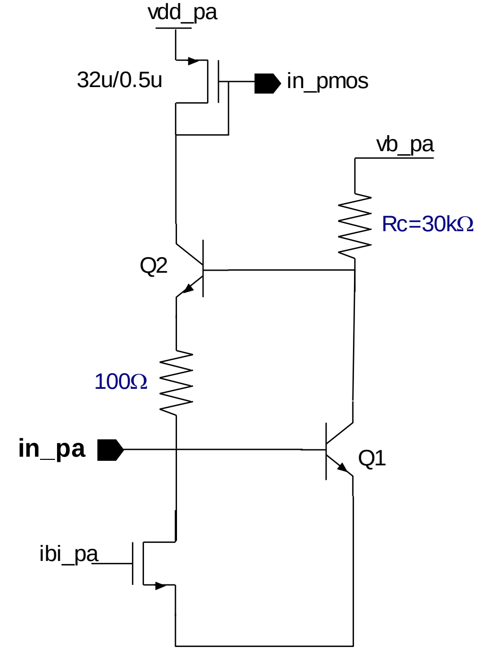


MAROC2

MAROC3 : MultiAnode Read-Out Chip

- Complete front-end chip for 64 channels multi-anode photomultipliers
  - 6bit-individual gain correction
  - Auto-trigger on 1/3 p.e. at 10 MHz
  - 12 bit charge output with internal ADC
  - SiGe 0.35 µm, 12 mm^2, Pd = 5 mW/ch

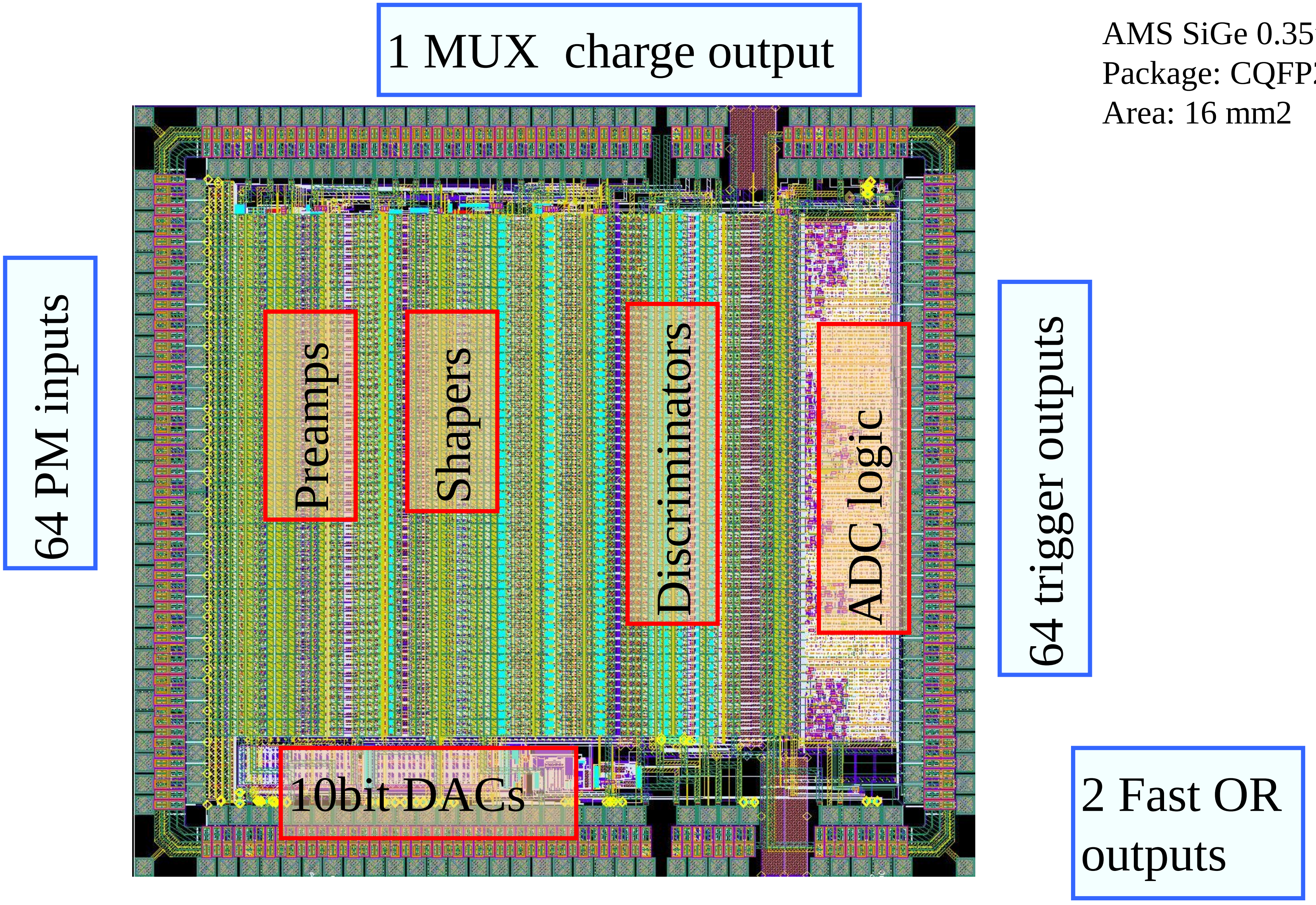




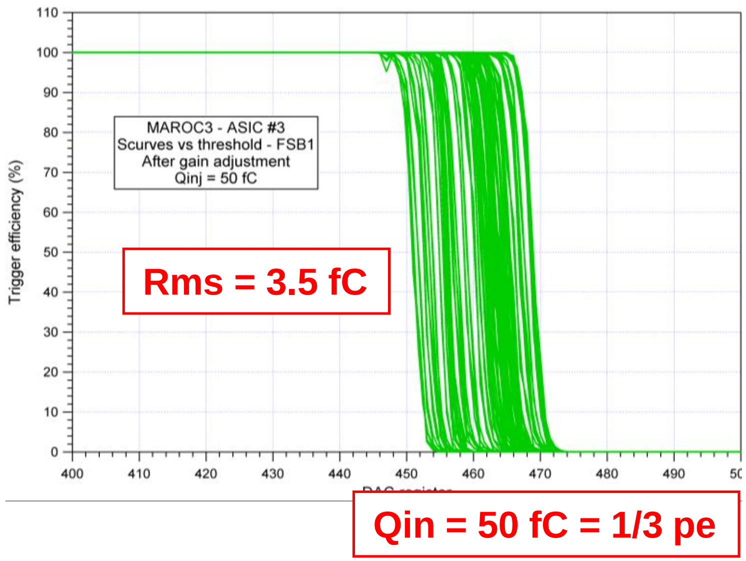
Preamplifier « super-common base »

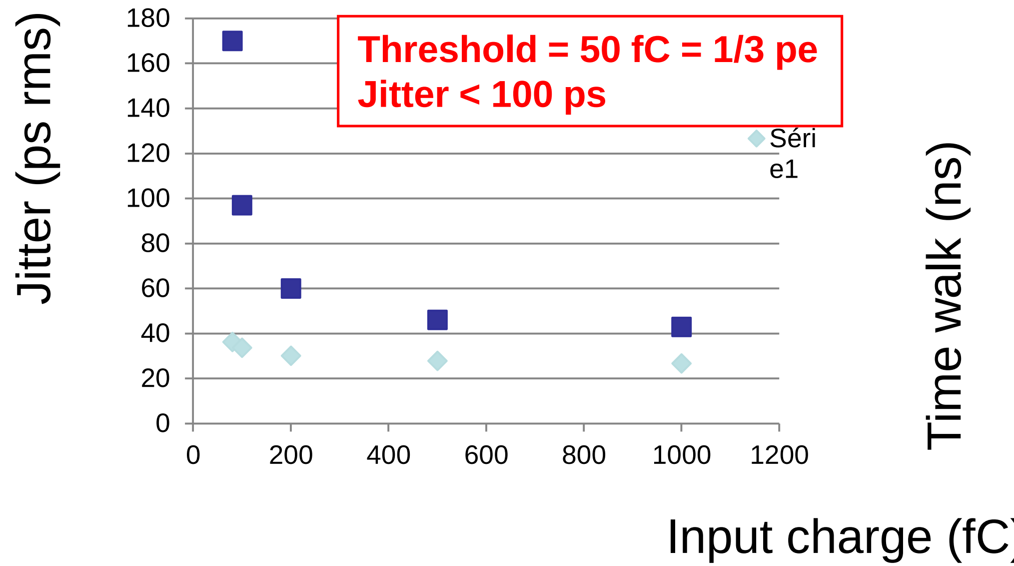
MAROC3 layout

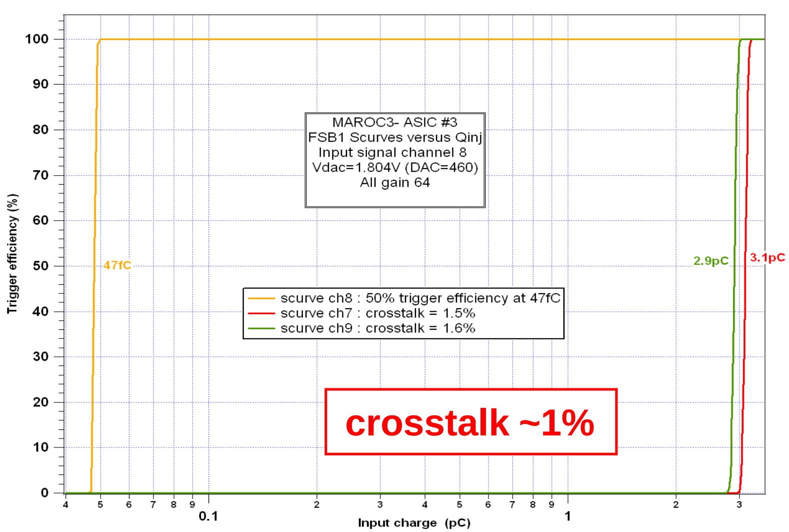
AMS SiGe 0.35µm
Package: CQFP240
Area: 16 mm2

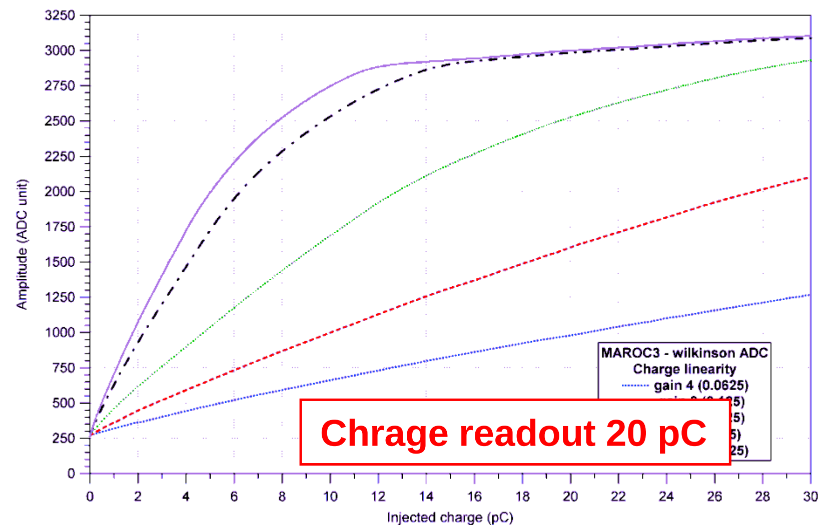


MAROC3 performance



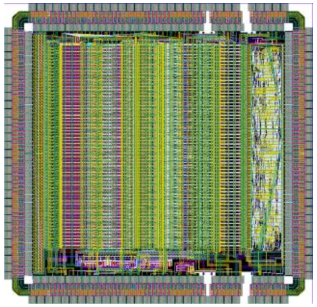


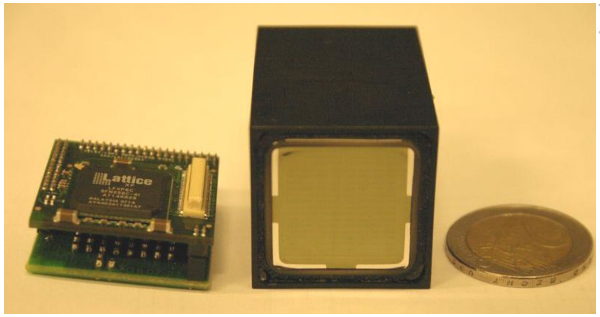


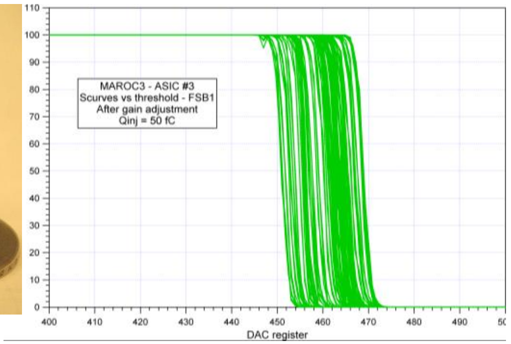


MAROC3 users

Omega







2012-2013	
Ralf ENGELS	Allemagne/Juelich
Vladimir SOLOVOV	Portugal/ Coimbra
Scott Lumsden	UK/Glasgow
JJ Velthuis	UK/Bristol
Piero Giorgio FALLICA/ ST micro	Italie/ Catania
Vincent TATISCHEFF	France/Orsay
Alexander Nadeev	Russie
Domenico Lo Pesti	Italy/Catania
E.L. Rizzini	Suisse/Genève
D. Lo Presti	Italie/ Catania
P. Rodrigues	Portugal/Lisboa
Stephen Wotton	Suisse/Genève
JJ Velthuis	UK/Bristol
Riccardo Faccini	Italie/Roma
Patrizia Rossi	Italie/Frascati
Sima Cristina	Roumanie/Magurele
Patrizia Rossi	Italie/Frascati
D.Cussans/P.Baesso	UK/Bristol
Paolo Baesso	UK/Bristol

Alain Blondel	Suisse/Genève
Pedro Rodriguez	Portugal / Lisboa
William Brooks	Chili / Valparaiso
Stephane Colonges	France / Paris
Evandro Lodi Rizzini	Suisse / Genève
Günter Kemmerling	Allemagne/Juelich
Thomas Schweizer	Allemagne/Munich
Jason Legere	USA / Durham
Evandro Lodi Rizzini	Suisse / Genève
Ronan Oger	France / Paris
Erik Vallazza	Suisse / Genève
Daniel Bertrand	Belgique / Bruxelles
Ronan Oger	France / Paris
Jason Legere	USA / Durham
Tanushyam Bhattcharjee	Kolkota/Inde
Vincent Tatischef	France / Orsay

Gabriela Llosa	Espagne / Valence
Pierre Salin	Sofia Antipolis/France
Prof. A.A.Petrukhin	Russie/Moscou
Erik Vallazza	Suisse / Genève
Riccardo Faccini	Roma/Italie
Pierre Salin	Sofia Antipolis/France
John Parsons	USA
Bernard Genolini	France / Orsay
Nicoleta Dinu	France / Orsay
JJ Jaeger	France / Paris
Vincent Tatischef	France / Orsay

ATLAS lumi : 500chips (LAL)
Double Chooz : 1000 (Nevis)

CLAS12 RICH (INFN)
LHCb RICH ? (CERN)
JUNO Veto ? (IPHC)

IFIN-HH

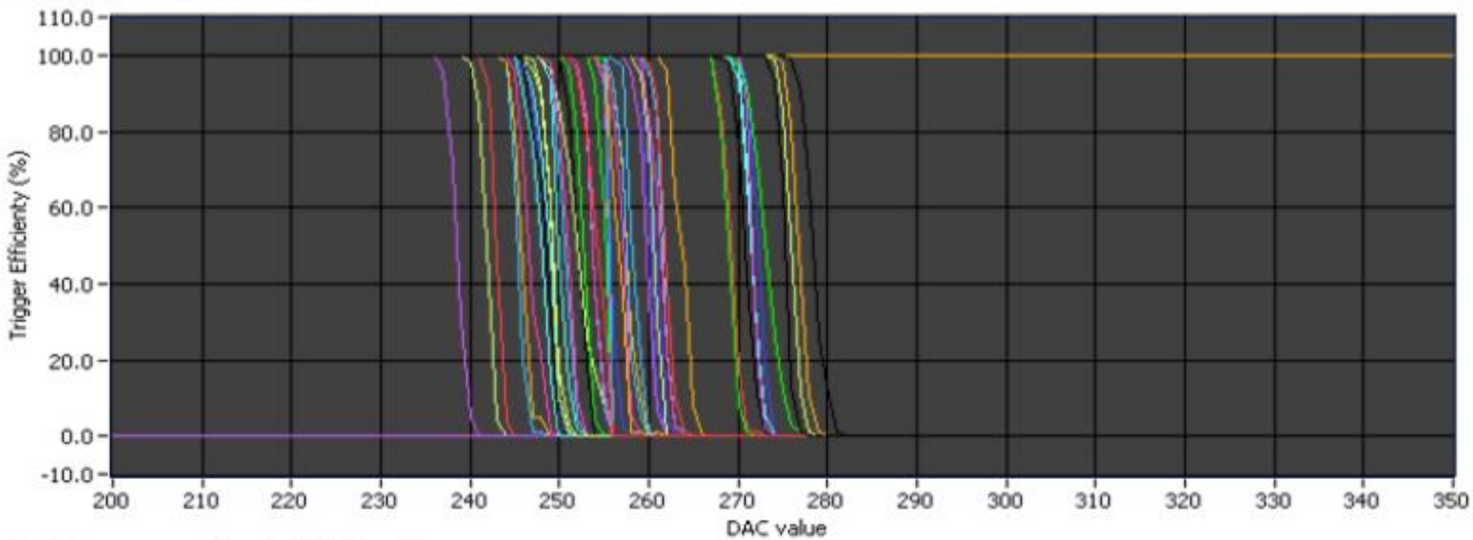
LHCb

Results

S curve

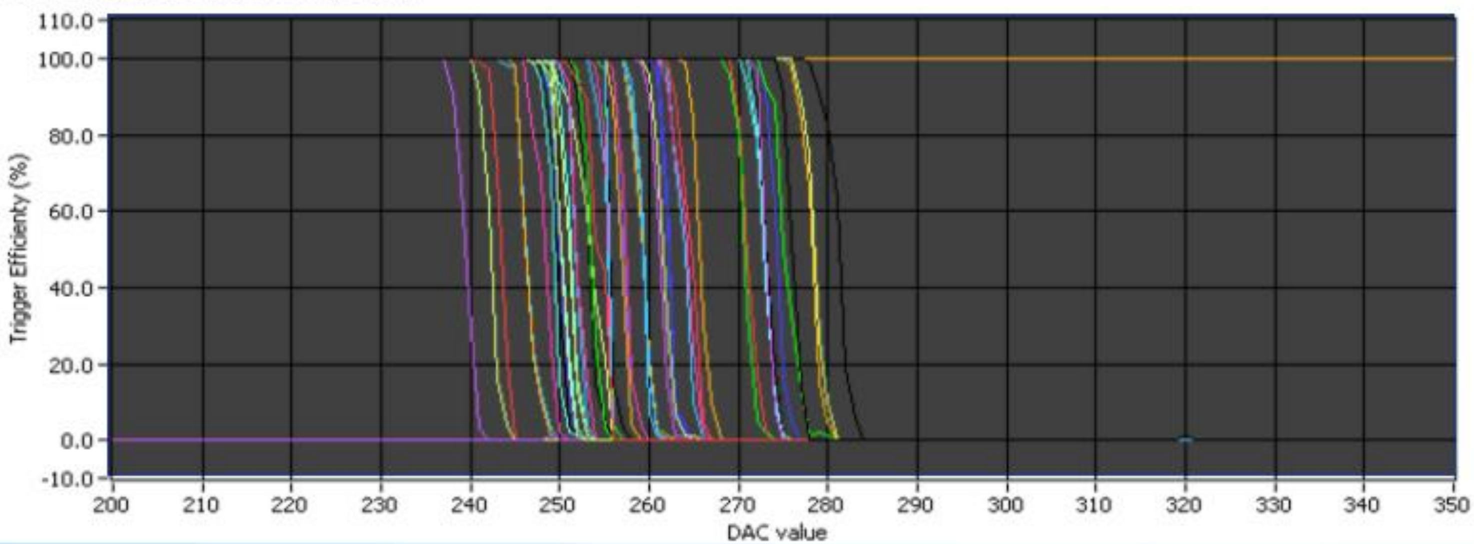
Charge: 150 fC
Before irradiation

Test S-curve vs Threshold (Ctest)



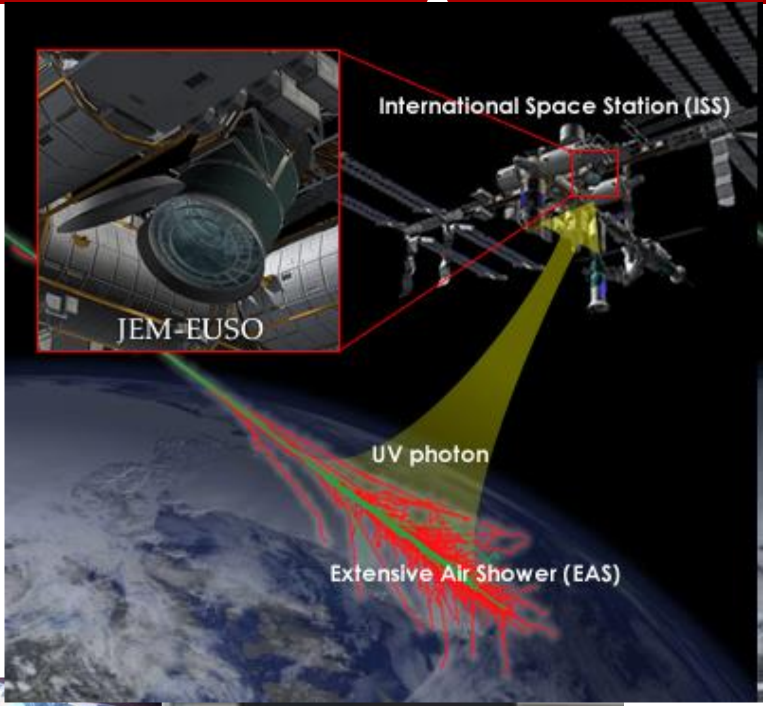
Charge: 150 fC
Dose_4: 24 Mrad

Test S-curve vs Threshold (Ctest)



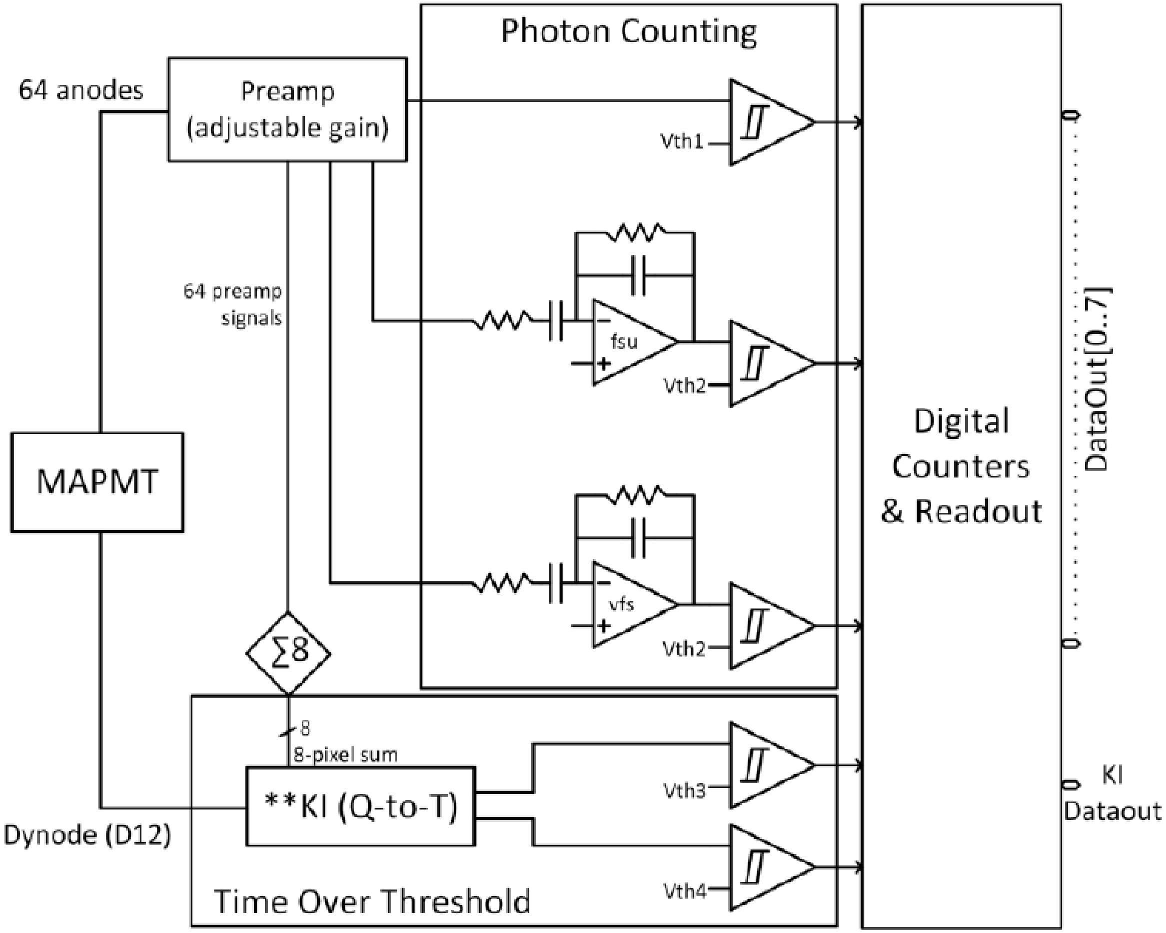
Variant : SPACIROC for JEM-EUSO

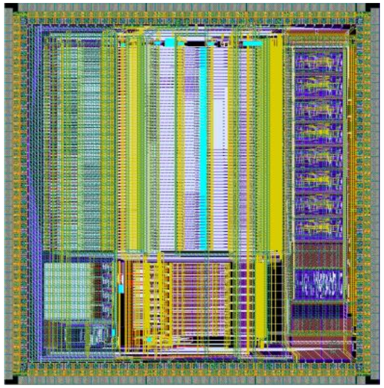
- JEM-EUSO (JAXA)
  - Cosmic ray imaging from ISS
- EUSO balloon (CNES)
  - Test flight 25/8/14
- TA experiment (UTAH)



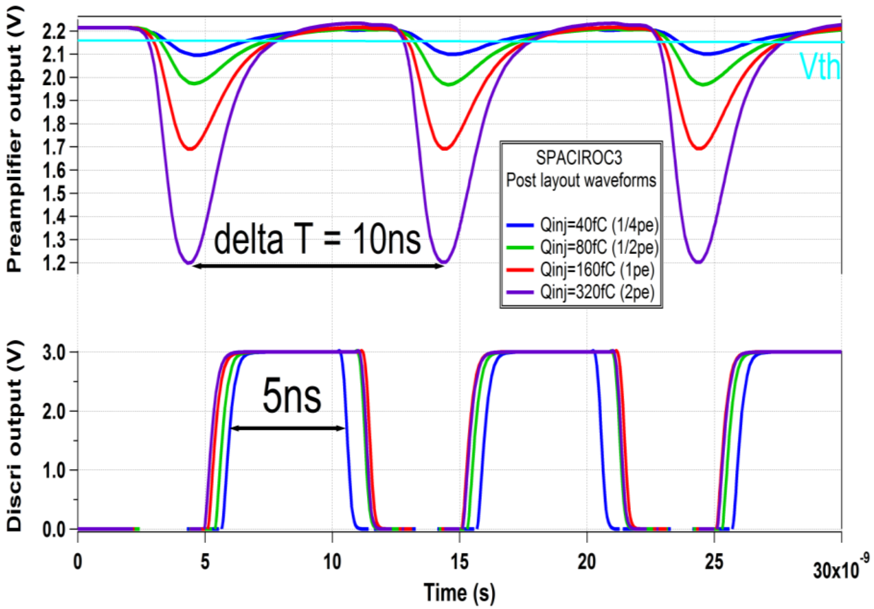
SPACIROC

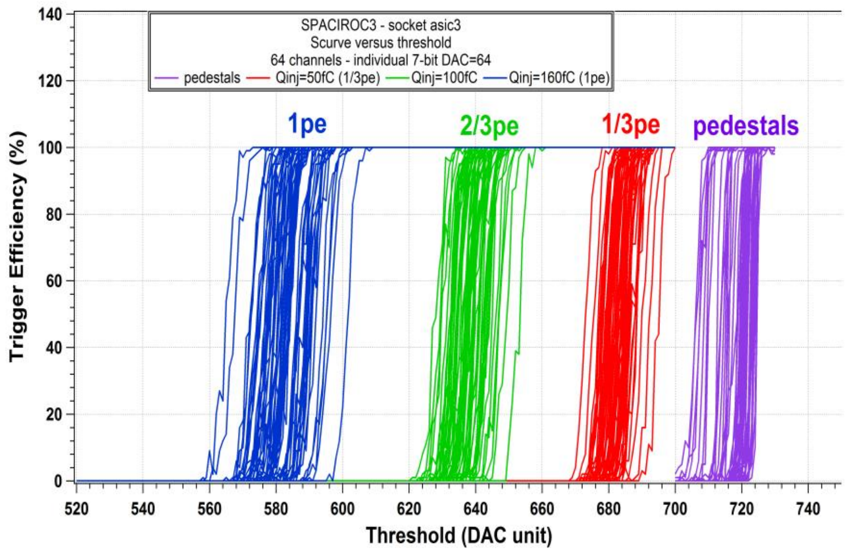
- 100 MHz Photon counting for JEM-EUSO
- 64 ch radtol MaPMT readout
- Pd < 1 mW/ch

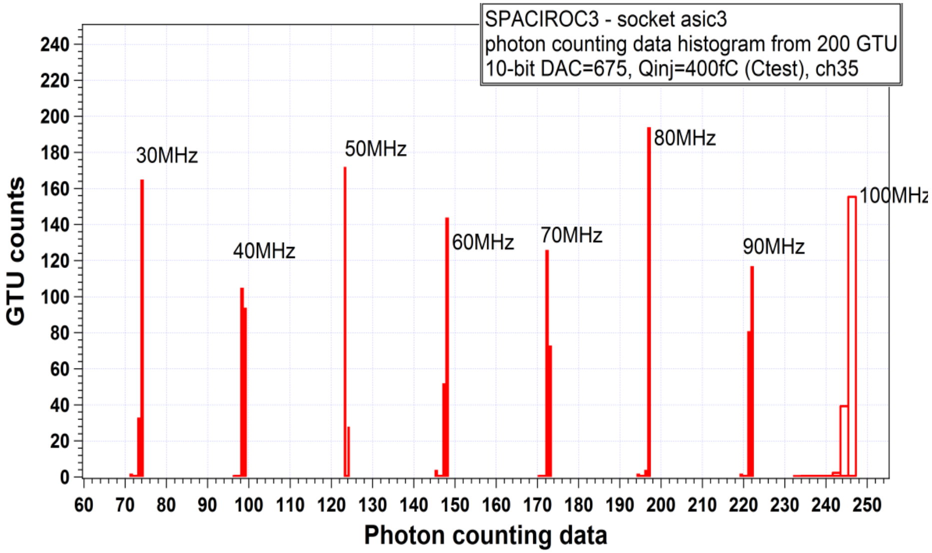


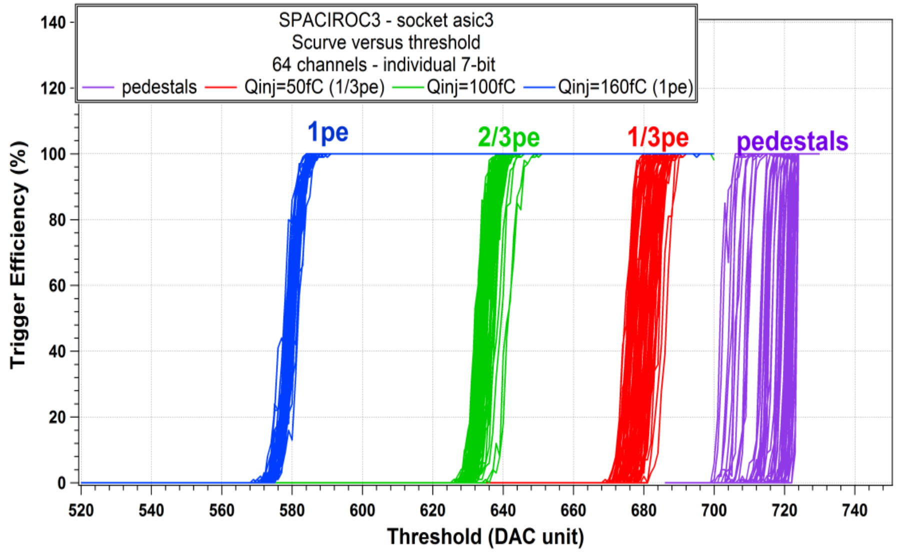


SPACIROC3 performance

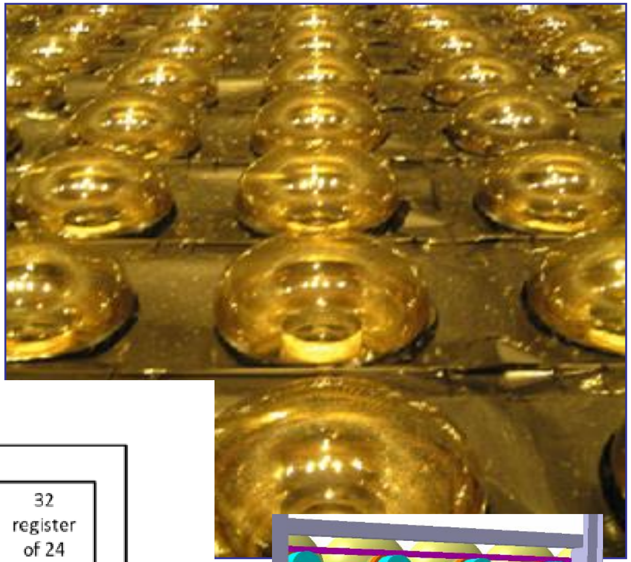


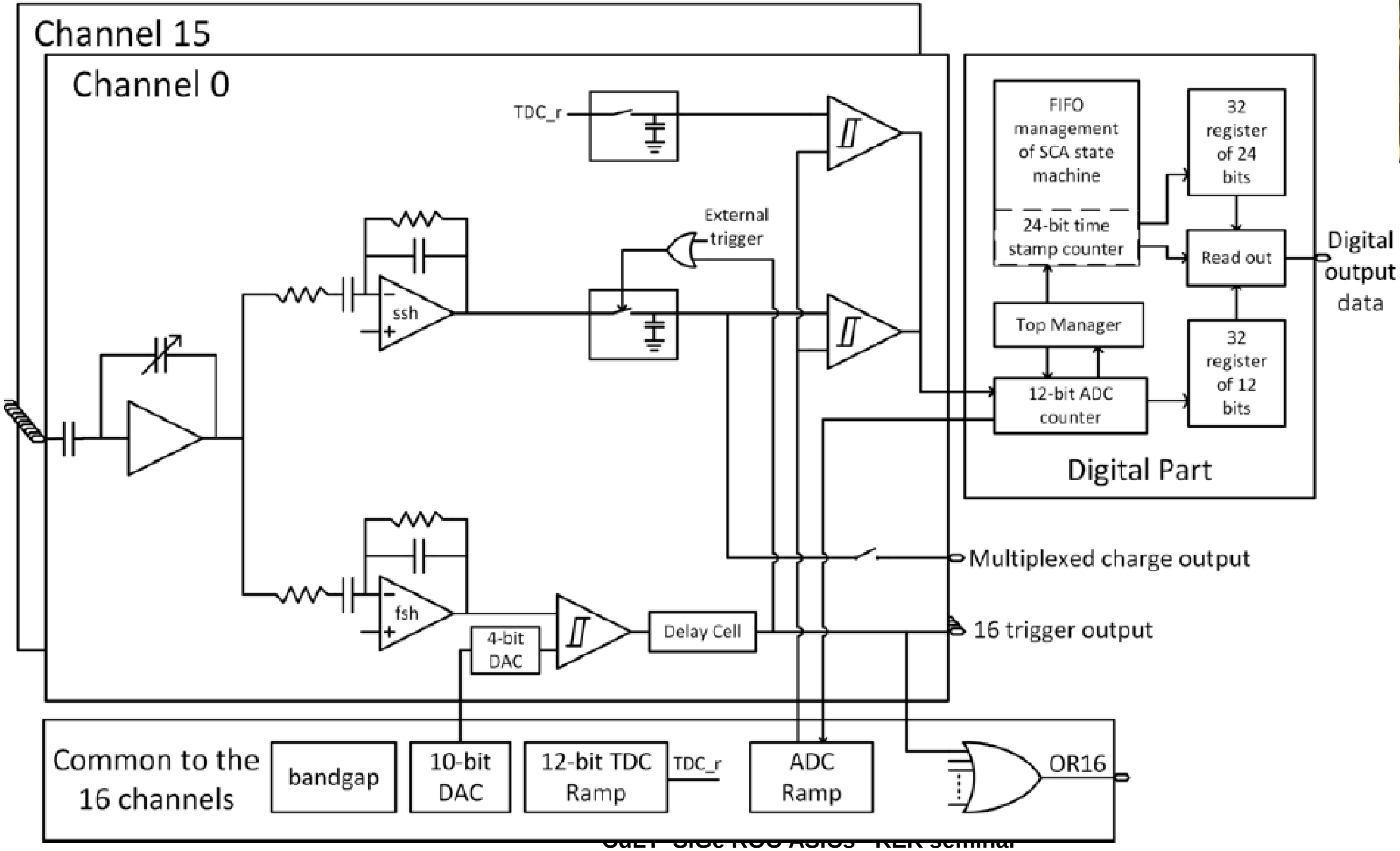


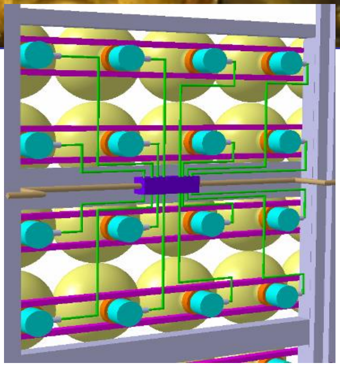


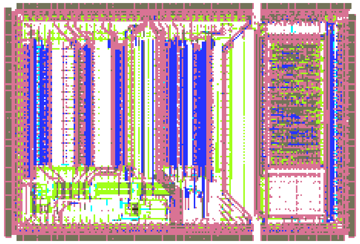


- Photomultiplier ARray Integrated SiGe ROC
  - « Large area PMT array » with centralized ASIC
  - Auto-trigger at 1/3 p.e.
  - Charge and time measurement (10-12 bits)
  - Data driven : « One cheap wire out »



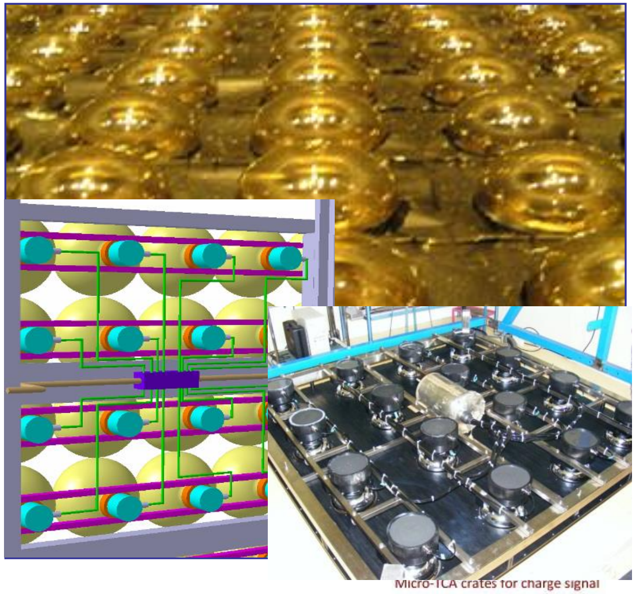


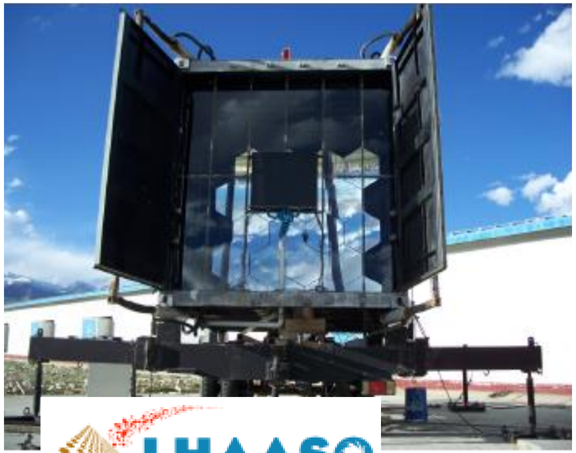


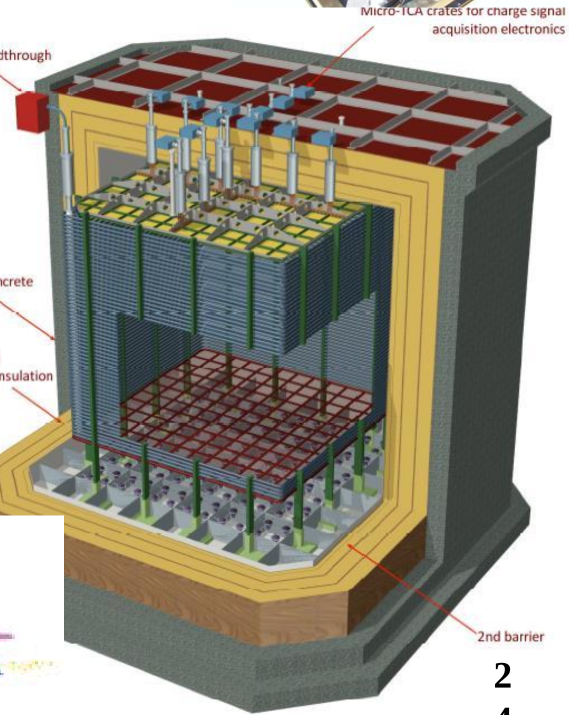


LAGUNA/LHAASO : PARiSROC (PMm²)

- Next generation large area photomultipliers
  - Replace large PMTs by arrays of smaller ones (PMm² project)
  - Centralized ASIC 16 independent channels
  - Data driven : zero suppressed digital output
  - Single photoelectron sensitive, 100 ps timing





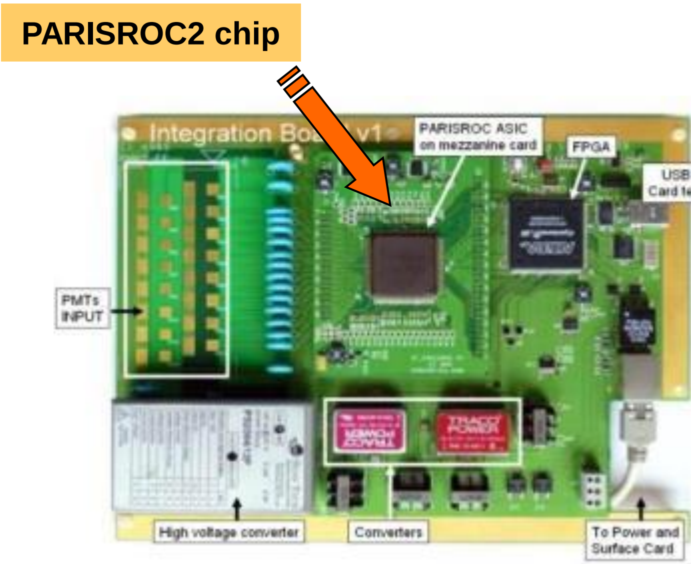


Large scale demonstrator with 7680 electronic channels in liquid Argon

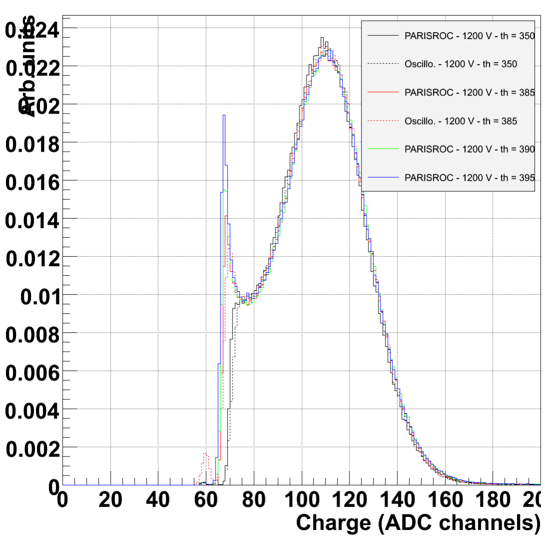
© Tomas Patzak, Margherita Buizza APC, Paris, France

© Tiina Suomijarvi, Yingtao Chen IPN, Orsay

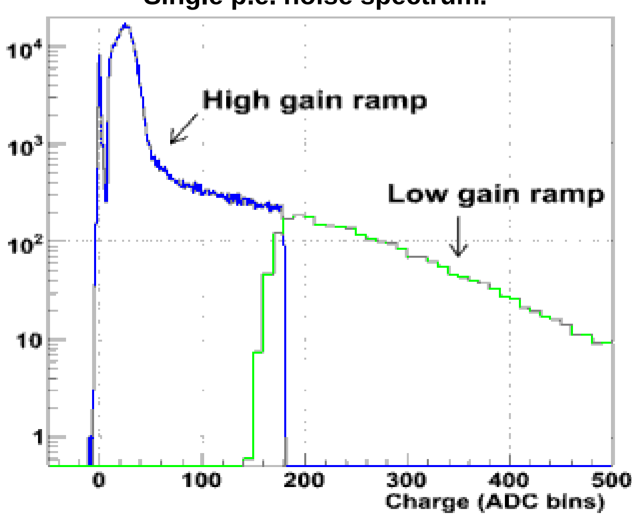
PMm² demonstrator

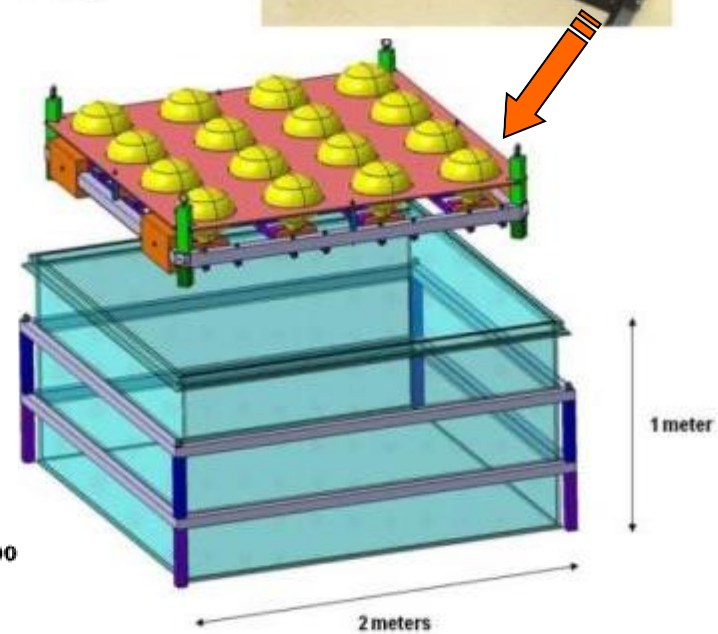


1-in (XP3102) single p.e. noise spectrum.



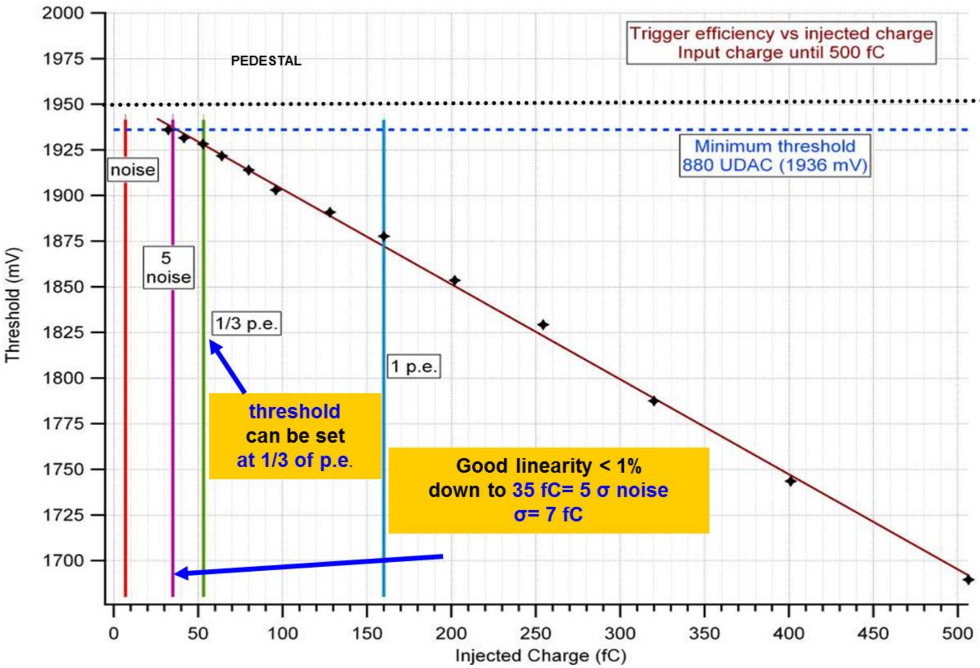
8-in (Hamamatsu R5912)
Single p.e. noise spectrum.

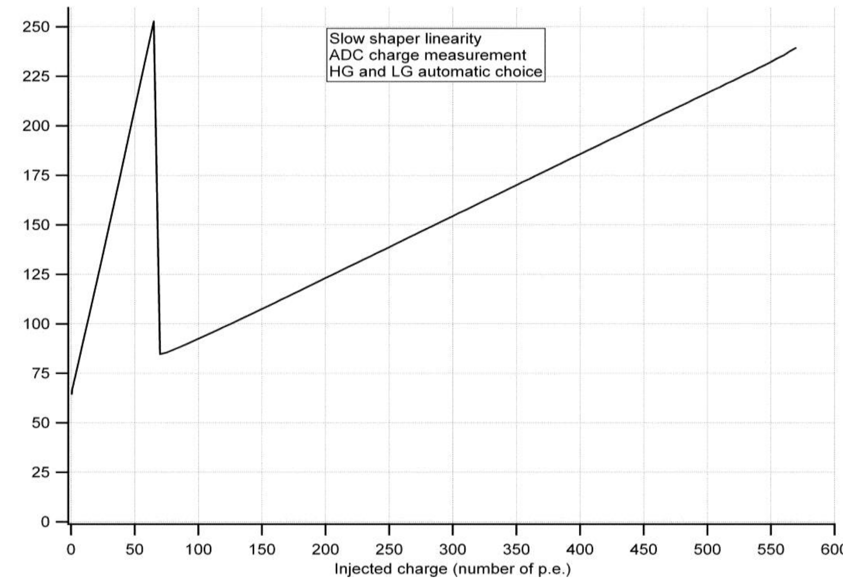


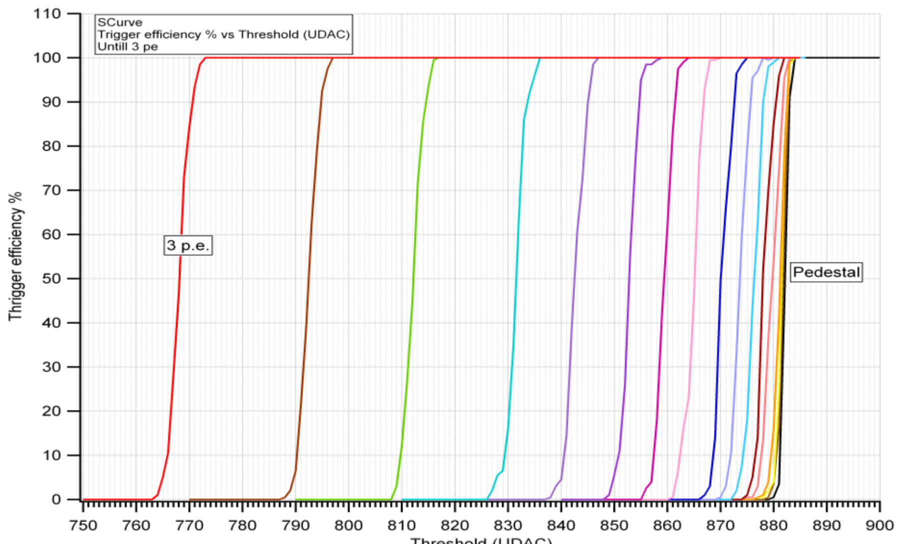


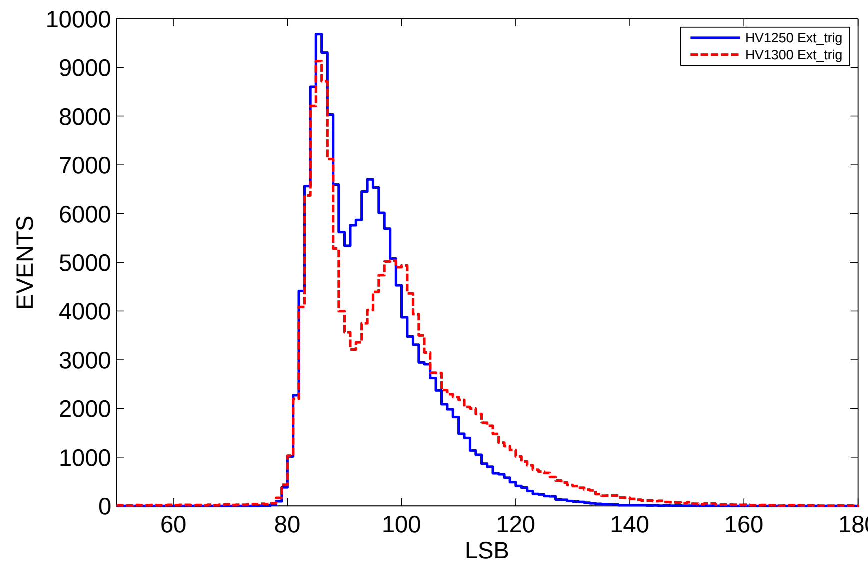
Performance

Ωmega

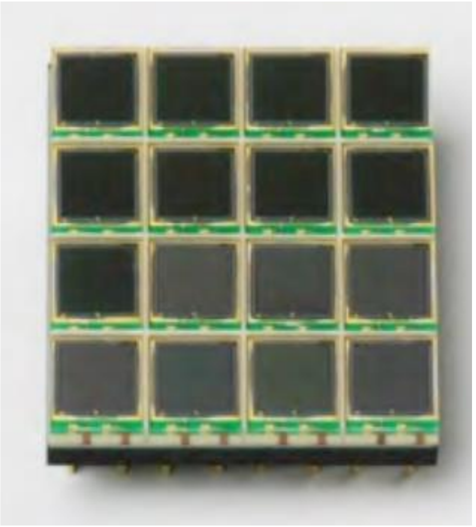








- SPIROC
- EASIROC/CITIROC
- PETIROC
- TRIROC



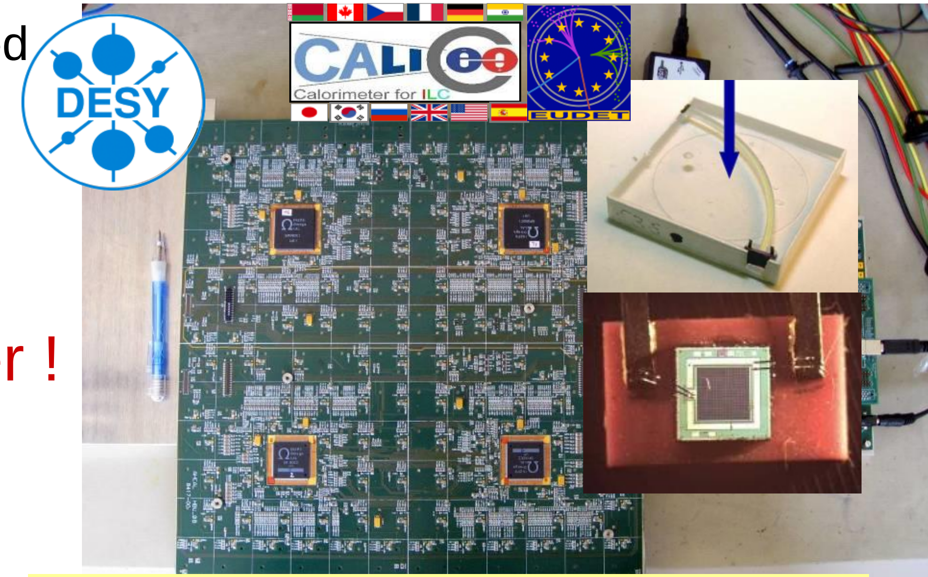
SiPM from SPIROC to TRIROC

- FLC_SiPM designed and produced to equip the Analog H-Cal physics prototype for the ILC in 2005 (1 cubic meter, 38 layers, 2cm steel plates, 8000 tiles with SiPM)
  - 1st ASIC to readout SiPM
- SPIROC developed in November 2007 to equip the CALICE AHCAL and ECAL EUDET technological prototypes
- Variants of SPIROC: EASIROC designed in September 2009, CITIROC in 2013
  - EASIROC/CITIROC : "light" analog version of SPIROC for SiPM users who don't need the ILC specific digital core
- Others applications using SPIROC/EASIROC/CITIROC chips for SiPM readout
  - Astrophysics: PEBS experiment (Aachen University), CTA
  - Medical imaging (Roma, Pisa, INMC Orsay, Valencia, etc.)
  - Nuclear physics: E40 experiment (KEK)
  - Volcanology: MuRay muon radiography of geological structures (INFN Napoli)
- Dedicated chip for fast timing and high timing resolution applications
  - PETIROC (November 2013)
  - TRIROC (March 2014) "FP7" project

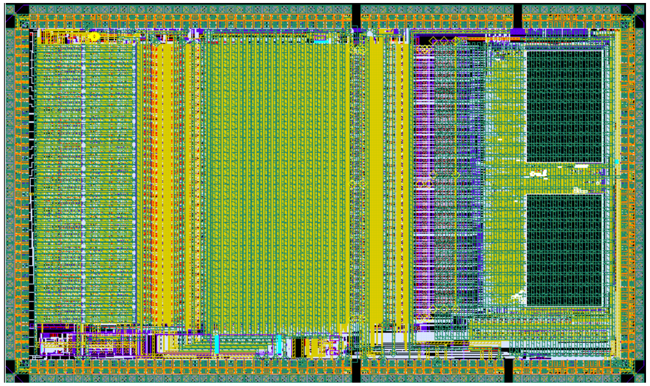
SPIROC for SiPM readout

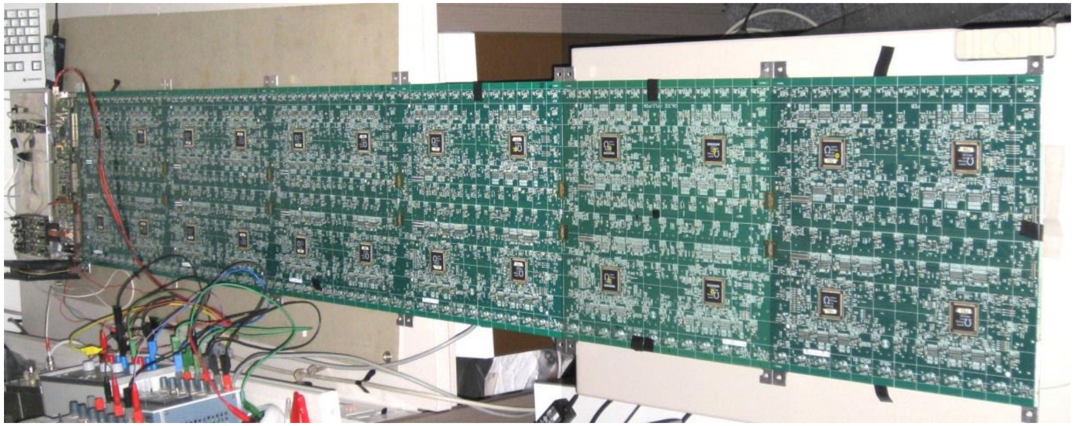
- SPIROC : Silicon Photomultiplier Integrated Readout Chip
  - Developed to read out the analog hadronic calorimeter for CALICE (ILC)
  - DESY collaboration (EUDET project)
  - Chip embedded in detector : **low power !**

- 36 channels autotrigger 15bit readout
  - Energy measurement : 15 bits in 2 gains
  - Autotrigger down to ½ p.e.
  - Time measurement to ~1ns
  - Power dissipation : 25µW/ch (power pulsed)

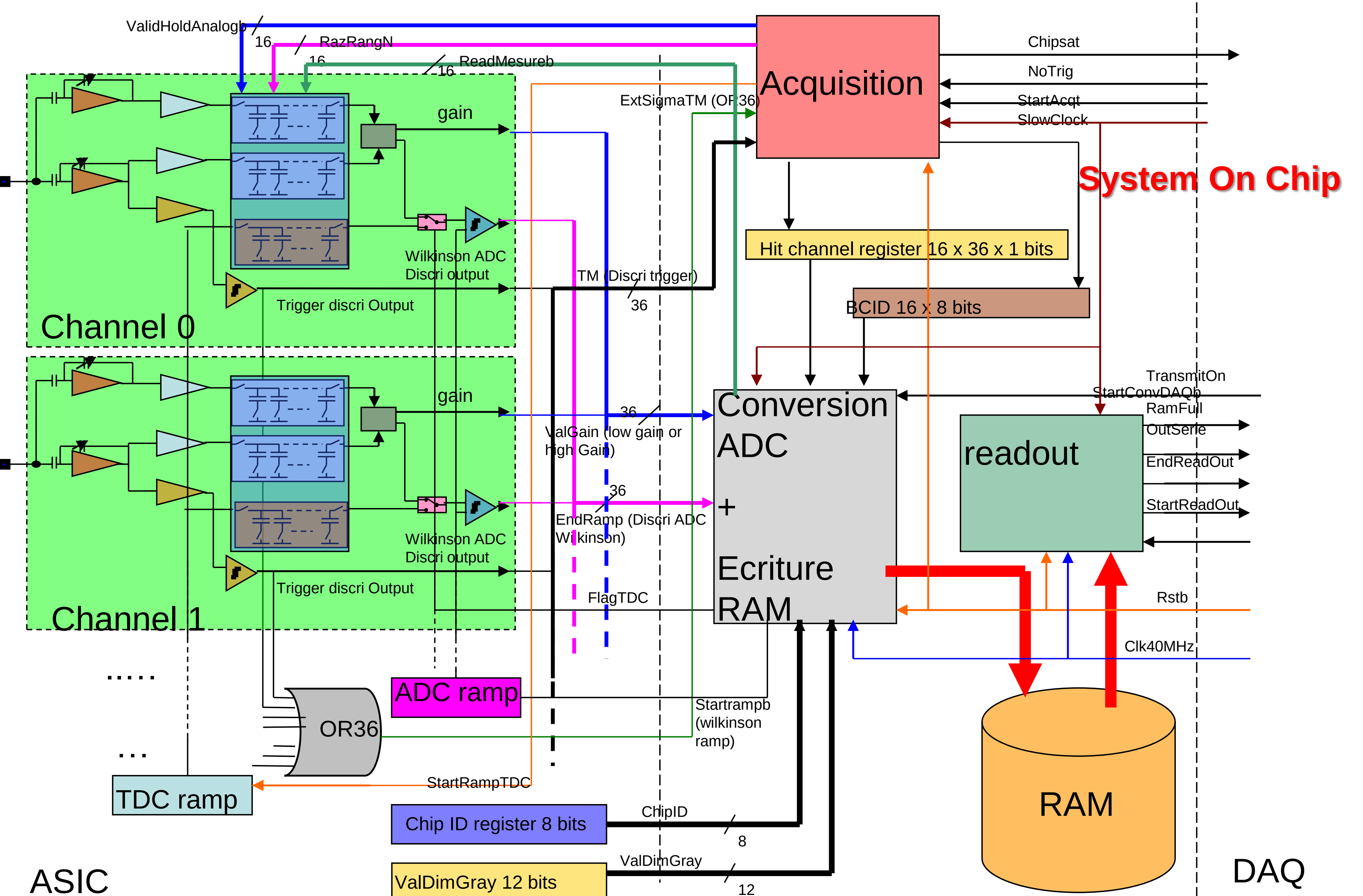


$(0.36m)^2$ Tiles + SiPM + SPIROC (144ch)



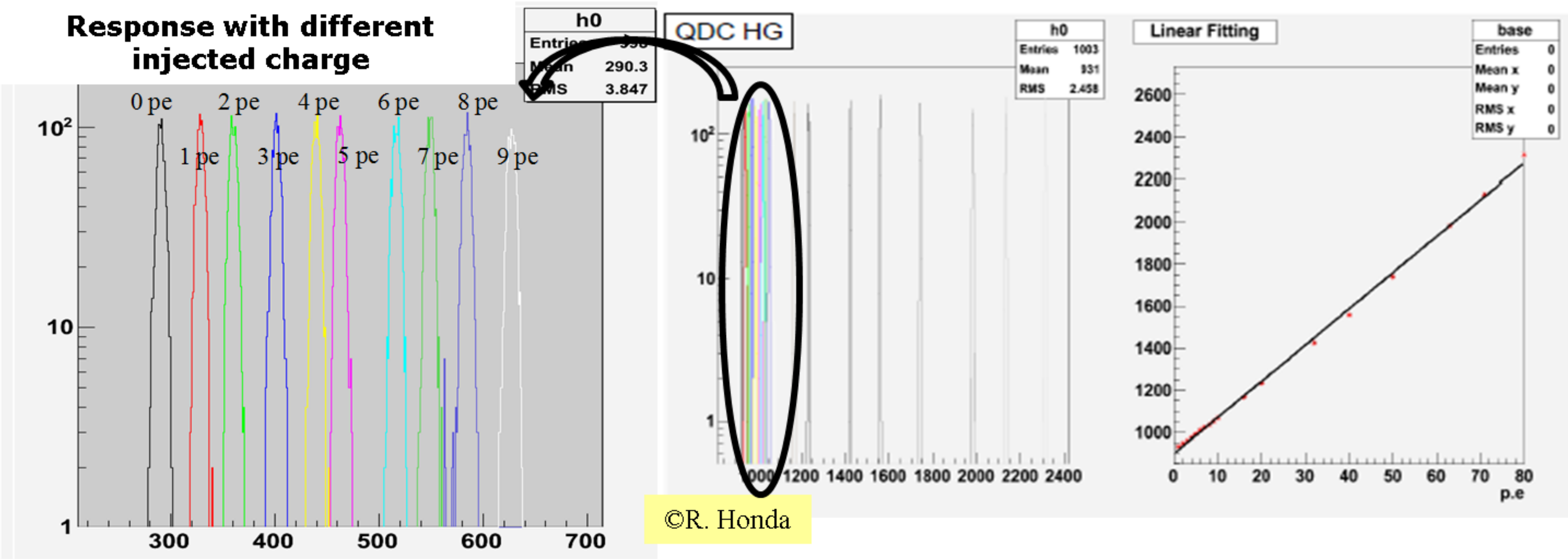


SPIROC : System On Chip

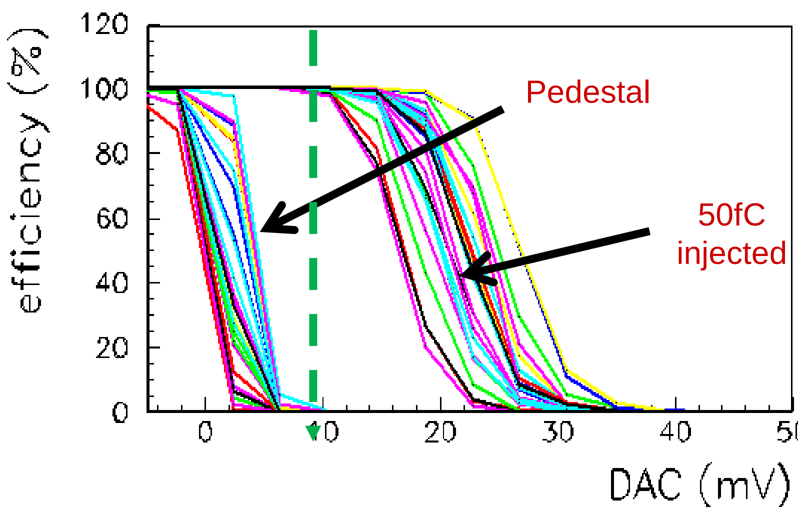


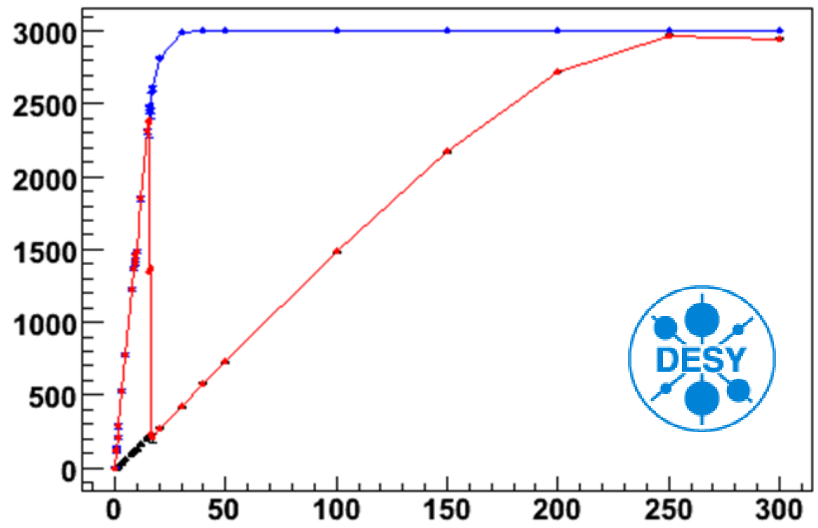
SPIROC performance

Response with different injected charge



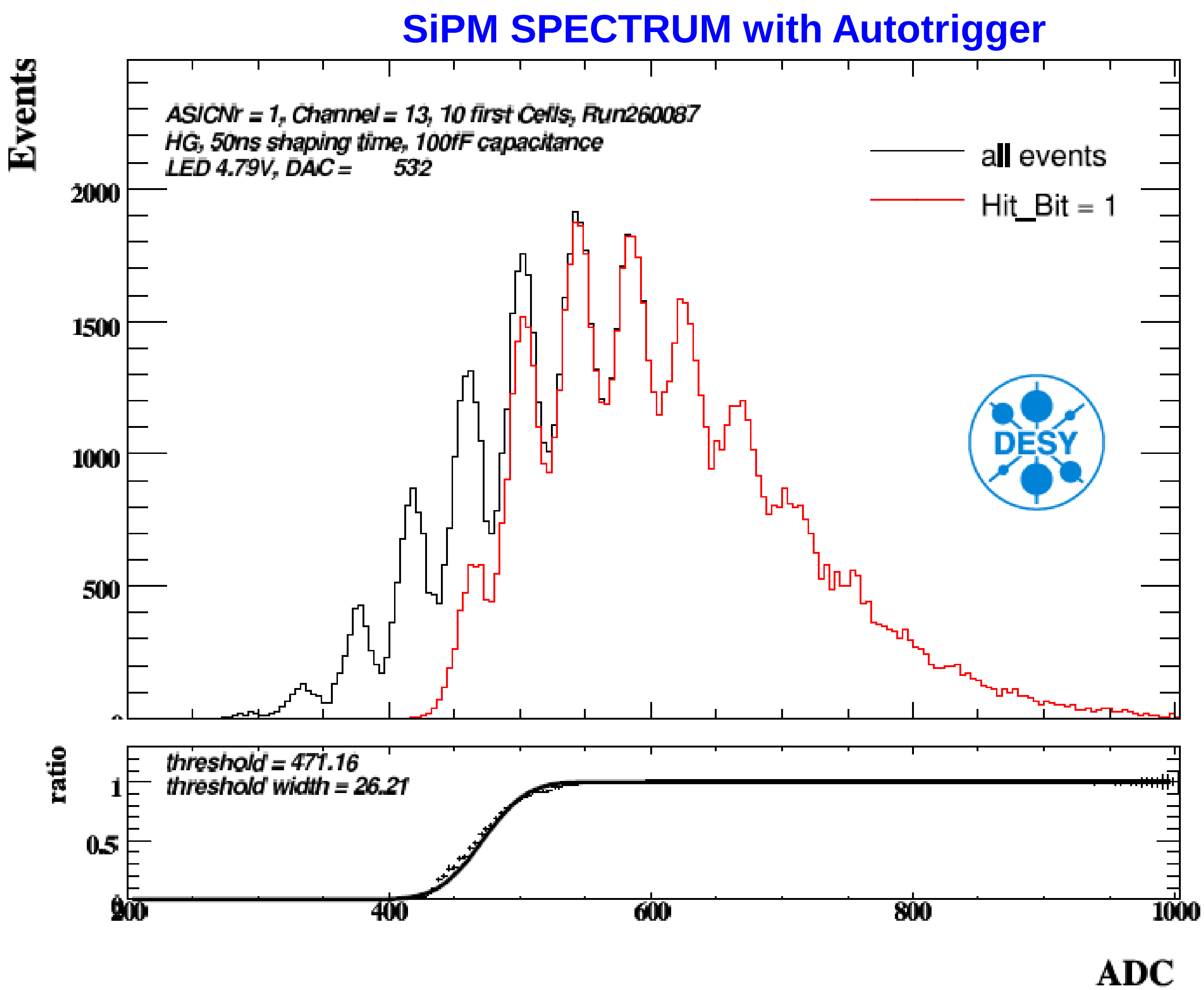
36-channel S-curves: trigger efficiency versus threshold (1 LSB = 2 mV)



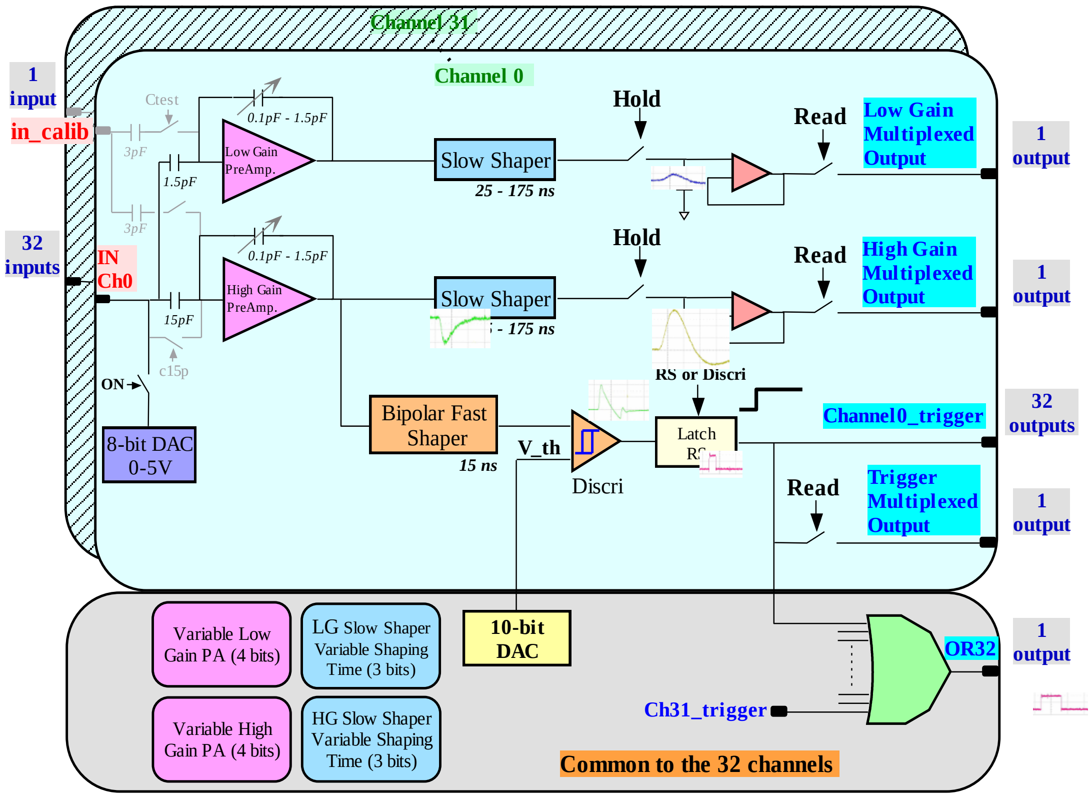


SPIROC2 performance

Ωmega

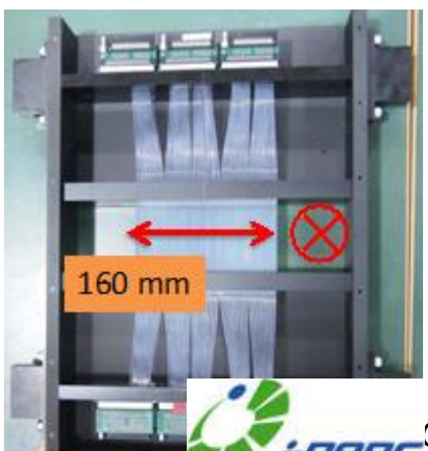


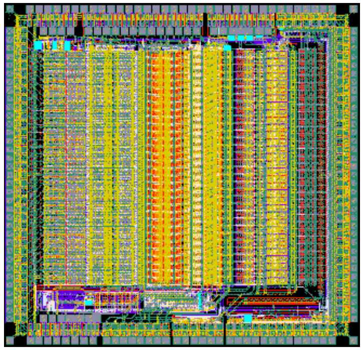
Variant : EASIROC/CITIROC



- 32-channel front-end readout (analogue part of SPIROC)
  - 2 multiplexed analog outputs (high gain, low gain) [tri state outputs]
- Trigger output
  - 32 Trigger outputs
  - OR32 output
  - Trigger multiplexed output (latch included) [Tri state output]
- Low power : 4.84 mW/channel, 155 mW/chip

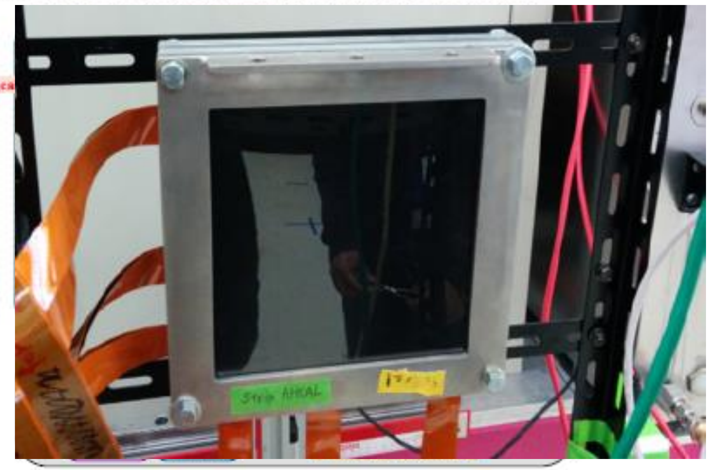
SipMed, IMNC, LAL, OMEGA

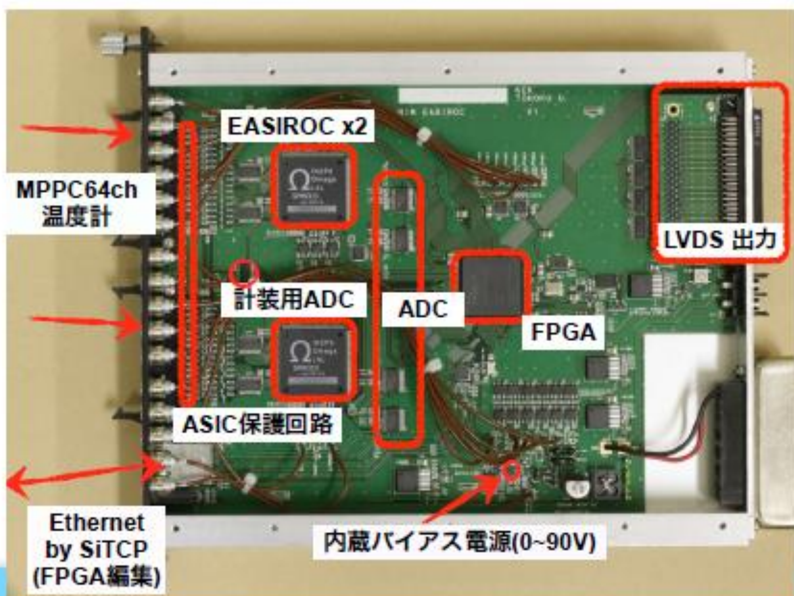


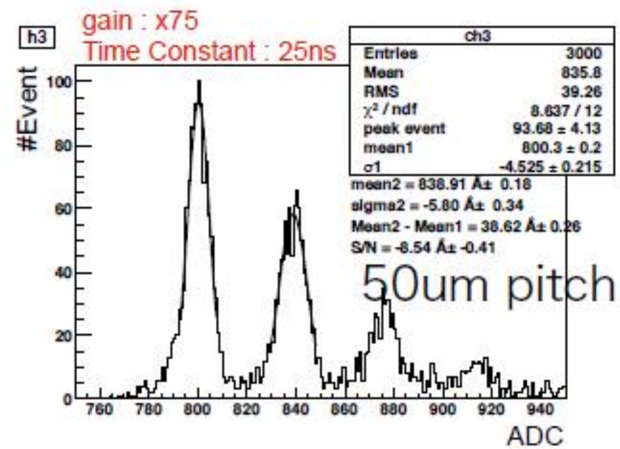


Easiroc module

- two EASIROC's + on board ADC
- 32x2 channel
- Vb = V0~-4.5V 8bit
- TCP/IP connection







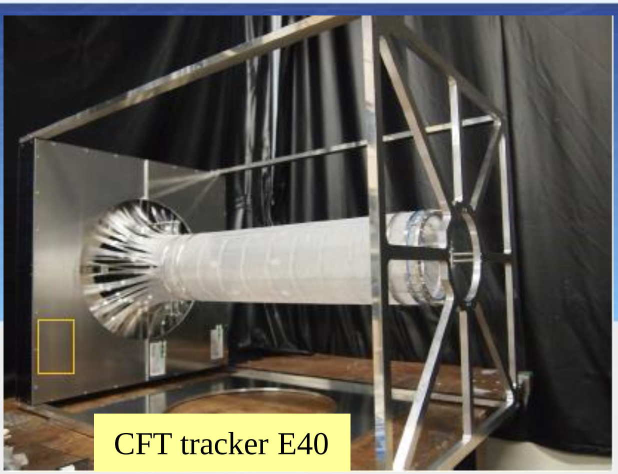
LED

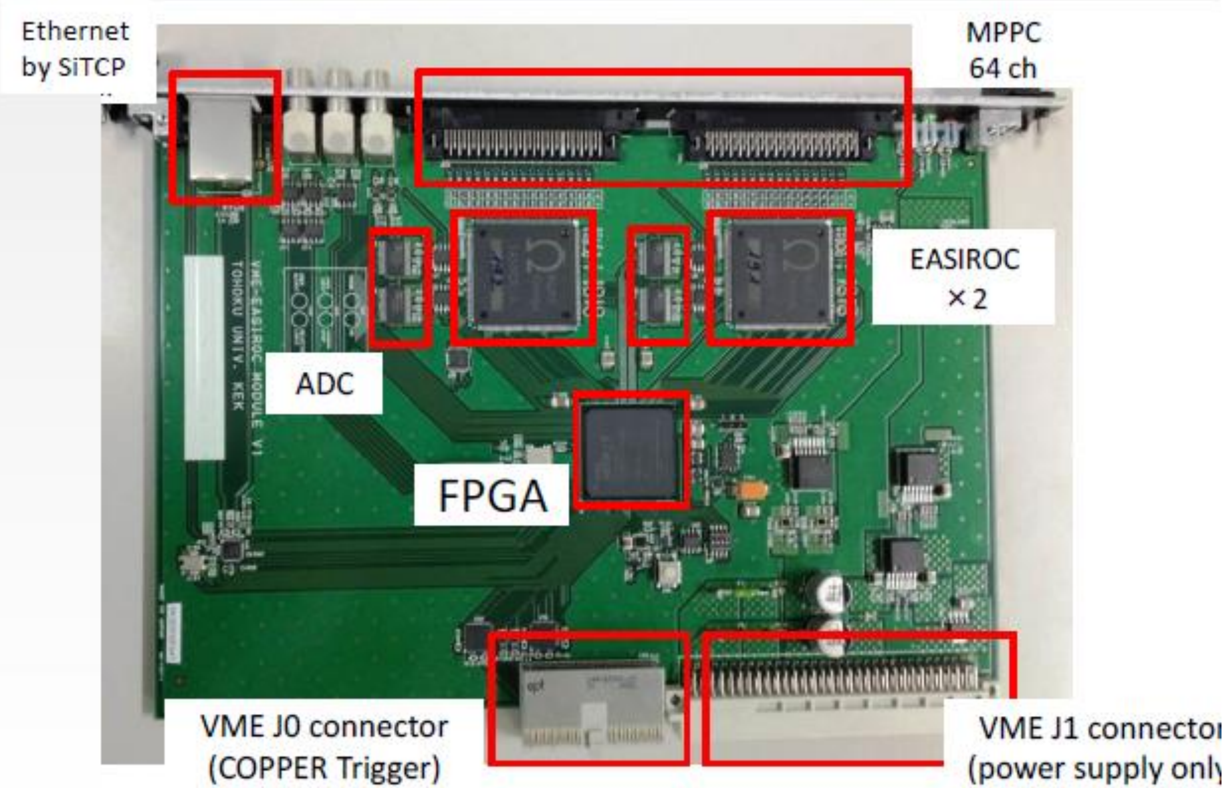
Ishijima

VME-EASIROC board Specification (ADC, TDC)

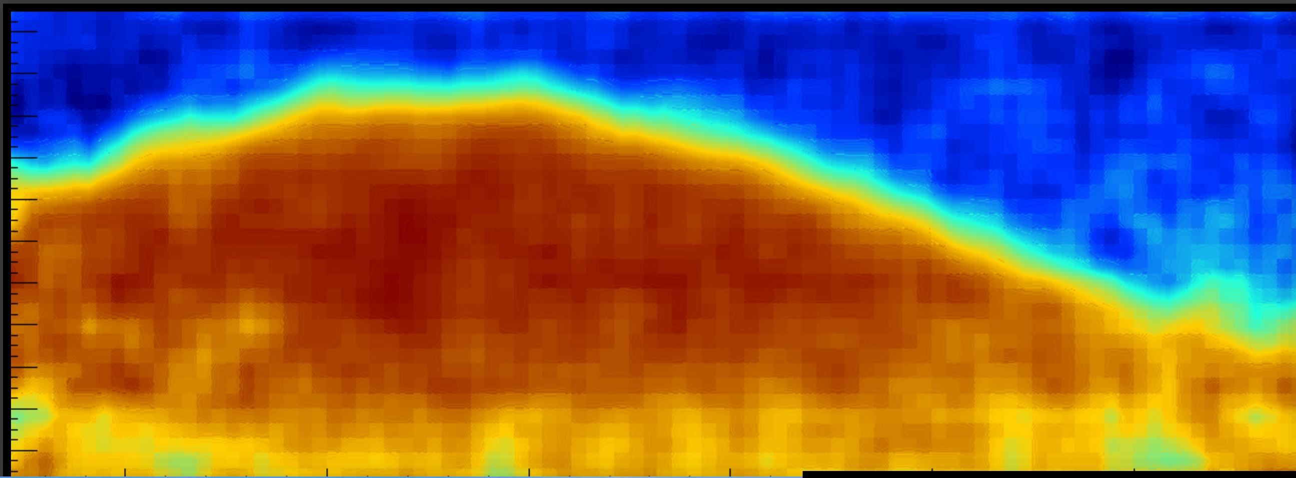
- VME 6U
- MPPC 64 ch (EASIROC x 2)
- FPGA Artix-7
- ADC
  - Dead time 12 µs
  - w/ Pedestal suppression
  - Fact clear
- MHTDC
  - LSB 1ns
  - hit depth / ch 16
  - Dead time : depend on hit number
    - < 12 µs
  - Fast clear
  - Time window 0~4 µs

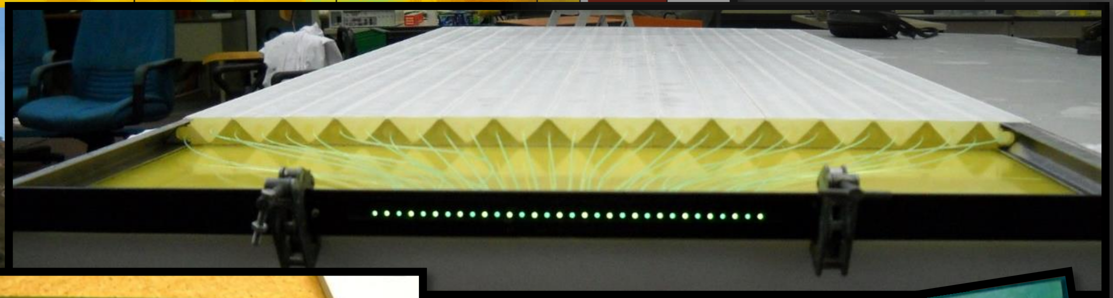
© T. Shiozaki, R. Honda, K. Miwa
S. Akawa (Tohoku, Univ)
T. Uchida, K. Ucheno (KEK E-sys)

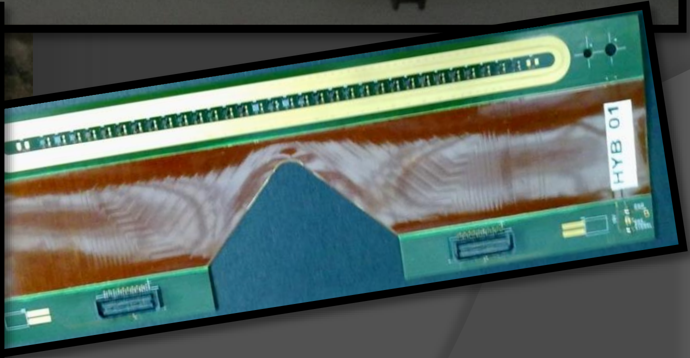




The "Shadow" of the Vesuvius



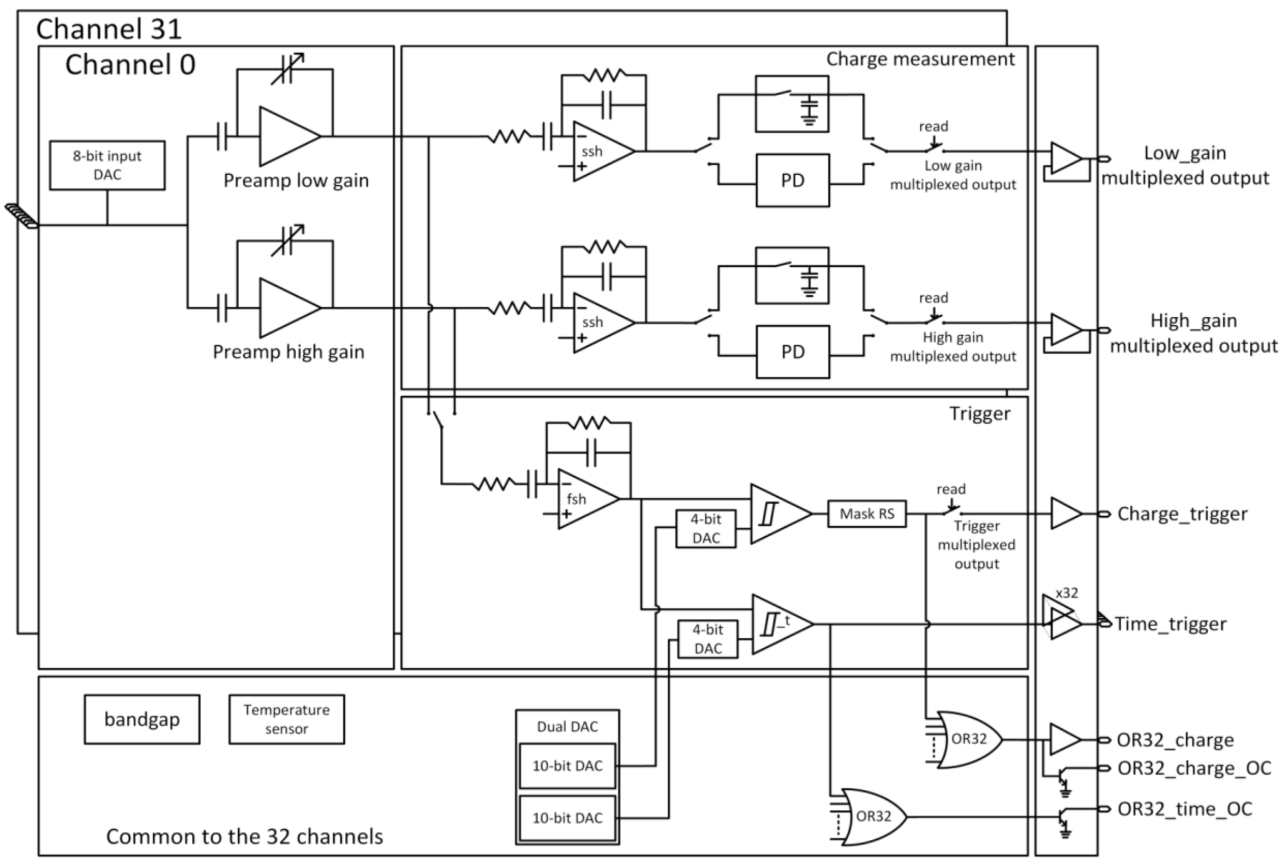


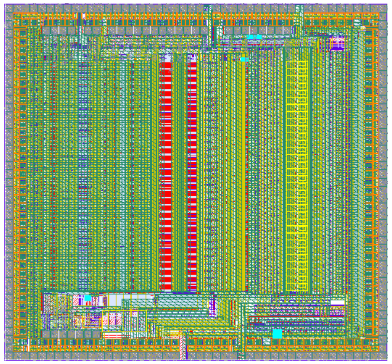


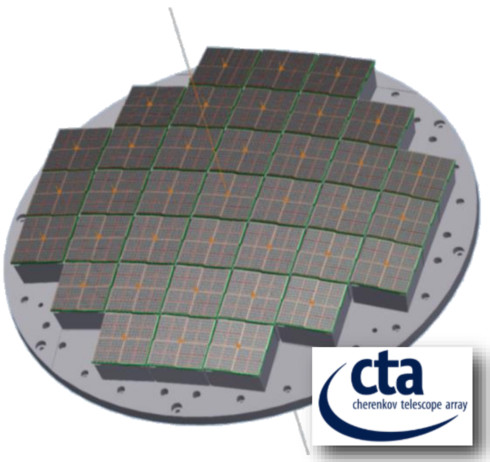
Omega

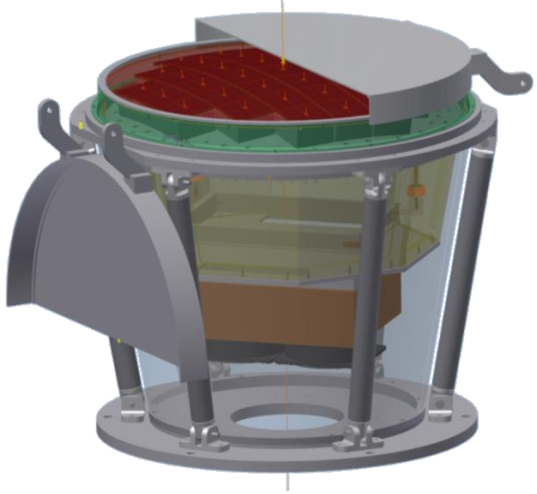
- Evolution of EASIROC 32 ch SiPM readout
  - 32 channels, positive input, 5V input DAC HV adjustment
  - 32 trigger outputs & High Gain / Low gain multiplexed charge output
  - Peak detector and two trigger level (timing & energy)
  - Gain adjustment per channel (6 bits)

weeroc



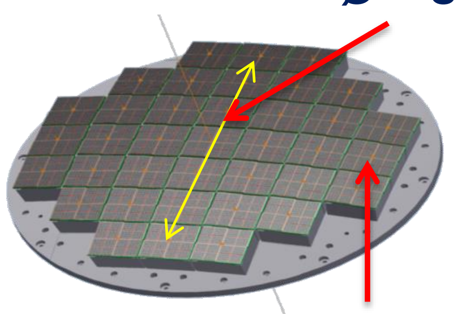






FOV = 9.6°

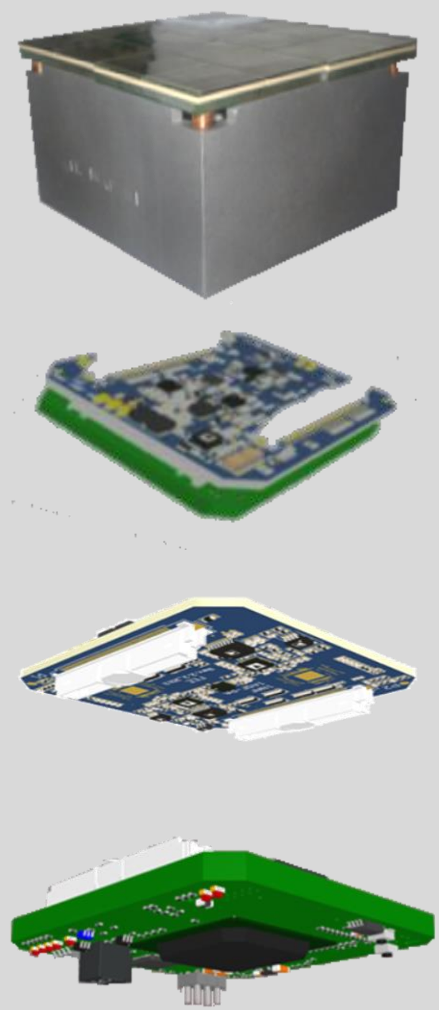
Ø = 350mm

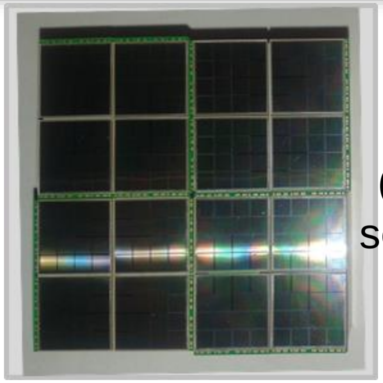


Photon Detection Module (PDM)

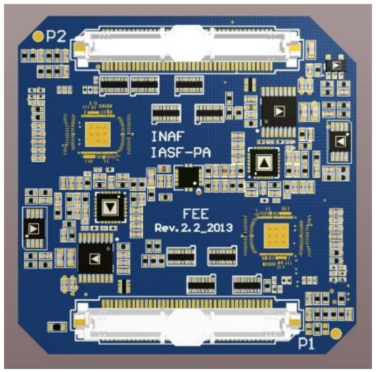
Pixel = 0.17° → 6.2 x 6.2 mm

ASSEMBLING

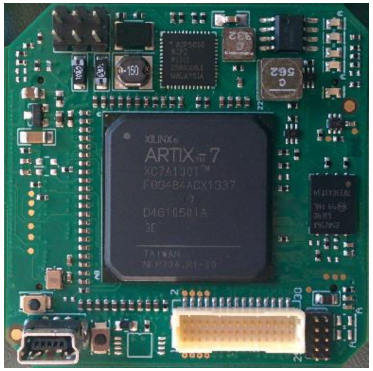




SiPM board
(9 +1 temperatur
sensors embedde

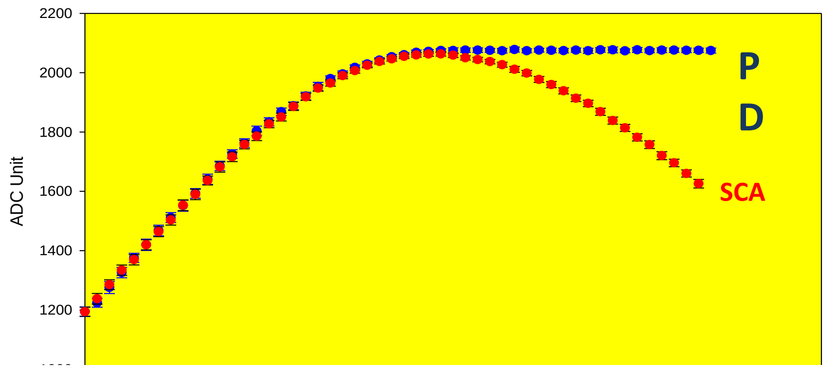


Front-End board
(2 CITIROC
ASIC)



PDM FPGA Board
(XILINX ARTIX 7)

CITIROC: Peak detector



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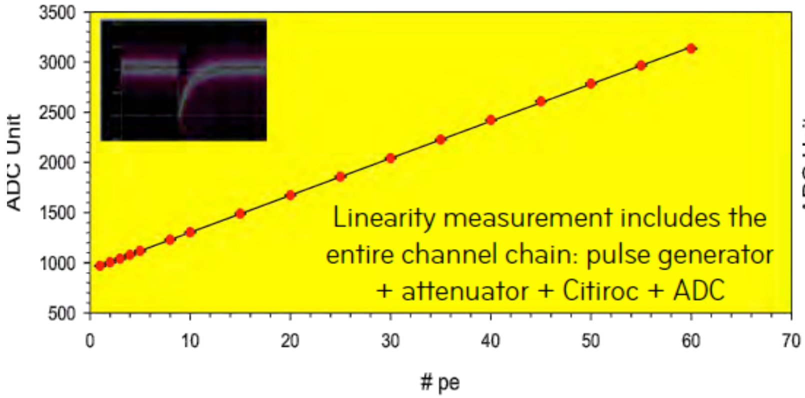
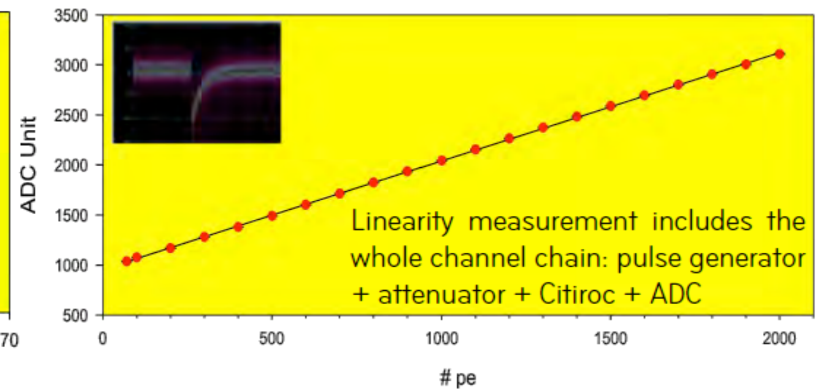
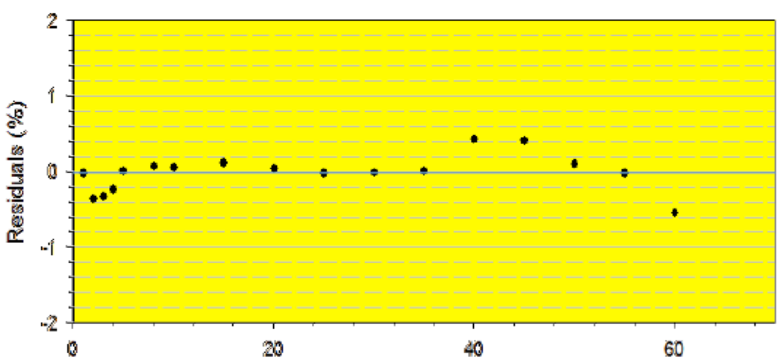
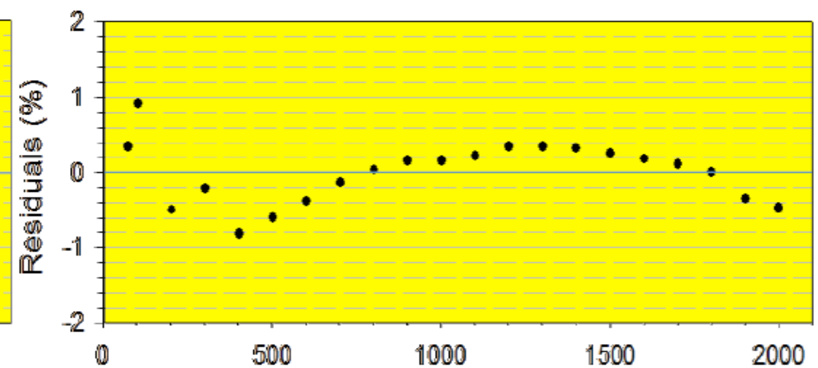
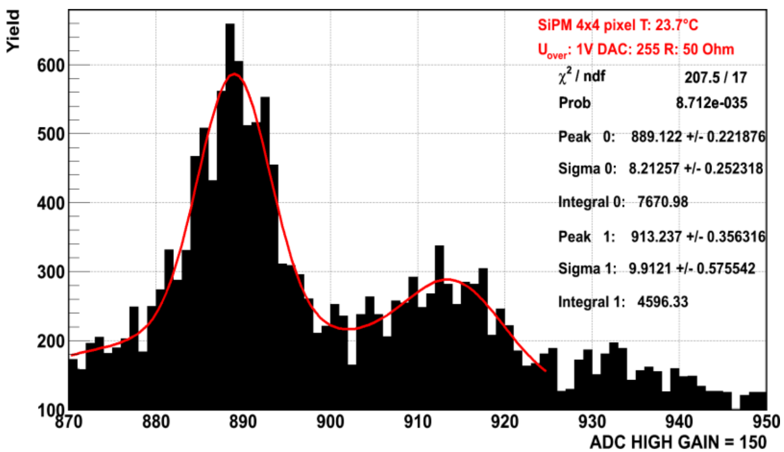


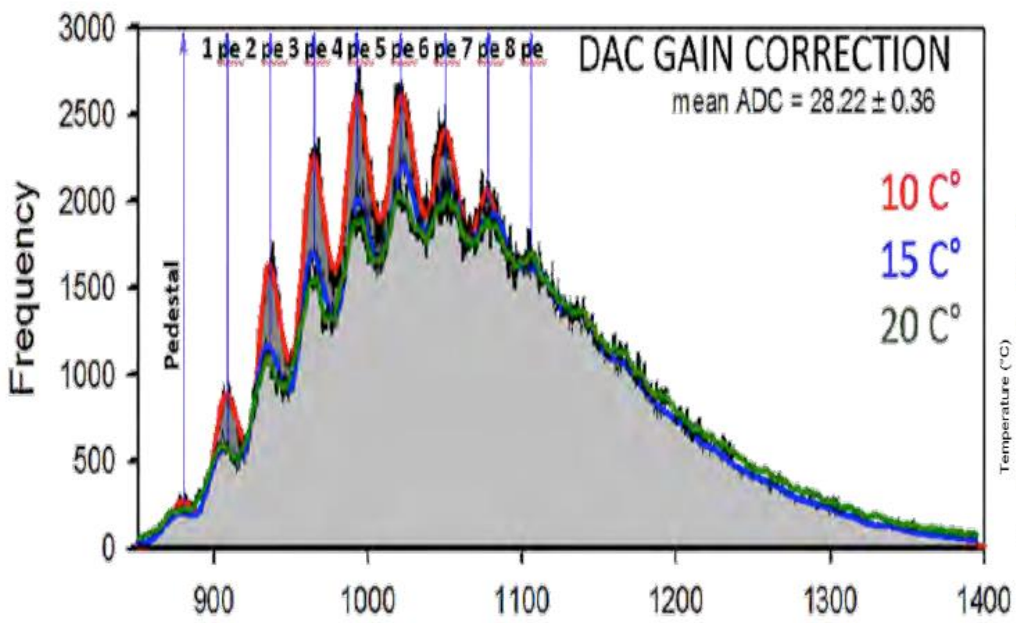


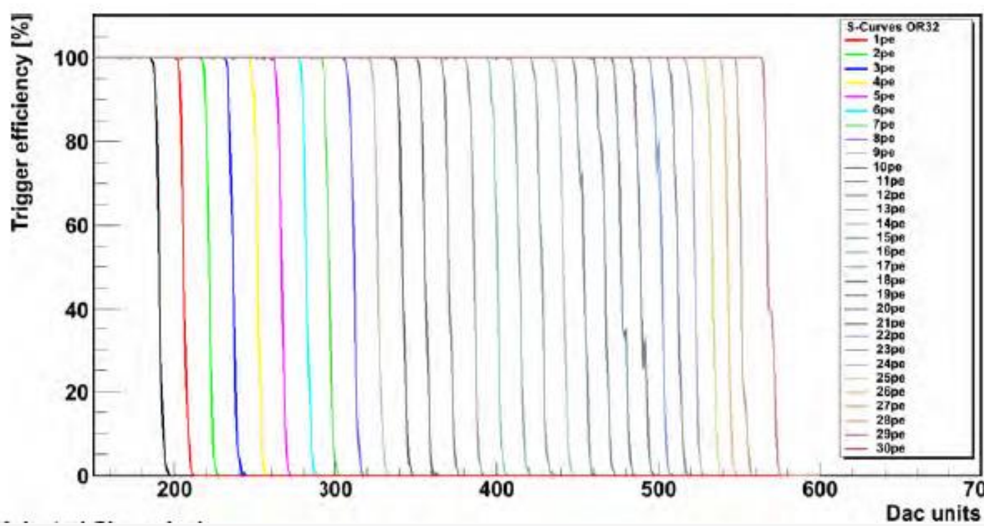




Gain premplifier =4*25fF ≈ 150 nom.
Shaping Time = 50ns
Steps of 1,2,3,4,5,6,7,8,9,10 pe







SiPM 4 pixel High Gain =150
Shaping Time = 50ns
delay time = 38 x 2.5 ns
Temp = 23.7 °C U_{over} = 1V
Resistance = 50 Ohm
Threshold = 922 DAC ~50% of 1 plateau

SiGe GHz Front End

Omega

- R&D of 10GHz GBWP preamps for applications where fast timing or high timing resolution is needed (Time Of Flight PET MRI, preclinical, particle physics…)
- 3 architectures in 0.35µm SiGe technology integrated and tested

1 pe-=160fC

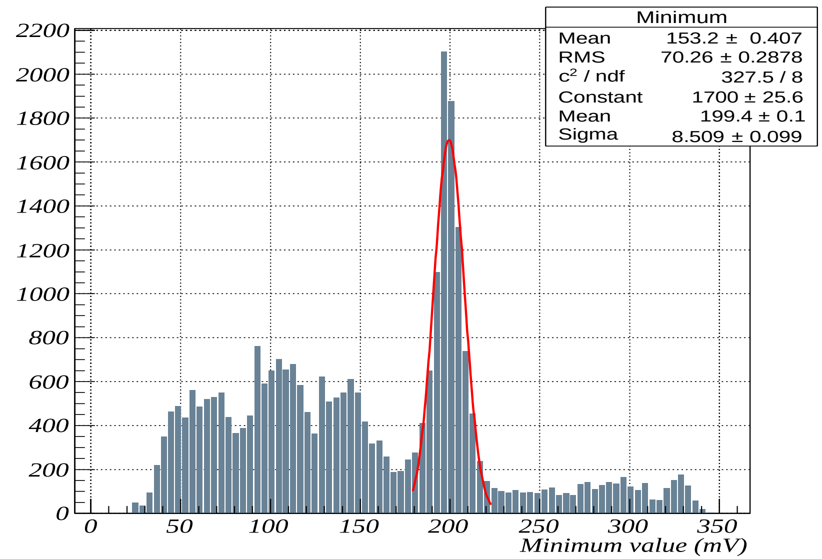
Testboard #3	RF (Common Emitter)	Common Base	Super Common Base
With 100pf/50 Ohm injector (SiPM emulation)		Vb_cb : 400 #DAC	Vb_scb : 1023 #DAC
Noise floor (pedestal)	185-187 #DAC / 1.196V	216-224 #DAC / 1.259V	340-342 #DAC / 1.514V
Signal value @ 10pe	235 #DAC / 1.300V	137 #DAC / 1.085V	115 #DAC / 1.038V
Signal amplitude @ 10pe (signal minus pedestal)	50 #DAC / 110mV	83 #DAC / 174mV	226 #DAC / 476mV
Gain (mV/pe)	**10.4mV/pe (5 #DAC/pe)**	**17.4mV (8.3 #DAC)**	**47.6mV/pe (22.6 #DAC/pe)**
Jitter - threshold 1 pe @10pe	**13ps RMS**	**6ps RMS**	**8ps RMS**
Jitter - threshold 3 pe @10pe	**8ps RMS**	**6ps RMS**	**8ps RMS**
With 100nF DC block (for voltage gain & BW meas.)	**18mV injection**	**18mV injection**	**7mV injection**
Signal Value	267 #DAC / 1.371V	41 #DAC / 0.884V	192 #DAC / 1.2V
Signal amplitude (signal minus pedestal)	81 #DAC / 175mV	179 #DAC / 375mV	150 #DAC / 320mV
Voltage gain (before 50 ohm bridge => factor of 0 .5)	**4.86 V/V**	**10.4 V/V**	**22.5 V/V**
Bandwidth, after discriminator (Δt 10% T50% meas.)	**Δt : 150ps / 660MHz**	**Δt : 360ps / 280MHz**	**Δt : 400ps / 250MHz**

⇒ Design of PETIROC1: 16 channels with RF amplifier

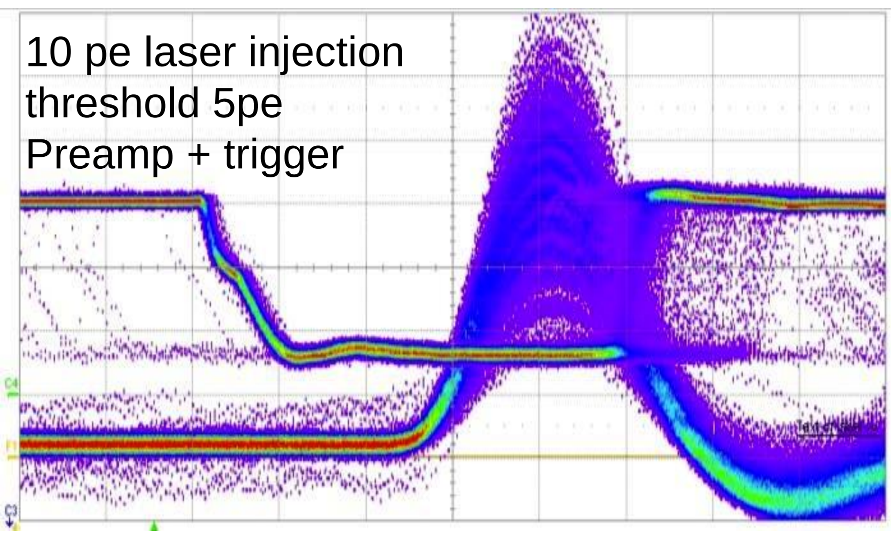
⇒ PETIROC2 32ch   TRIROC 64 ch

PETIROC1: Triggers on first pe

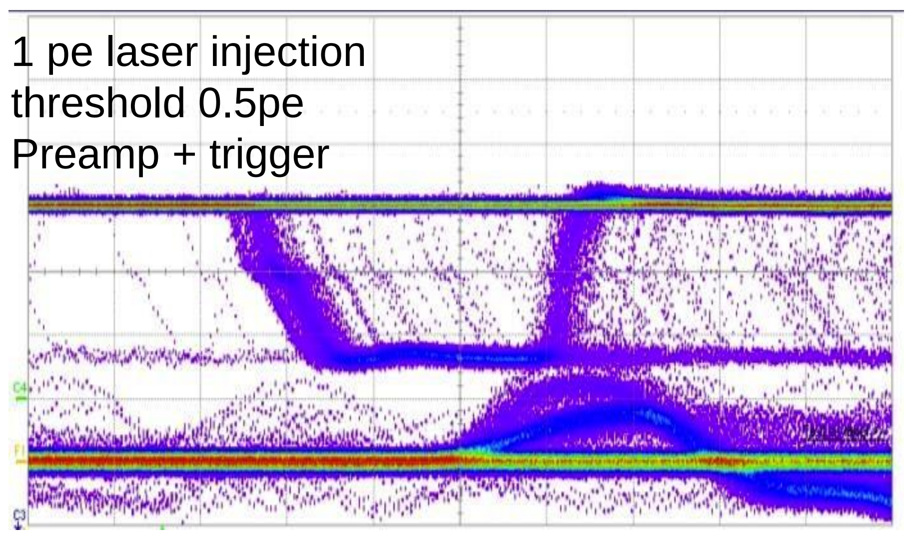
- Tests on EPTIROC1 (analog version of PETIROC2)
- 1x1mm SiPM Hamamatsu
- Laser for low light injection
  - 405nm, Jitter : 28 ps FWMH
- Petiroc can trigger on first photoelectron
- Petiroc is low noise : single photon identification



2 ns/div



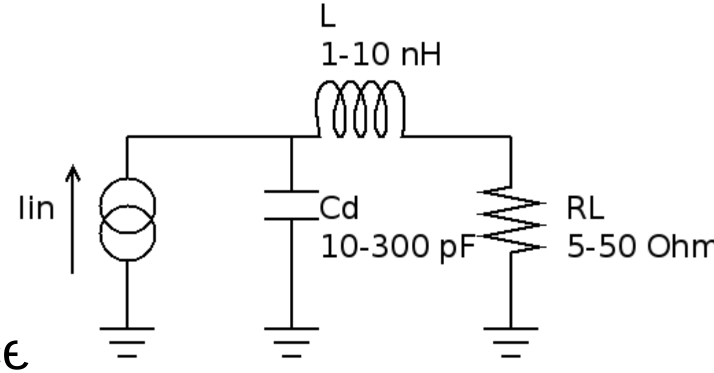
2 ns/div

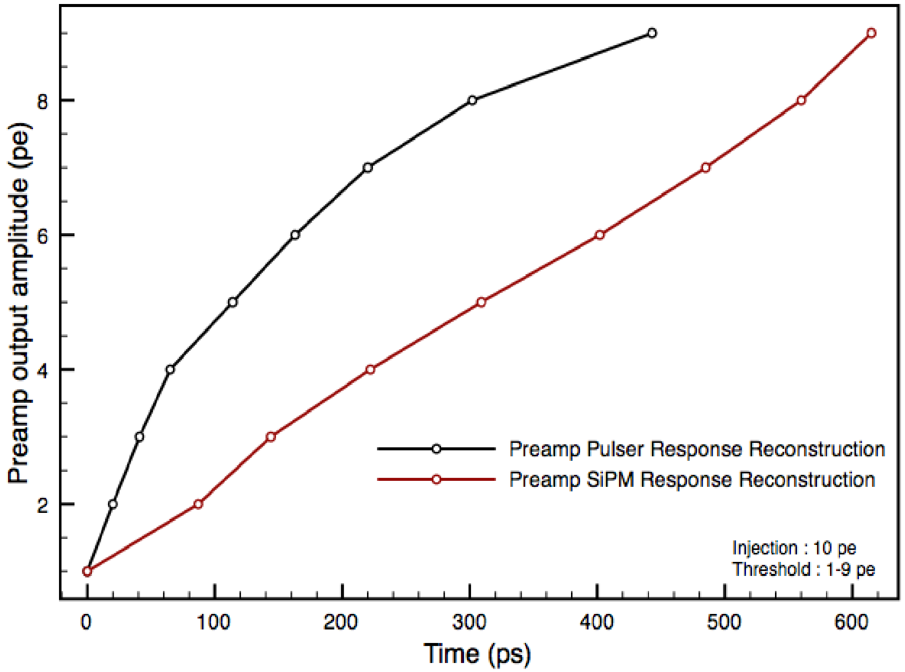


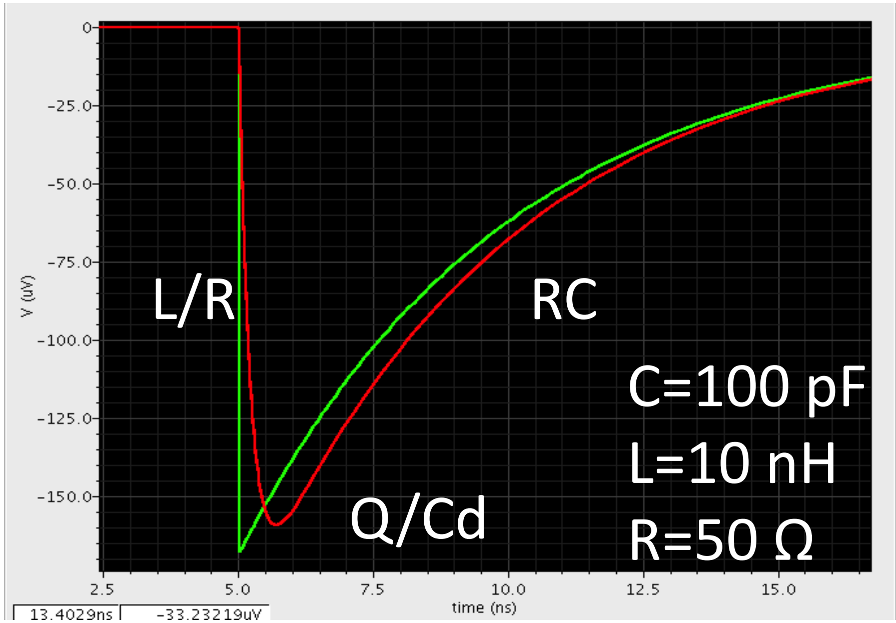
2 ns/div

Petiroc : bandwidth issues

- Pulser vs SiPM comparison
- SiPM is significantly slower than Petiroc
  - Pulser with 100pF injection capacitance, 10pe injected
  - SiPM illuminated with laser pulse, 10pe measured
  - Threshold from 1pe to 9pe
- Petiroc bandwidth meas. : 877MHz with pulser
- With SiPm: limitation due to the stray inductance

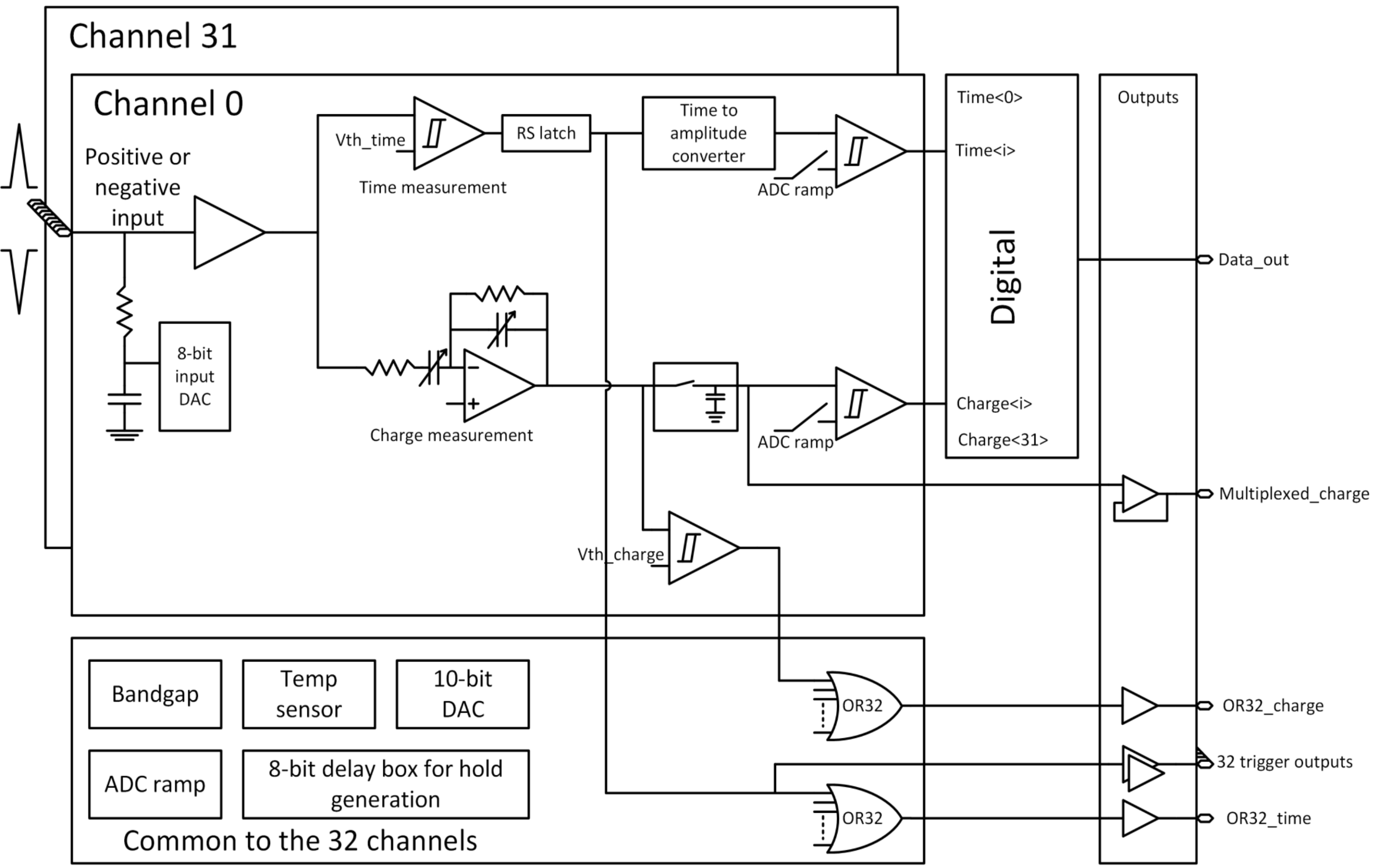


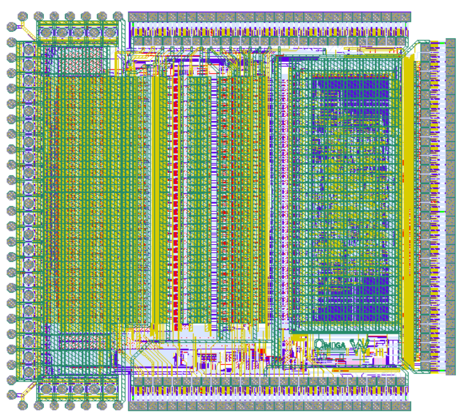




PETIROC2

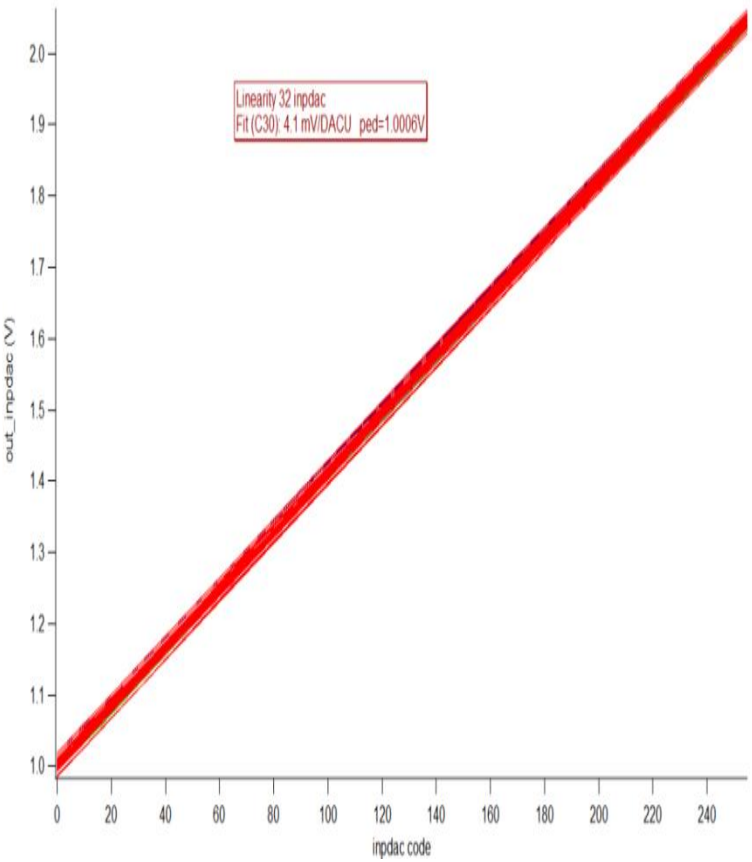
- 32 ch SiPM GHz readout ASIC, dual polarity, 100 fC-400 pC, 6 mW/ch
- 32 trigger outputs and multiplexed data output
- Embedded 10 bit ADC and 50 ps TDC
- Dual threshold : first photons and energy



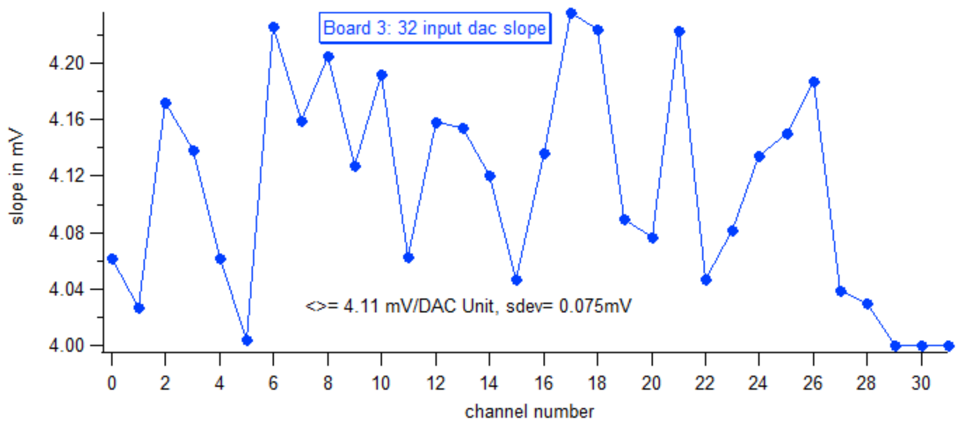


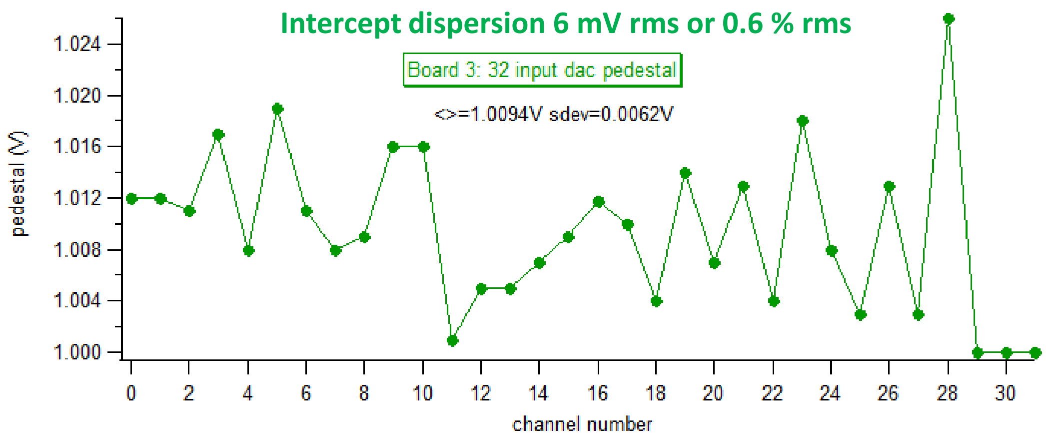
PETIROC2: Input DAC uniformity

- Linearity and dispersion of the 32 8-bit input DAC



Slope dispersion 75 uV rms or 2% rms

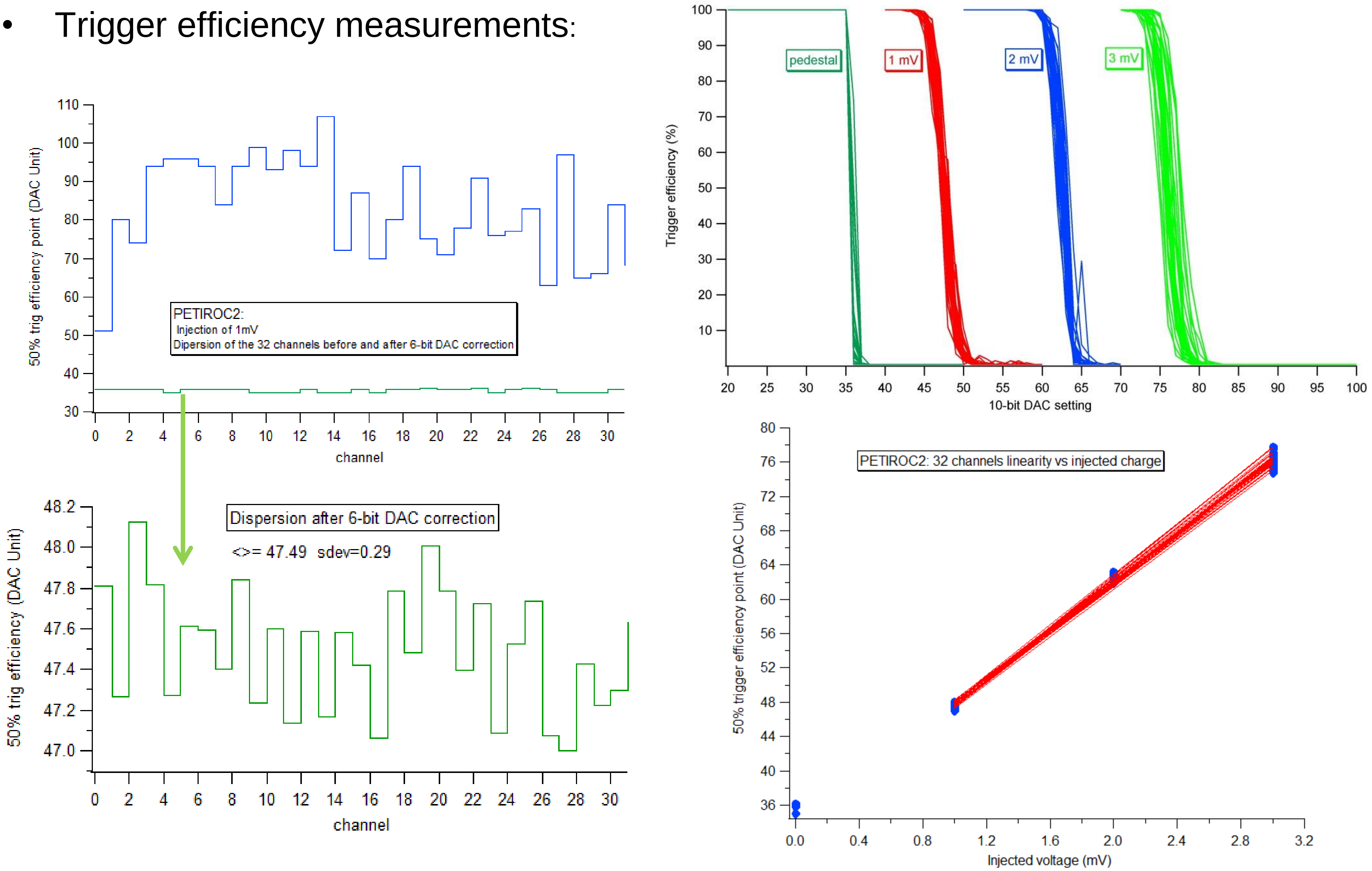




PETIROC2: « S-curves »

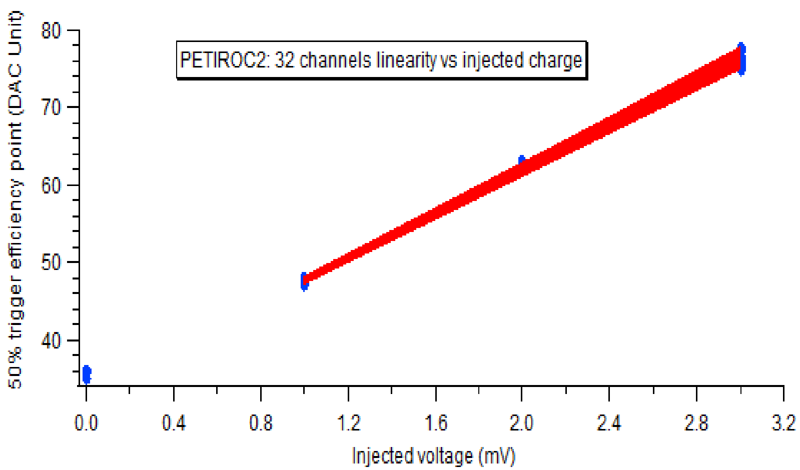
Ωmega

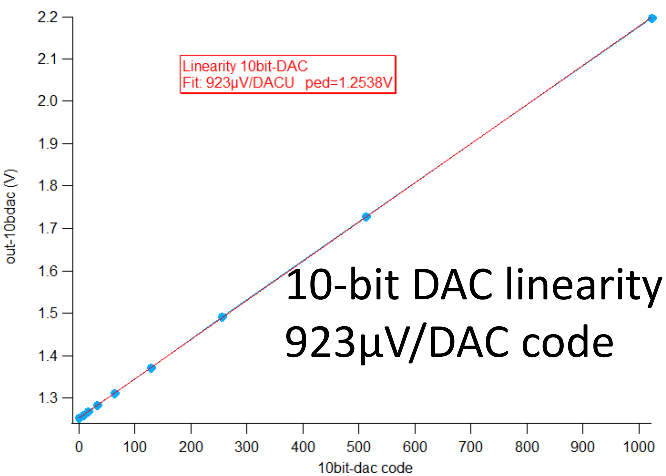
- Trigger efficiency measurements:

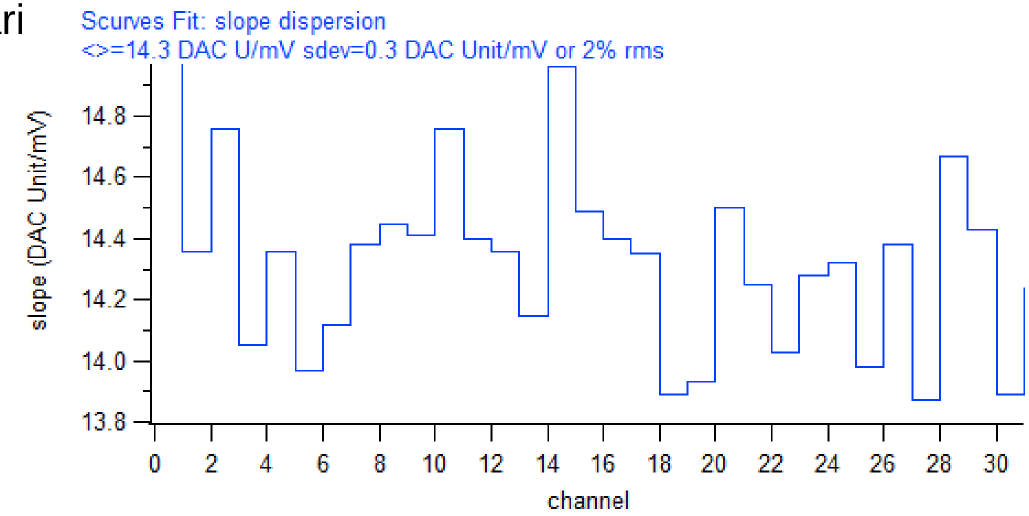


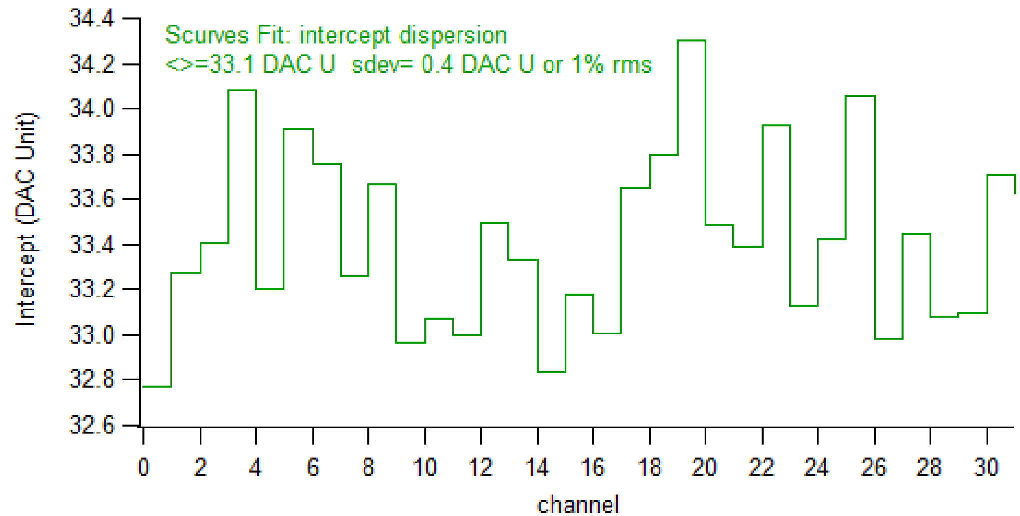
PETIROC2: efficiency uniformity

- Trigger efficiency measurements: Lineari
- One 10-bit DAC Unit= 923 µV





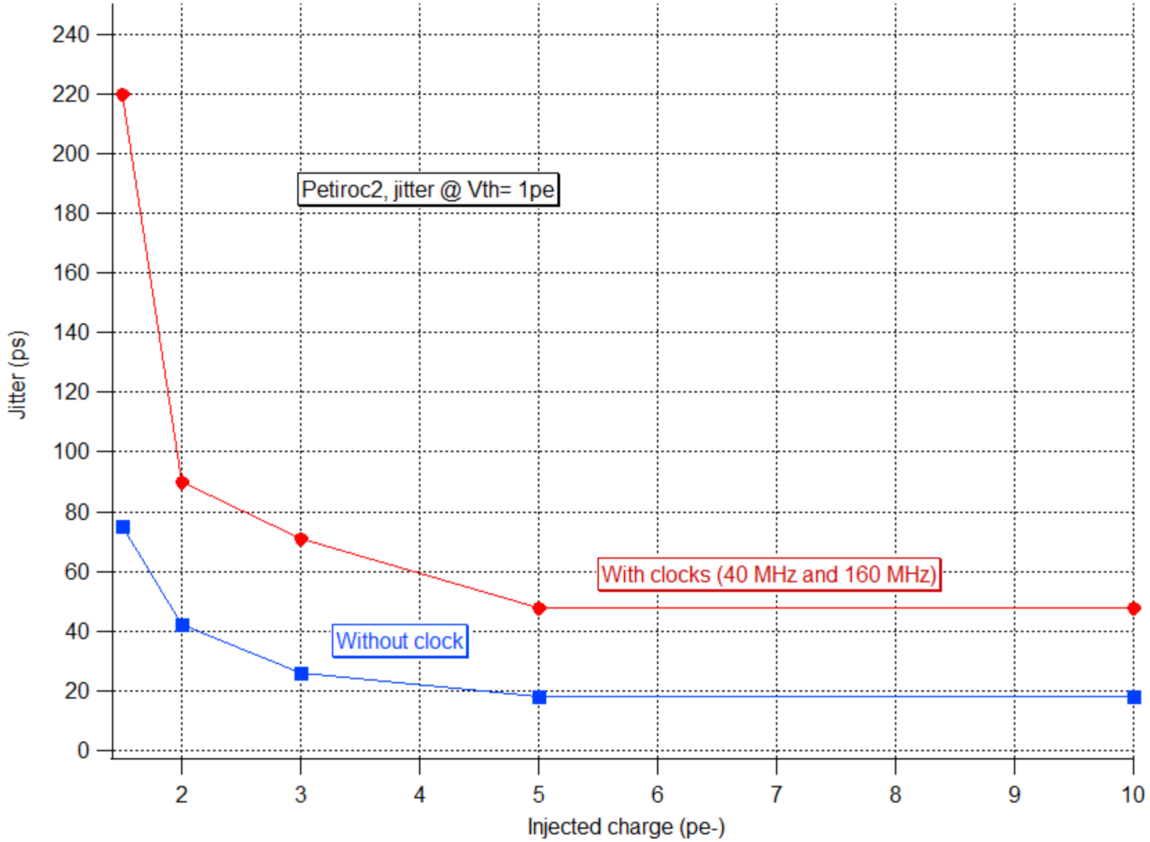




PETIROC2: Time measurement

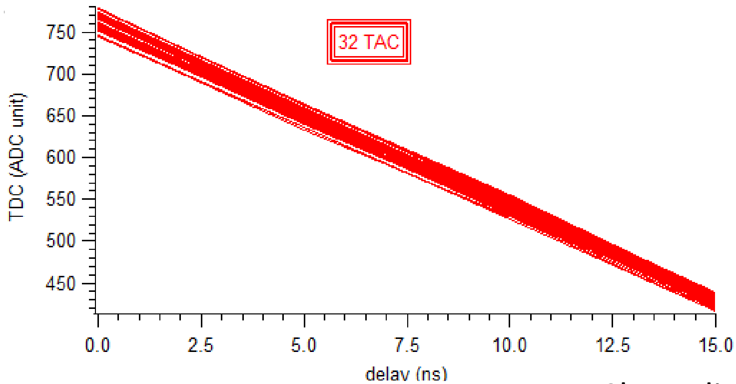
Omega

- Jitter vs threshold & injection
- Jitter improves with signal
- Clock couplings (understood)
- Jitter below 20ps

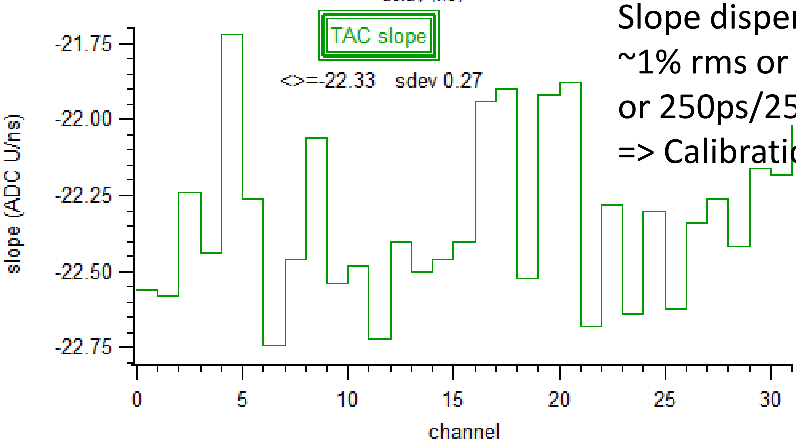


PETIROC2: TAC measurement

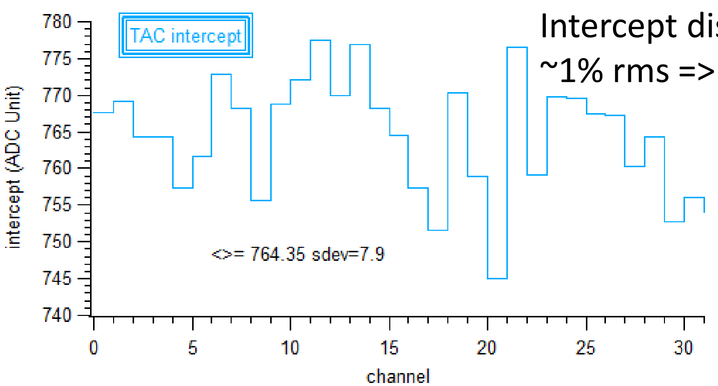
Omega



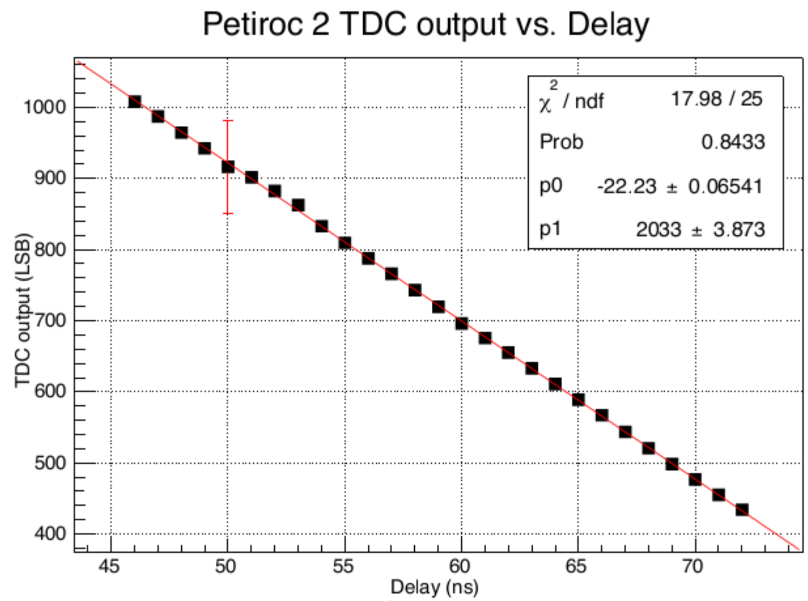
weeroc

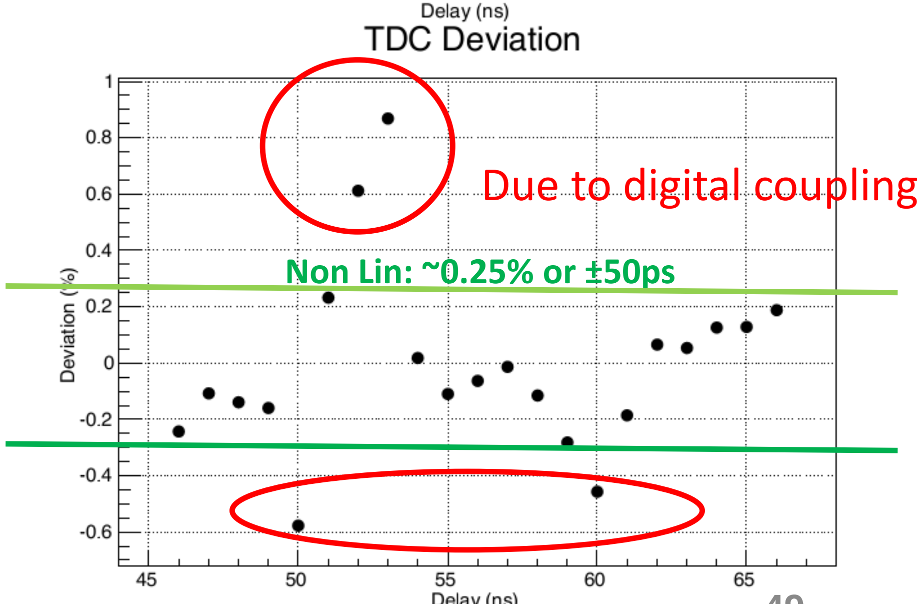


Slope dispersion:
~1% rms or 10ps/1ns
or 250ps/25ns
=> Calibration



Intercept dispersion:
~1% rms => Calibration

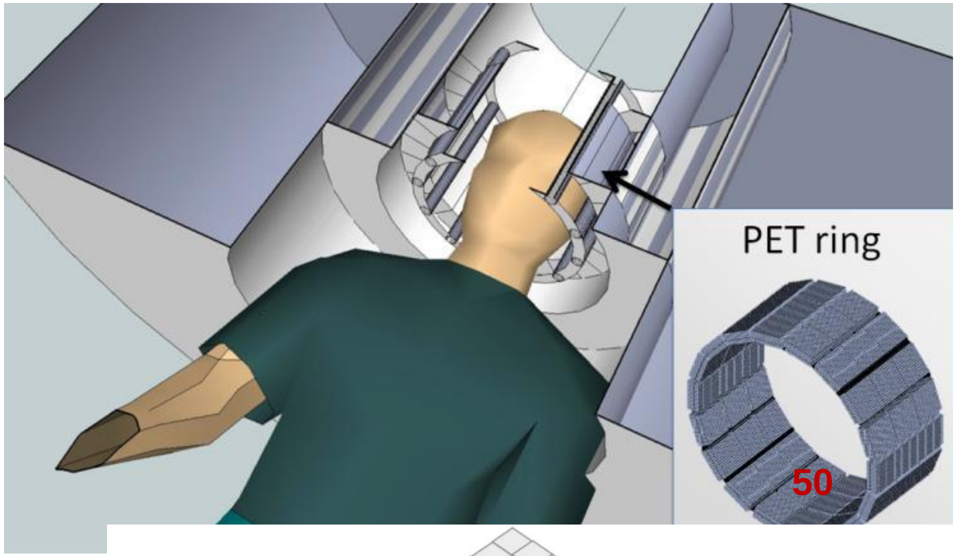


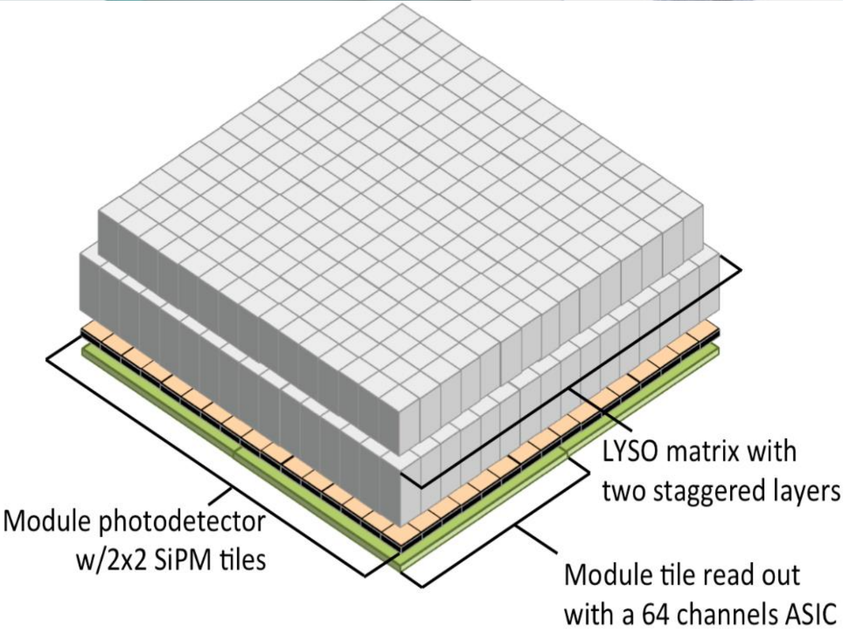


The TRIMAGE european project

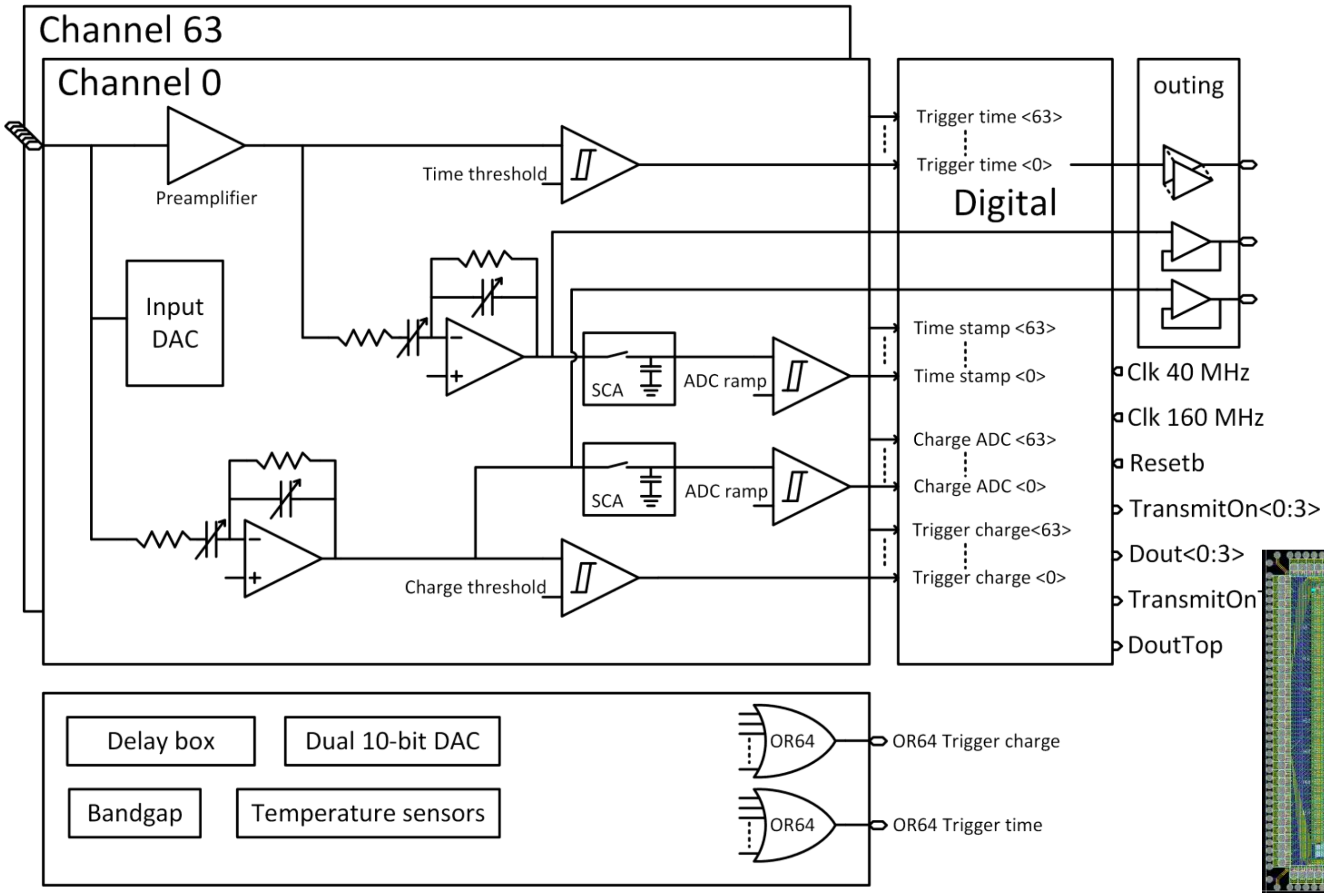
- Cost effective tri-modality (PET – MR – EEG) imaging tools

Project Partners	Role in the project
University of Pisa (UNIPI)	Coordinator & PET system development
Technological Educational Institute of Athens (TEIA)	Dissemination & Monte Carlo simulations
Forschungszentrum Juelich GmbH (FZJ)	Coil design & PET/MR/EEG integration
JARA BRAIN, RWTH (JRB)	Clinical application
Technische Universitat Munich (TUM)	Image quantification & clinical application
University of Zurich (PUK)	Patient recruitment & clinical data analysis
Istituto Nazionale di Fisica Nucleare (INFN)	PET system development & characterization
AdvanSiD (ASD)	SiPMs and chip-scale package development
Weeroc (WRC)	PET modules production & testing
Raytest GmbH (RAY)	Mechanical parts design & market strategy
RS2D (RS2D)	Design, assembly, test 1.5T MRI

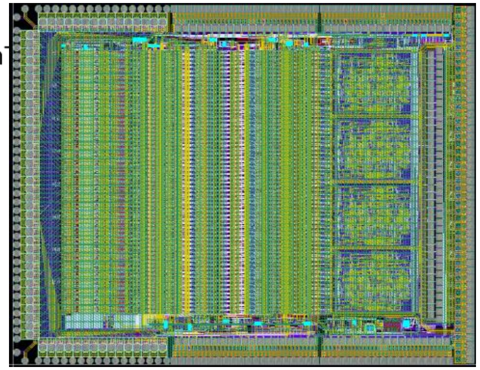




- 64-channel SiPM readout : positive & negative polarity inputs
- 8-bit Input DAC for SiPM HV tuning
- Time Stamp and ADC charge outputs



weeroc



Technology transfer

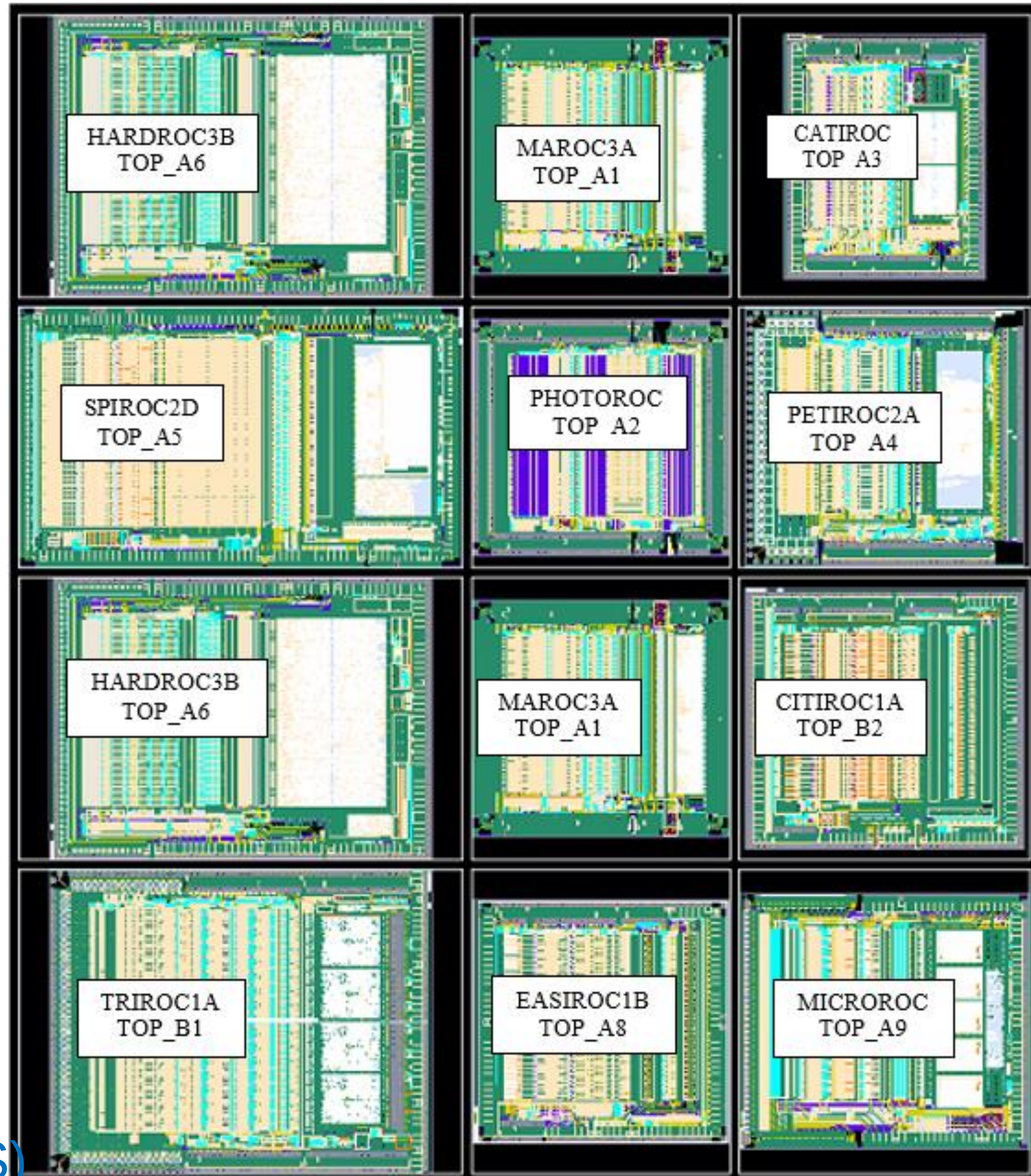
Ωmega

- Several chips transfered to other academic users
- Non-profit « academic price »
- Industry transfer via startup « WEEROC »

chip	year	IN2P3 users	external users
MAROC3	2010	**LAL**, APC, CSNSM	NEVIS, KEK, CERN, Roma, Seoul, Pisa, Bari, Genève, Mocow, Valencia, Kolkata, Durham, Bruxelles, München, Jülich, Valparaiso, Lisboa, Bristol, Frascatti, Budapest, Catania, Glasgow, Coimbra, Grenoble
HARDROC2B	2010	**IPNL**, LPCCF	
SPIROC2B	2010		**DESY (D)**, TOHOKU (JP), Bergen (N)
SKIROC2	2010	LAL, **LLR**	IHEP
SPACIROC1	2010	**APC**, LAL	
EASIROC	2010	**IMNC**, LAL, LLR,	Palermo, FNAL, KEK, München, Dijon, CERN, Roma, Aachen, Toulouse, Lyon, Seoul, Bari, Tokyo, Pusan, Kyushu, Osaka
PARISROC2	2010	**IPNO**, LAPP, LLR, APC	IHEP
CITIROC	2013		**INAF**, CERN, JLAB, Rio, Berne, Mendoza, Aachen
PETIROC2	2013	**IPNL**, LPCCF	KEK, Tohoku

Production Run : Feb 2015

- MAROC3A
- PHOTOROC ~~*(MAROC4)*~~
- HARDROC3B (RPC)
- SPIROC2D (SiPM)
- ~~**SKIROC2B (Si PIN)**~~
- CATIROC ~~*(PARISROC3)*~~
- PETIROC2A
- ~~SPACIROC3A~~
- CITIROC1A
- ~~CITIROC1B~~
- EASIROC1B
- ~~DOSIROC1A~~
- ~~DOPIROC2~~
- TRIROC1A
- MICROROC (µMEGAS)



Evolution of SiGe for HEP

- Motivation :
  - SiGe 0,35µm getting outdated
  - Particularly for digital part too slow
- AIDA2020 EU proposal
  - Microelectronics workpackage to study 130/180 nm SiGe process
  - Proposed consortium to share expertise on SiGe
  - Study for LHC run 2, ILC…

RF and HPA Applications and Technology

Front-End Modules

RF SOI and SiGe Power Amplifiers

- Power Amplifiers
- Antenna Switch
- PA Controllers

mmWave

High Performance SiGe

- Optical Fiber Networks
- Automotive Radar
- 60 GHz WiFi, Backhaul MW
- Light Peak and Thunderbolt

High Performance Analog

Complementary BiCMOS

- Line Drivers DSL, HomePlug, ATE
- HDD PreAmp
- OpAmps, DAC, ADC

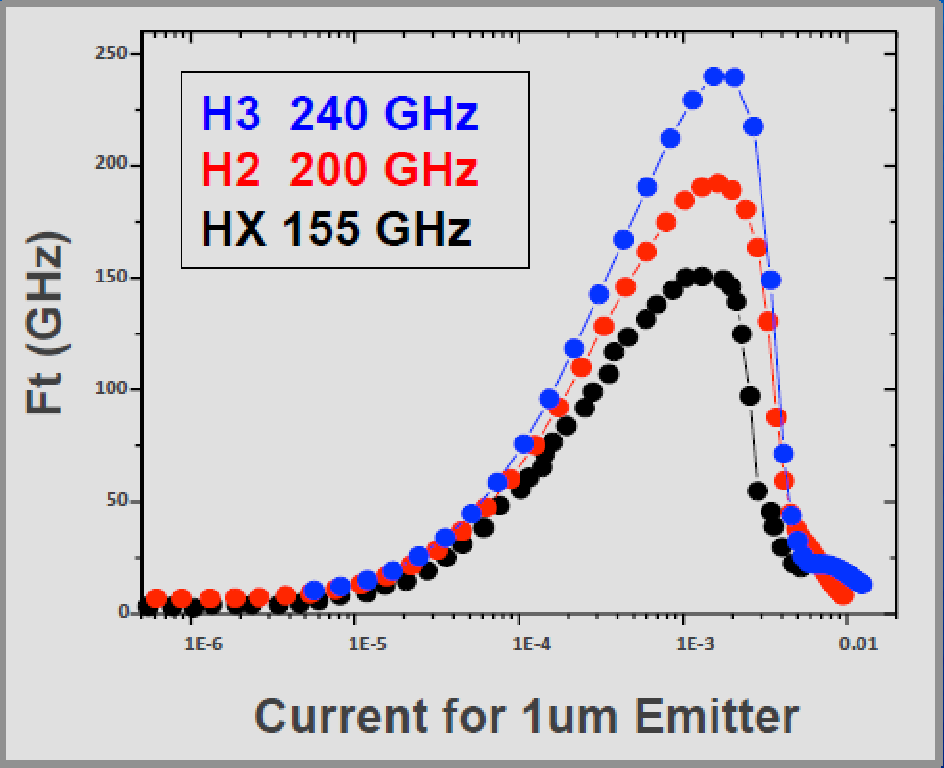
RF and Tuners

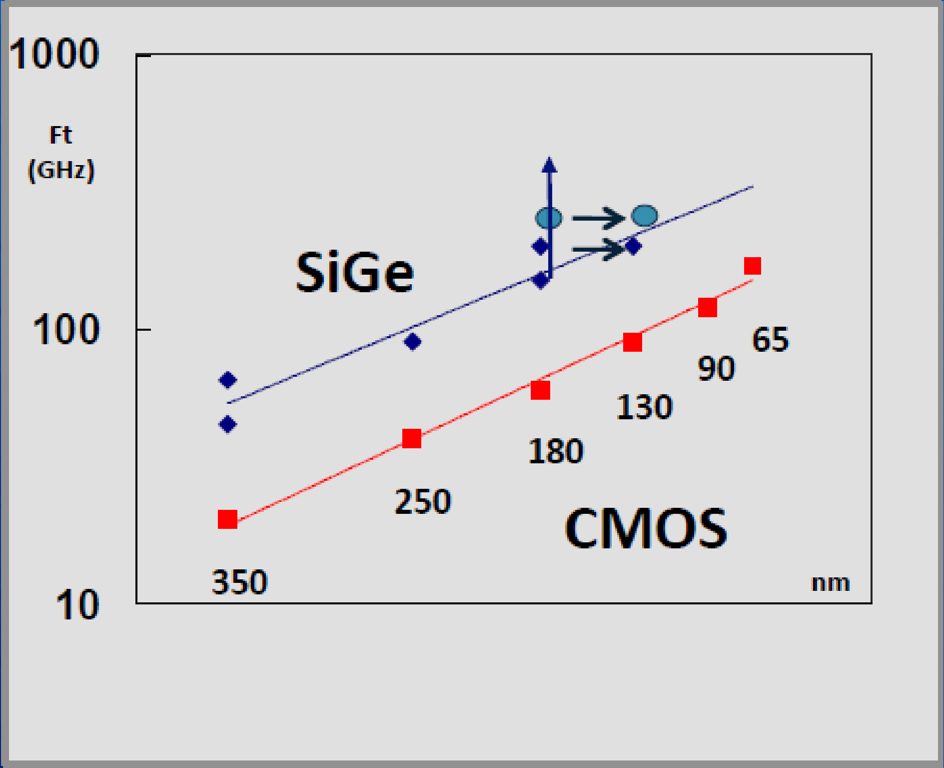
RF CMOS and SiGe BiCMOS

- Cell Phones, WiFi TxRx
- Basestation, Specialty Wireless
- TV, Satellite, STB Tuners

Best-in-class SiGe, RF CMOS, RF models and Design Enablement

High Performance SiGe



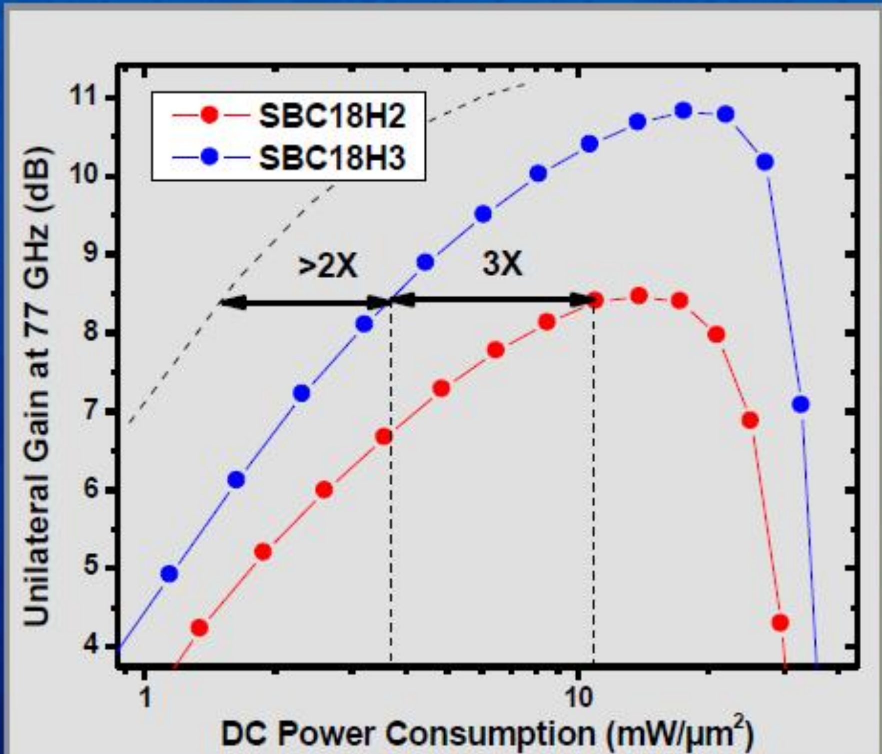


NEW

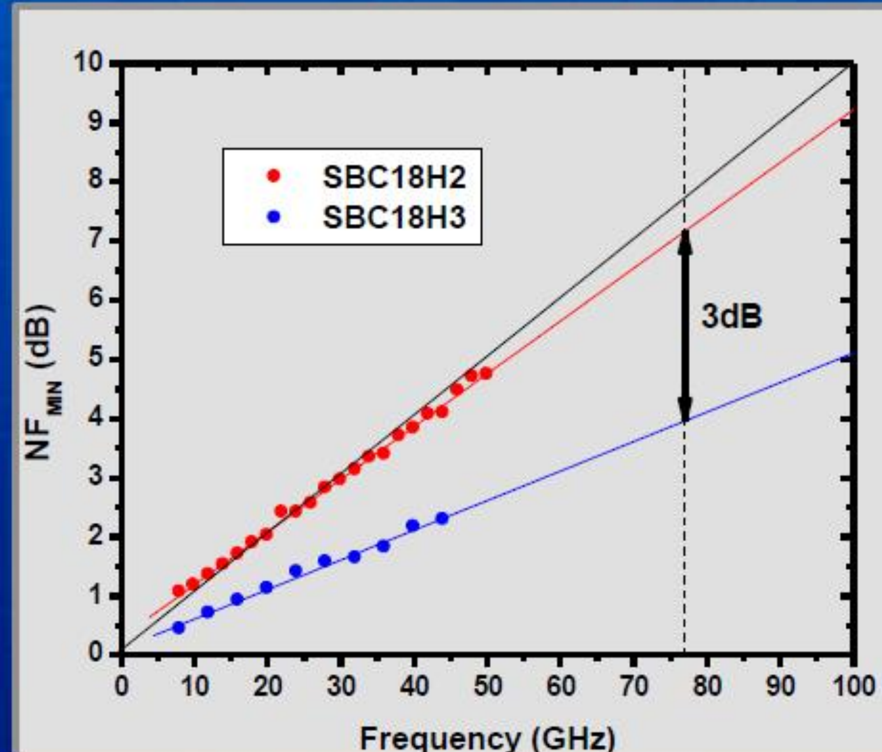
- **SBC18H3:** PDK for 0.13um version (SBC13)
- **SBC18H4:** 1st successful Shuttle (11 customers)
- **SBC18H5:** Target for >400 GHz Fmax

TOWERJAZZ

SBC18H3



Ft = 240 GHz, Fmax = 280 GHz

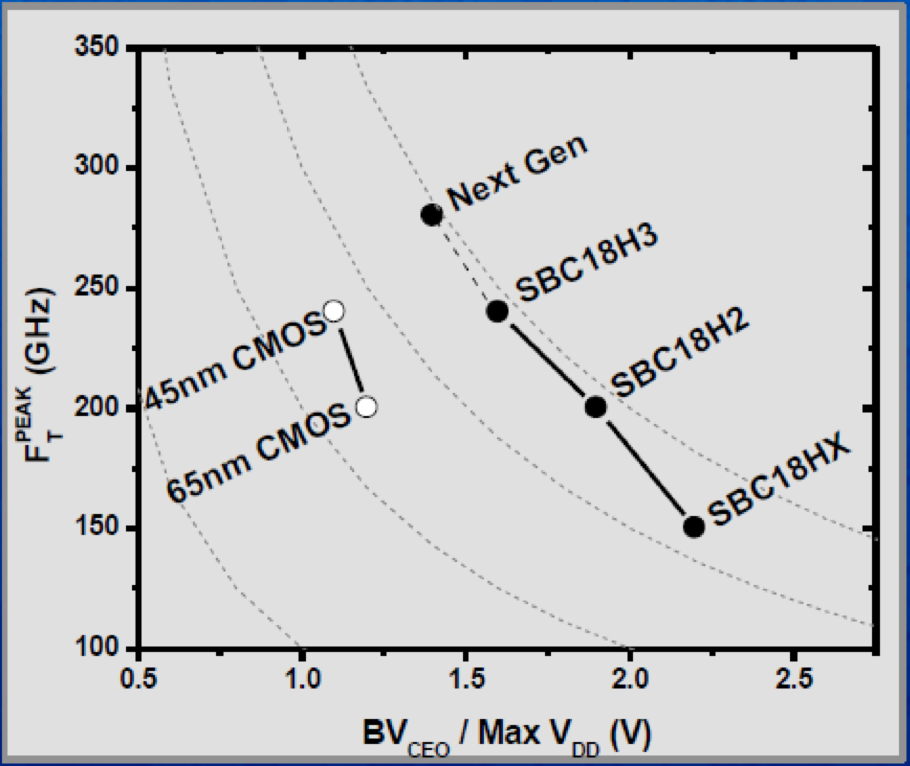


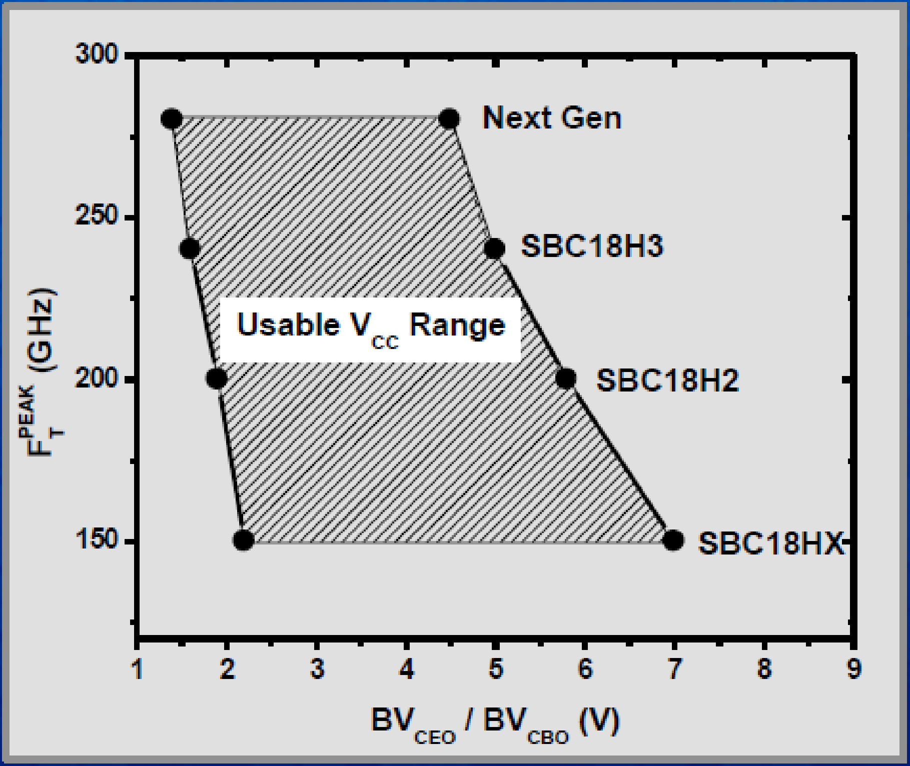
Minimum Noise Figure of 2 dB at 40 GHz

Best in Class SiGe Speed/Power

Best in Class Noise

High Performance SiGe: High Dynamic Range





SiGe Technology Offers Greater Dynamic Range than Equivalent RFCMOS Nodes

0.13um RF CMOS and SiGe BiCMOS

	TS13	TSBL13	SBL13	SBC13	
1.0 V CMOS	Option	No	No	No	
1.2 V CMOS	Yes	Yes	Yes	Yes	
2.5 V CMOS	Option	No	No	No	
3.3 V CMOS	Yes	Yes	Yes	Yes	
Vt Options	Std/Low/Hi	Std/Low/Hi	Std/Low/Hi	Std/Low/Hi	
SiGe NPN Ft	No	90/67/37	90/67/37	200/75	GHz
SiGe NPN BVceo	No	2.4/3.5/6.0	2.4/3.5/6.0	2/3.5	GHz
Triple Well	Option	Option	Option	Option	GHz
Native FET	Option	Option	Option	Option	
MIM Cap	1,1.5, 2	2	2.8, 5.6	2.8, 5.6	fF/um2
Poly Resistor	256/320/1K	310/1K	310/1K	310/1K	ohm/sq
Metal Layers	6, 7, 8	6, 7	6	6	
Metal Material	Cu	Cu	Al	Al	
Top Metal (um)	3.3 or 3.3 / 3.3	3.3	3	3	um

Conclusion

- SiGe is an interesting technology for high speed, low power, large dynamic range readout chips

- A large family of ROC ASICs has been realized by OMEGA over the last 10 years in AMS SiGe 350 nm. They are used by many groups and available for research.

- A new SiGe 130nm is now being investigated within AIDA2020 EU program to enhance analog and digital performance of SoC

SUMMARY

http://omega.in2p3.fr/ http://www.weeroc.com/ Ωmega

Chip	Detector	Ch	Polarity	Dyn Range	Specificities
MAROC	PM	64	<0	5 fC - 5 pC	64 trig outputs, internal 8/10/12-bit ADC (for charge measurment)
SPACIROC	PM	64	<0	2 pC- 220 pC	Fast photon counting (50MHz)
PARISROC	PM	16	<0	50 fC - 100 pC	Internal TDC (<1ns), 16 trig outputs
HARDROC	RPC	64	<0	2 fC - 10 pC	3 discriminators, 128 deep digital memory to store 2x64 discriminator encoded data
MICROROC	µMEGAS/GEM	64	<0	0.2 fC - 500 fC	3 discriminators, 128 deep digital memory to store 2x64 discriminator encoded data
SKIROC	Si pin diodes	64	>0	0.3 f C - 10 pC	Internal 12-bit ADC for charge measurement
SPIROC	SiPM	36	>0	10 fC - 300 pC	36 HV SiPM tuning (8 bits), Internal 12-bit ADC for charge and time measurement
EASIROC	SiPM	32	>0	10 fC - 300 pC	32 HV SiPM tuning (8 bits), 32 trigger outputs
CITIROC	SiPM	32	>0	10 fC - 300 pC	32 HV SiPM tuning (8 bits), 32 trigger outputs
PETIROC	SiPM	32	<0	100fC – 300 pC	32 HV SiPM tuning (8 bits), 32 trigger outputs, Internal 10-bit ADC for charge and time measurement (25 ps)
TRIROC	SiPM	64	Both	100 fC- 300 pC	64 HV SiPM tuning (8 bits), 64 trigger outputs, Internal 10-bit ADC for charge and time measurement (25 ps)

Backup slides

Summary

Omega

- Main activity : Analog and mixed-signal ASIC design

- Research topics :
  - multi-channel ASICs for particle physics and astrophysics detectors
  - BiCMOS SiGe and deep submicron CMOS technologies
  - ultra-low noise, low power and high speed design
  - radiation tolerance, reliability and space applications
  - integration with sensors and System on Chip (SoC)
  - chips for photodetectors, semiconductors or gaseous detectors

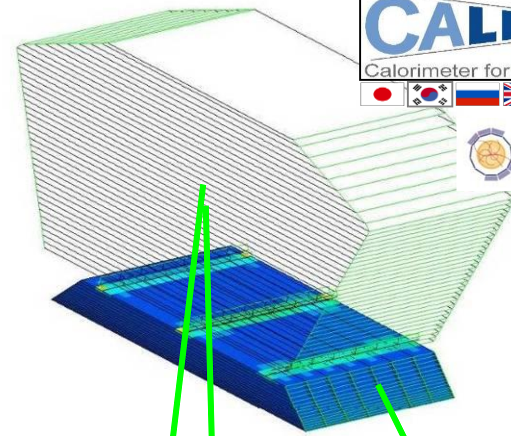
- Specific Applications :
  - medical imaging
  - low light "single photon" imaging
  - utilization in space

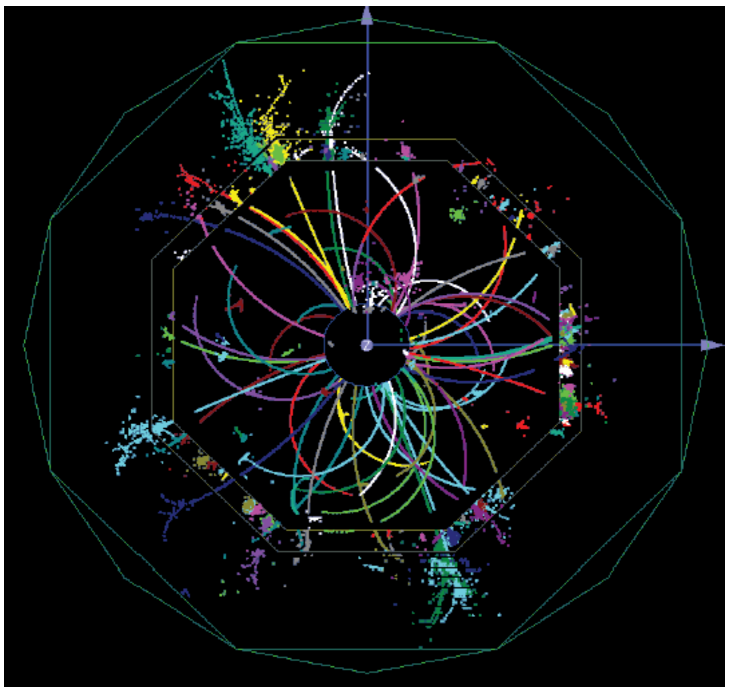
0.18um RF CMOS and SiGe BiCMOS

	CA18	SBL18	SBC18PA	SBC18	SBC18H2	SBC18H3	
1.8 V CMOS	Yes	Yes	Option	Option	Yes	Yes	
3.3 V CMOS	Yes	Yes	No	Yes	Yes	Yes	
5 V CMOS	w/ LDMOS	No	Yes	Yes	No	No	
SiGe Ft	No	90, 67, 37	30	155, 78, 38	200, 75	240, 55	GHz
SiGe Fmax	No	123, 115,100	168	200, 190, 150	200, 150	270, 100	GHz
SiGe BVceo	No	2.4, 3.5, 6	8	2.2, 3.5, 6	1.9, 3.5	1.6, 3.2	V
HS PNP Ft	No	23	No	17	No	No	GHz
Triple Well	Option	Option	Option	Option	Option	Option	
Native FET	Option	No	No	Option	No	No	
SOI	Option	No	No	Option	No	No	
MIM Cap	2, 4	2, 4	2	1, 2, 4, 5.6	2	2.8,5.6	fF/um2
Poly Resistor	310, 1000	235, 1000	235, 1000	235, 1000	235, 1000	235, 1000	ohm/sq
Metal Resistor	No	No	No	24	24	24	ohm/sq
DSV / TSV	No	No	Option	Option	No	No	
Metal Layers	4, 5, 6	5	4	3, 4, 5, 6	6	6	
Metal Material	Al	Al	Al	Al	Al	Al	
Top Metal	3	3	3, 5.2	3, 5.2	3	3	um

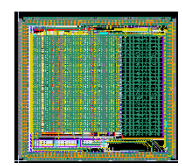
CALICE = « imaging calorimetry »

- Calorimeter readout: auto-trigger, analog storage, digitization and token-ring readout…
- power pulsing : <1 % duty cycle
- Optimized commonalities within EUDET/AIDA

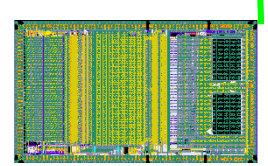




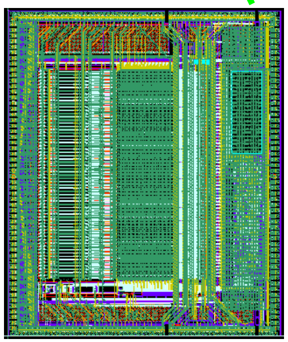
HARDROC2
SDHCAL RPC
64 ch 16 mm²



SPIROC2
AHCAL SiPM
36 ch 30 mm²



SKIROC2
ECAL Si
64 ch. 70 mm²

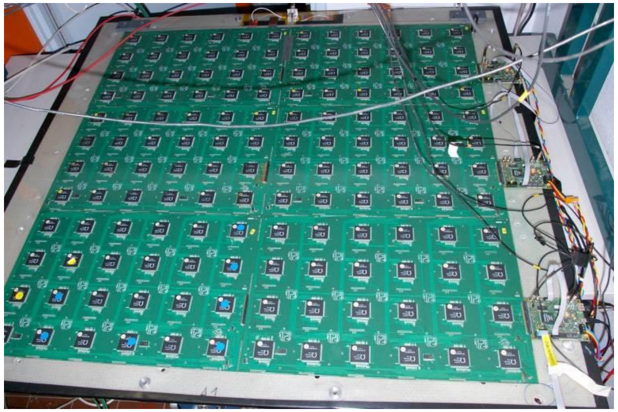


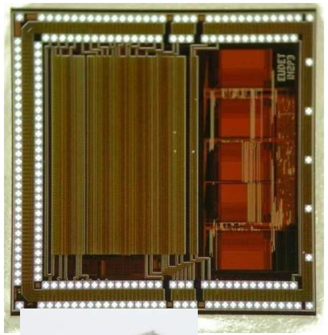
FLC_PHY3 (2003)

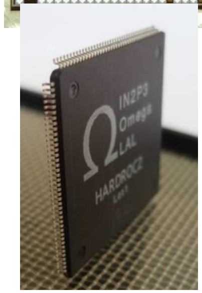
Omega

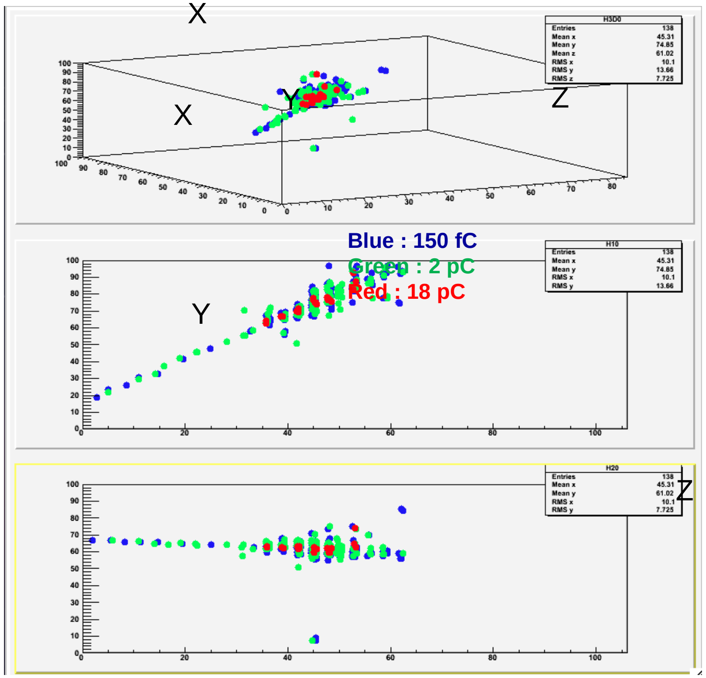
- **HARDROC2: 64 channels (RPC DHCAL)**
  - preamp + shaper+ 3 discris (semi digital readout)
  - Auto trigger on 10fC up to 20 pC
  - 5 0.5 Kbytes memories to store 127 events
  - Full power pulsing => 7.5 µW/ch
  - Fully integrated ILC sequential readout
  - 10 000 chips produced to equip 400 000 ch
  - SDHCAL technological proto with 40 layers (5760 HR2 chips)
    - Successful TB in 2012 : 40 layers with Power Pulsing mode

Cosmic hadronic shower





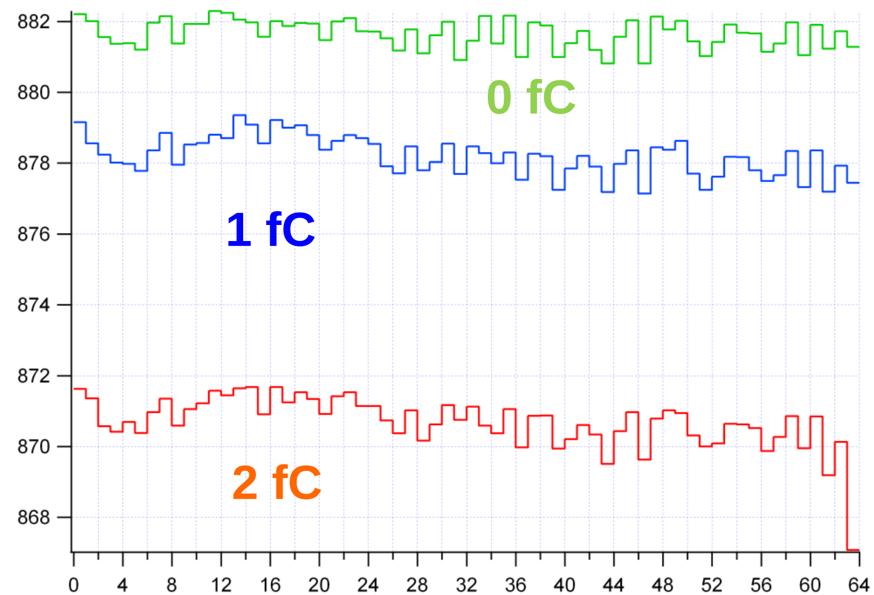




lapp Laboratoire d'Annecy-le-Vieux de Physique des Particules

ipnl

MICROROC: 64 channels for µMegas (DHCAL ILC)



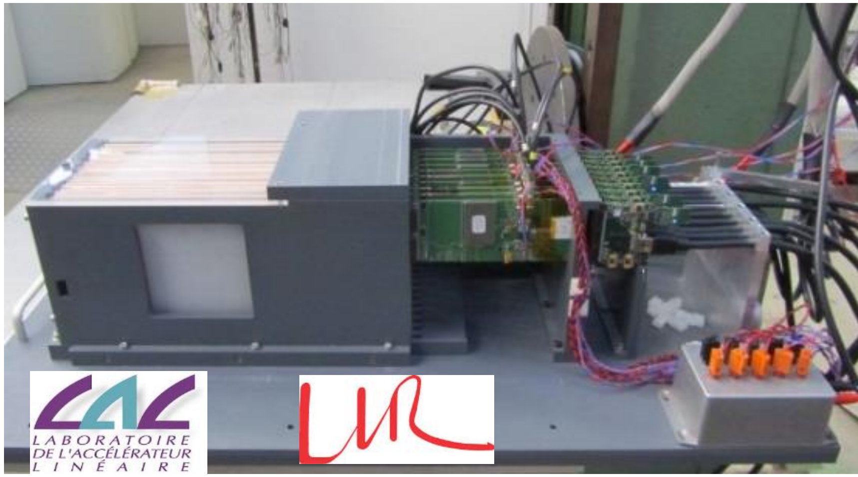
- ❑ Very similar to HARDROC except for the input preamp (collaboration with LAPP Annecy) and shapers (100-150 ns)
- ❑ Noise: **0.2fC Cd=80 pF => Auto trigger on 1fC** up to 500fC
- ❑ Pulsed power: **10 µW/ch** (0.5 % duty cycle)
- ❑ **HV sparks protection**
- ❑ 1 m2 in TB in August and October 2011. Very good performance of the electronics and detector (Threshold set to 1fC).
- ❑ 2012: 4 m2 in TB

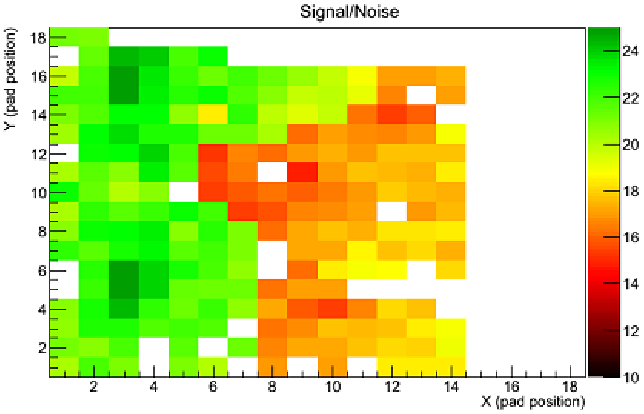
@LAPP Annecy

1m2 equipped with 144 MICROROC

SKIROC : SiECAL chip

- 64 ch Si readout chip
  - Autotrigger @ ½ MIP = 2 fC
  - Charge measurement 15 bits
  - Time measurement 1 ns





S/N > 10